ECE 4570 Electronic Device Fundamentals

Fall 2019
Dept of Electrical & Computer Engineering
Cornell University
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Final Exam (Solutions)
12/19/2019
2:00-4:30 pm

NOTE: Solve analytically before substituting numerical values. Provide sketches with labels wherever the situation demands. State your approximations clearly, and use your intuition to cut down the math.

Problem 1 (20 Points): Miscellaneous

a) Prove that the maximum conductance of an electron mode is q^2/h (the quantum of conductance).
b) Explain why the pn junction, the Schottky diode, the bipolar transistor, and the FET all have ideal 'subthreshold slope' of SS = k_bT*ln(10), which is 60 mV/decade @300K.
c) Explain why the SS of part b) limits the low-energy limit of electronic device performance.
d) Explain why Zener and Avalanche breakdown limit the high-energy performance of electronic devices.

Solutions by Kathleen Smith:

Problem 1

a) Using current in 1-D for simplicity's sake, but the arguement scales.

$$I = q n v \; ; \; n = [L^{-1}]$$

$$= \frac{q g_s g_v}{L} \sum_k f(k)\, v_g(k)$$

$$v_g(k) = \frac{1}{\hbar}\frac{\partial E(k)}{dk} \; ; \; E(k) = \frac{\hbar^2 k^2}{2m^*}, \; \frac{\partial E}{\partial k} = \frac{\hbar^2 k}{m^*}$$

$$I = \frac{q g_s g_v}{\hbar L}\int_{-\infty}^{\infty} \frac{f(k)}{2\pi/L}\frac{\partial E(k)}{dk}\, dk$$

$$= \frac{q g_s g_v}{h}\int_{-\infty}^{\infty} f(k)\, \partial E$$

$$f(k) = f(E) = \frac{1}{1+\exp\left(\frac{E-E_F}{k_BT}\right)}$$

$$I = \frac{q g_s g_v}{h} k_B T \left[F_0\left(\frac{E_{F,S}-E_F}{k_BT}\right) - F_0\left(\frac{E_{F,D}-E_F}{k_BT}\right)\right]$$

$$= \frac{q g_s g_v}{h} k_B T \ln\left[\frac{1+\exp\left(\frac{E_{F,S}-E_F}{k_BT}\right)}{1+\exp\left(\frac{E_{F,D}-E_F}{k_BT}\right)}\right]$$

$$\text{Conductance} = \frac{I}{V}$$

@ $T = 0$

$$I \to \frac{q g_s g_v}{h} k_B T \left[1 + \frac{E_{F,S}-E_F}{k_BT} + 1 - \frac{E_{F,D}-E_F}{k_BT}\right]$$

$$= \frac{q g_s g_v}{h}(E_{F,S} - E_{F,D}) = \frac{q g_s g_v}{h} q V$$

$$\frac{I}{V} = \frac{q^2}{h} g_s g_v \Rightarrow$$ quantum of conductance is q^2/h

b) Current is proportional to the number of carriers. For a device under bias, electrons and holes have different Fermi levels, which alters the carrier statistics. Under bias:

$$np = n_i^2 \exp\left(\frac{E_{fn} - E_{fp}}{k_B T}\right) = n_i^2 \exp\left(\frac{qV}{kT}\right)$$

For all of these devices, the number of carriers that are available to generate current is therefore

$$n \propto \exp\left(\frac{qV}{kT}\right)$$

& therefore

$$I \propto \exp\left(\frac{qV}{kT}\right).$$

below threshold.

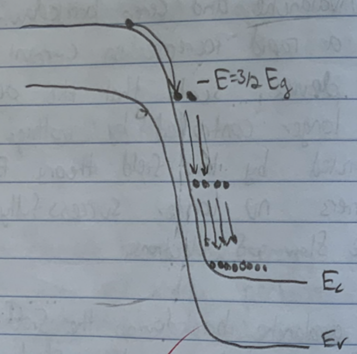
The subthreshold slope, measured on a $\log_{10}$ scale, is therefore

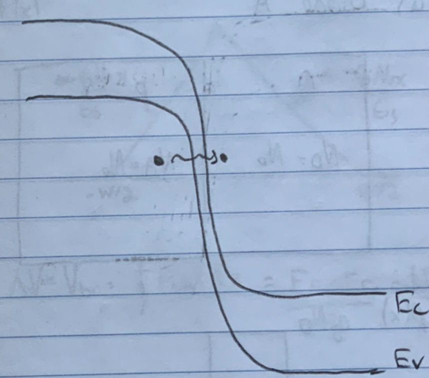
$$I \propto \frac{kT}{q} \ln 10$$

c) The SS limits low energy performance because low energy performance aims to get the greatest increase in current from the smallest possible increase in voltage, since power dissipated, $P = IV$. The SS sets the maximum allowed change in current per voltage increase and therefore sets the minimum power required to attain a desired current.

2) Avalanche and Zener breakdown lead to a rapid increase in current in a device, such that the device is no longer controlled by voltage as predicted by low field theory. Energy barriers no longer successfully block the flow of electrons.

In avalanche breakdown, the field is sufficiently high such that electrons have enough kinetic energy to collide with the lattice and generate a conduction electron + valence hole pair. These carriers have enough energy to repeat the process, causing the number of carriers to increase exponentially.





Zener breakdown occurs when the field is strong enough to cause an electron to tunnel through the barrier from the valence to the conduction band. This typically occurs at higher voltage than avalanche.

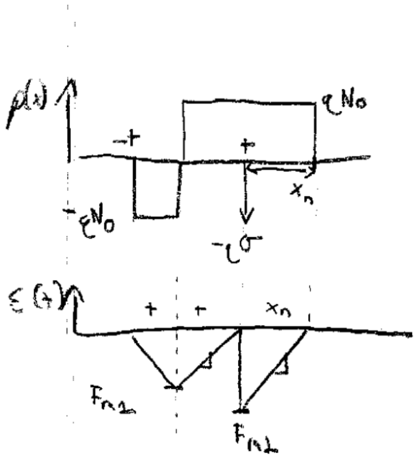
Problem 2 (20 Points): Diagnosing pn junction Diodes

Two p-n junction diodes A and B are fabricated on a semiconductor wafer. The semiconductor has an intrinsic carrier density n_i. The intentional doping in both n- and p-regions of the p-n junctions equal $N_A=N_D=N_0$. However, during ion implantation for isolation of the two diodes, negatively charged ions of sheet density σ incorporate a distance t from the metallurgical junction region in the *n-type side* of diode B. No such ions enter diode A. Neglect Gummel correction.

a) Express the total depletion region thickness W in diode A in terms of n_i, N_0, and the Debye length L_D in the intentionally doped regions of the semiconductors. The Debye length in a doped region is given by $L_D = \sqrt{\varepsilon_S kT / q^2 N}$, where N is the doping.

b) Assume that the extra incorporated ions in diode B are inside the n-type depletion region of B. From two known facts, you will find the two unknowns - the sheet doping density σ, and the thickness t.
First fact: The electric field drops to ZERO on the junction side of the plane of the sheet charge in diode B.
Second fact: The zero-bias junction capacitances of diodes A and B are exactly the same.

Find σ in terms of N_0 and W, and t in terms of W. Draw the charge-field-band diagrams as you go along (you can't solve the problem without them!).



Charge Neutrality:

$$qN_0 t + q\sigma = qN_0 (t + x_n)$$

If $t = x_n = \frac{1}{3}W$ and $\sigma = \frac{1}{2} N_0 \cdot W$

$$qN_0 \cdot \frac{W}{3} + qN_0 \cdot \frac{W}{2} = qN_0 \left(\frac{W}{3} + \frac{W}{3}\right)$$

$$\frac{W}{3} + \frac{W}{2} \neq \frac{2W}{3}$$

– Solution Violates Charge Neutrality

$L_D = \sqrt{\frac{\epsilon_s kT}{q^2 N_0}}$ Diode A: $W = \left[\frac{2\epsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_0}\right)\left(kT \ln\left(\frac{N_A N_0}{n_i^2}\right)\right)\right]^{1/2} = 2L_D \cdot \sqrt{\ln\left(\frac{N_0^2}{n_i^2}\right)}$

Diode B:

Given $\mathcal{E}(x)$ goes to zero on junction side of σ

$$C_A = C_B \qquad \frac{\epsilon_s}{W_A} = \frac{\epsilon_s}{W_B} \quad \therefore \quad W_A = W_B$$

So:

$$2t + x_n = W_A = 2L_D \sqrt{\ln\left(\frac{N_0^2}{n_i^2}\right)}$$

From charge Neutrality:

$$\sigma = N_0 x_n$$

Built in Voltage:

$$F_{m1} = q\frac{N_0 t}{\epsilon_s} \qquad F_{m2} = \frac{q N_0 x_n}{\epsilon_s} = \frac{q\sigma}{\epsilon_s}$$

$$V_{bi,B} = \frac{1}{2}F_{m1} \cdot t + \frac{1}{2}F_{m1} t + \frac{1}{2}F_{m2} \cdot x_n$$

$$= \frac{1}{\epsilon_s}\left[qN_0 t^2 + \frac{1}{2} qN_0 x_n^2\right]$$

If the two built in voltages are equal:

$$\frac{kT}{q}\ln\left(\frac{N_0^2}{n_i^2}\right) = \frac{qN_0 t^2}{\epsilon_s} + \frac{1}{2}\frac{N_0 x_n^2}{\epsilon_s}$$

$$\frac{\epsilon_s kT}{q^2 N_0}\ln\left(\frac{N_0^2}{n_i^2}\right) = t^2 + \frac{1}{2}x_n^2$$

$$\frac{1}{4}W_A^2 = t^2 + \frac{1}{2}(W_A - 2t)^2$$

$$\frac{1}{4}W_A^2 = t^2 + \frac{1}{2}W_A^2 - 2t \cdot W_A + 2t^2$$

$$0 = 3t^2 - 2t \cdot W_A + \frac{1}{4}W_A^2$$

$$t = W/2 \text{ or } t = W/6$$

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if $t = W/2$ $\sigma = 0$, Diode A case

If $t = \frac{W}{6}$:

$$W = 2t + x_n \quad \text{so} \quad x_n = \frac{2}{3}W$$

$$\sigma = N_0 x_n = \frac{2}{3} N_0 \cdot W$$

Checking Charge Nuetrality:

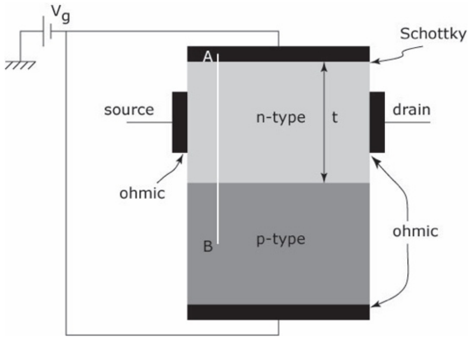
$$qN_0 t + q\sigma = qN_0(t + x_n)$$

$$qN_0\left(\frac{W}{6}\right) + q\left(\frac{2}{3}N_0 W\right) = qN_0\left(\frac{W}{6} + \frac{2}{3}W\right)$$

$$\frac{W}{6} + \frac{2}{3}W = \frac{W}{6} + \frac{2}{3}W$$

Charge Nuetrality Satisfied.

Problem 3 (20 Points): A "MESJFET"

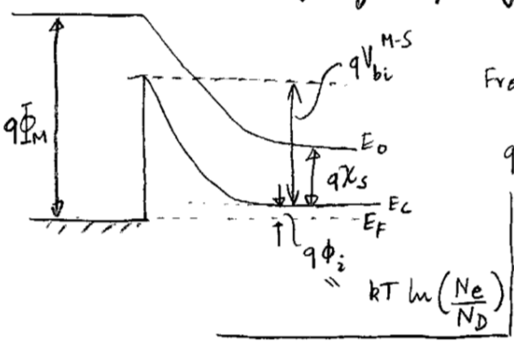


The figure on the left shows a device that needs to be analyzed for a certain application. The design part assigned to you will only require your knowledge of metal-semiconductor and p-n junctions. Here's what is required: the device should operate as a transistor. The current flow between the source and drain ohmic contacts has to be modulated by the gate voltage, V_g. Your main task is to find the gate voltage at which no current can flow in the n-type layer. The *same* gate voltage is applied to both the metal - n-type semiconductor Schottky junction, as well as the metal – p-type semiconductor ohmic contact (as shown in the figure). Neglect Gummel correction for this problem. The following are given –

1- Semiconductor electron affinity: $q\chi_S$, intrinsic carrier density: n_i, Dielectric constant: ε_S
2 - Doping densities: N_D & N_A, such that $N_A >> N_D$ (use this to your advantage), and
3 - The thickness of the n-type layer: t.
4 - The n-layer is conductive between the source-drain contacts when V_g=0.

a) Find the work function $q\Phi_M$ of the Schottky metal such that the 'built-in' voltage of the Schottky junction is *exactly the same* as the built-in voltage of p-n junction. Choose this to be your metal work function for the rest of the problem.
b) Find the thickness of the <u>conductive</u> region in the n-type layer at zero gate bias. Do so by sketching the charge-field-band diagram along the line A-B for the case when V_g=0, and taking it from there. What can you say about the thickness t from given conditions 3 & 4 above?
c) It is specified that the horizontal current between the source-drain contacts should be zero at a certain gate voltage, called the pinch-off voltage. This can happen only if the n-type layer is completely depleted of free carriers. Find the pinch-off gate voltage. Is it positive or negative?
d) Why the strange name – 'MESJFET' (other than that this device has been invented for this exam)?

(a) Built-in voltage of the p-n junction: $\boxed{V_{bi}^{p-n} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)}$



From band-diagram on left,

$$qV_{bi}^{M\text{-}S} = q\Phi_M - q\chi_S - q\phi_i$$

$$= q\Phi_M - q\chi_S - kT\ln\left(\frac{N_C}{N_D}\right)$$

$$= qV_{bi}^{p-n} \quad \text{(Required)}.$$

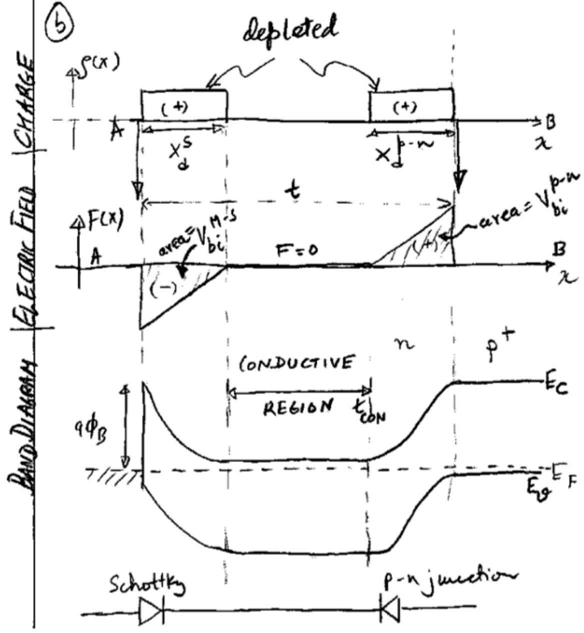
∴ The necessary work function is

$$q\Phi_M = qV_{bi}^{p-n} + kT\ln\left(\frac{N_C}{N_D}\right) + q\chi_S$$

$$= kT\ln\left(\frac{N_A N_D}{n_i^2}\right) + kT\ln\left(\frac{N_C}{N_D}\right) + q\chi_S$$

$$\boxed{q\Phi_M = q\chi_S + kT\ln\left(\frac{N_A N_C}{n_i^2}\right)}$$

(b)



From the figure on left, the depletion widths of the M-S & p-n junctions are the SAME, since the voltage drops across them are the same!

$\therefore$ $x_d^S = x_d^{p-n}$, where

$$V_{bi} = \frac{qN_D x_d^2}{2\epsilon_s} \quad @ \; V_g = 0.$$

$$\therefore \; x_d^S = x_d^{p-n} = \sqrt{\frac{2\epsilon_s V_{bi}}{qN_D}}$$

& The conductive region thickness is

$$\boxed{t_{CON} = t - 2x_d^S = t - 2\sqrt{\frac{2\epsilon_s V_{bi}}{qN_D}}}$$

Obviously, $\boxed{t^2 \geq \frac{8\epsilon_s V_{bi}}{qN_D}}$

Contd...

(c) Since the Schottky contact to n-layer & the ohmic contact to the p-layer are at the same potential,

$\boxed{+ve\ V_g} \Rightarrow$ Depletion Layer thicknesses x_d^S & x_d^{p-n} shrink, n-layer more conductive.

$\boxed{-ve\ V_g} \Rightarrow$ Depletion layer thicknesses x_d^S & x_d^{p-n} stretch, n-layer less conductive.

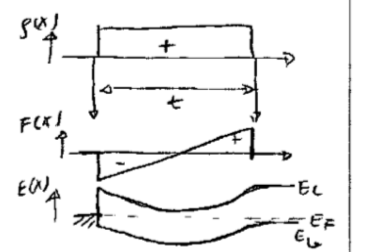
It is clear that a $-ve\ V_g$ is needed to deplete the n-layer

When a bias is applied,

$$x_d^S = \sqrt{\frac{2\epsilon_s (V_{bi} + |V_g|)}{qN_D}} \qquad x_d^{p-n} \approx \sqrt{\frac{2\epsilon_s (V_{bi} + |V_g|)}{qN_D}}$$

$$\therefore \quad t_{CON} = t - \left\{ \sqrt{\frac{2\epsilon_s (V_{bi} + |V_g|)}{qN_D}} + \sqrt{\frac{2\epsilon_s (V_{bi} + |V_g|)}{qN_D}} \right\}$$

$\left(\frac{1}{N_A} + \frac{1}{N_D}\right) \approx \frac{1}{N_D}$ since $N_A \gg N_D$

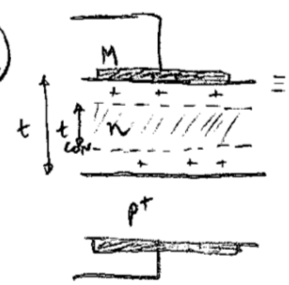


@ pinch-off, $\boxed{t_{CON} = 0} \Rightarrow$

$$t = 2\sqrt{\frac{2\epsilon_s (V_{bi} + |V_g|)}{qN_D}}$$

$$\Rightarrow \quad \boxed{V_g(\text{pinch-off}) = \frac{qN_D}{8\epsilon_s} t^2 - V_{bi}}$$

(d)

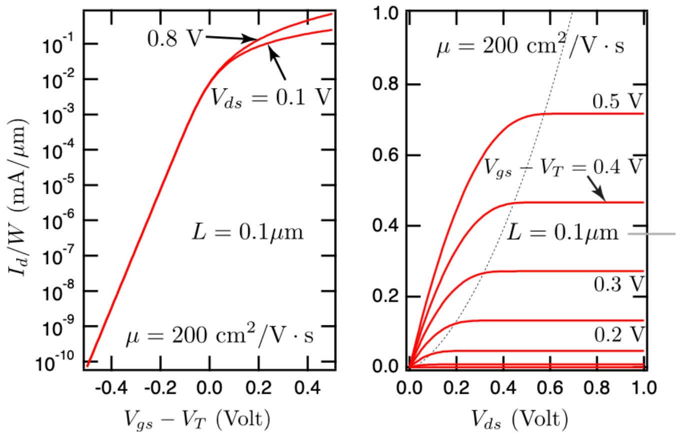


$\equiv$ MES FET — METAL-SEMICONDUCTOR

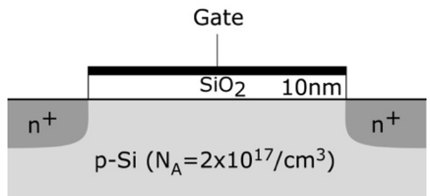
J FET — JUNCTION

MESJ FET — FIELD-EFFECT TRANSISTOR

The output and transfer characteristics are similar to a generic FET like the one shown below.



Problem 4 (40 Points): MOSFET Design



Consider the MOSFET shown above. Assume a gate metal with a work function of 4.5eV, the n+ regions are degenerately doped (N_D=N_c), and that there are no charges in the oxide layer. Use the following material parameters for your calculations. Remember to draw relevant sketches.

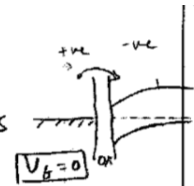
Si: $n_i(300K) = 10^{10}/cm^3$, $q\chi_{Si}$=4.05eV, $\varepsilon_S=12\varepsilon_0$, E_g=1.1eV, μ_n=200 cm^2/V.s
SiO_2: $q\chi_{ox}$=0.95eV, E_g=8.0eV, $\varepsilon_S=4\varepsilon_0$

a) Calculate the threshold voltage V_T at 300K by drawing the energy band diagram.
b) *Comment* how V_T would change if the temperature is lowered to 77K (do not calculate!).
c) Sketch the low- and high-frequency C-V curves if the voltage is applied between the metal gate, and to an ohmic contact to the p-substrate. Label everything of importance (capacitance values, V_{FB}, V_{th}), and explain.
d) Calculate the current per device width for a gate length of L=0.5 micron at bias conditions of V_{ds}=0.5 V and V_{gs}-V_T=1 V. Is the device in the linear or saturation regime?
e) Calculate the saturation current per device width at V_{gs}-V_T=1 V for a gate length of L=0.5 micron.
f) If I scale the FET gate length to below L~10 nm, I approach the ballistic limit of the FET. Estimate the ballistic saturation current at V_{gs}-V_T = 0.3 V in this limit.
g) Now if I want a high-voltage FET, I must increase the gate length. When V_{gs} = V_{FB}, I want to prevent *drain-source punchthrough* for V_{ds}=100 Volt. Find the gate length so that I am safe. Make reasonable approximations, and assume that the gate oxide can sustain very large fields.
h) Does the device at such gate lengths suffer from short-channel effects?

PROBLEM 3

(a) To calculate V_{Th}, first get V_{FB} -

$\phi_M < \phi_S$



$$V_{FB} = q(\phi_M - \phi_S) = q[\overbrace{\phi_M}^{4.5eV} - \overbrace{(q\chi_{Si} + \underbrace{E_c - E_F}))}^{5.04eV}]$$

$$\boxed{V_{FB} = -0.54\,eV}$$

negative!

$$\underbrace{(E_c - E_i)}_{\approx \frac{E_g}{2} \approx 0.55eV} + \underbrace{(E_i - E_F)}_{q\psi_B = kT\ln\left(\frac{N_A}{n_i}\right) = 0.44\,eV}$$

If V_{FB} was zero, the threshold voltage would be -

$$V_{TH}^0 = 2\psi_B + \frac{\sqrt{2q\epsilon_s N_A (2\psi_B)}}{C_{ox}}$$

$$= 2(0.44) + 0.98 = 1.86 \text{ Volt}$$

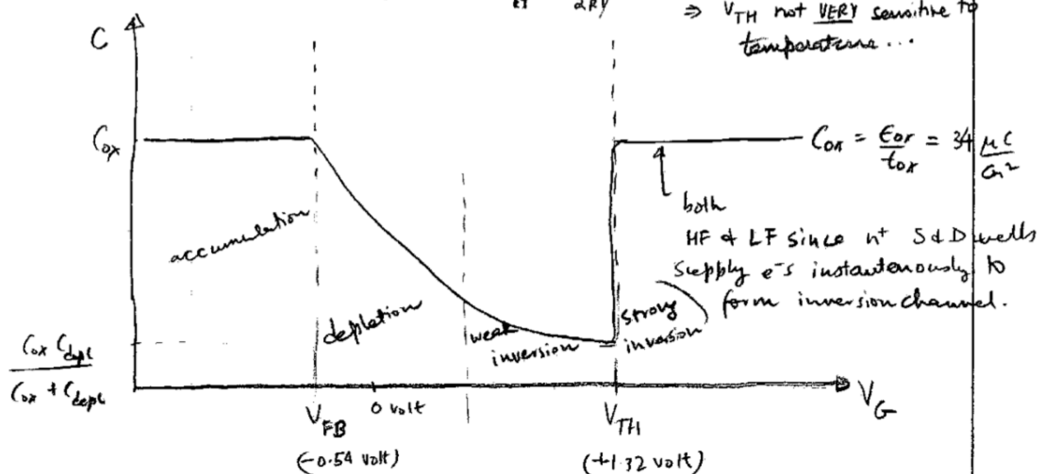
Since there is already band bending @ $V_G = 0$, the threshold voltage taking the flat-band voltage into account,

$$V_{TH} = V_{TH}^0 - |V_{FB}| = 1.86 - 0.54$$

$$\boxed{V_{TH} = 1.32 \text{ Volt}}$$

(b) Depends strongly on $\psi_B = kT\ln\left(\frac{N_A}{n_i}\right) \approx kT\left(\frac{-E_D}{kT} + \frac{E_g}{2kT}\right) \propto T^0$ to first order.
$\Rightarrow V_{TH}$ not VERY sensitive to temperature...

(c)

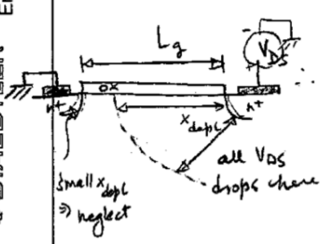


Prob 3, contd - - -

(d) Most of V_{DS} drops in the reverse-biased Drain-channel n^+-p junction, on the p-side.

∴ If the gate length is larger than L_g^{min}, where

$$\frac{qN_A(L_g^{min})^2}{2\epsilon_s} \simeq V_{DS} = 100 \text{ Volt},$$ I should be safe.



$$\therefore\ L_g^{min} \simeq \sqrt{\frac{2\epsilon_s V_{DS}}{qN_A}} \simeq 800\ nm \simeq 0.8\ \mu m$$

∴ $\boxed{L_g > 1\ \mu m}$ should do the job

(e) No, this is a long-channel MOSFET, since

$$F_{vertical} \sim \frac{V_{GS}}{t_{ox}} \qquad F_{horizontal} \sim \frac{V_{DS}}{L_g}$$

$$\text{long-channel} \Rightarrow F_{horizontal} << F_{vertical}$$

$$\frac{V_{DS}}{L_g} << \frac{V_{GS}}{t_{ox}}$$

$$\left(\frac{V_{DS}}{V_{GS}}\right) << \frac{L_g}{t_{ox}}$$

Under normal operation, $\frac{L_g}{t_{ox}} = \frac{1000\,nm}{10\,nm} = 100$

$\frac{V_{DS}}{V_{GS}} \approx 1$ ∴ $1 << 100$ is satisfied.

Parts d and e (from Kathleen Smith)

d) $\frac{I_D}{W} = \frac{\mu_n C_{ox}}{L}\left[\left[V_G - V_T - \frac{1}{2}V_D\right]V_D\right]$

5/5 $V_{ds} < V_{GS} - V_T \Rightarrow$ the device is in the $\boxed{\text{linear regime}}$

$V_D = 0.5\text{ V},\ V_{GS} - V_T = 1\text{ V},\ L = 0.5\ \mu m$

$\boxed{\frac{I_D}{W} = 0.531 \frac{A}{cm} = 0.0531 \frac{mA}{\mu m}}$

e) $\frac{I_{D,sat}}{W} = \frac{\mu_n C_{ox}}{2L}(V_G - V_T)^2 = 0.708 \frac{A}{cm}$

3/3

$\boxed{I_{D,sat} = 0.71 \frac{A}{cm} = 0.071 \frac{mA}{\mu m}}$

Parts f and g:
From class notes:

$$e^{\eta_s} \approx e^{\frac{V_{gs}-V_T}{V_{th}}} \cdot \frac{1}{1+e^{-v_d}} \implies \boxed{\frac{I_d}{W}|_{off} \approx J_0^{2d} \cdot e^{\frac{V_{gs}-V_T}{V_{th}}} \cdot 2\tanh\left[\frac{V_{ds}}{2V_{th}}\right]}. \quad (18.6)$$

On-State: For gate voltages $V_{gs} - V_T >> V_{th}$, the FET is in the **on-state**. The ballistic current in this limit is[14]

$$\boxed{\frac{I_d}{W}|_{on} \approx J_0^{2d} \cdot \left[\frac{\eta_s^{\frac{3}{2}}}{\Gamma(2+\frac{1}{2})}\right] \approx J_0^{2d} \cdot \frac{4}{3\sqrt{\pi}} \cdot \left(\frac{2C_g(V_{gs}-V_T)}{qn_q}\right)^{\frac{3}{2}}}$$

$$\implies \frac{I_d}{W}|_{on} \approx \frac{16}{3} \cdot \frac{qg_s g_v \sqrt{m_c^\star}}{h^2} \cdot \left[\frac{q(V_{gs}-V_T)}{1+\frac{q^2 \cdot \frac{g_s g_v m_c^\star}{2\pi\hbar^2}}{\frac{\epsilon_b}{t_b}}}\right]^{\frac{3}{2}}. \quad (18.7)$$

Use band parameters to get C_b=0.355 uF/cm and C_q=27 uF/cm^2, implying $C_q >> C_b$. Since the on-state saturation current per unit width depends on the total capacitance as $1/C_{tot} = 1/C_q + 1/C_b$, the quantum capacitance may be neglected ONLY in the on-state. Using the provided values of Silicon band parameters, and the MOSFET barrier dimensions, we obtain the currents at the appropriate bias voltages from the above equations as
I_{on}=0.08 mA/um, I_{off}=0.000036 mA/um, and I_{on}/I_{off} ~2247.