Current-carrying Capacity of Long & Short Channel 2D Graphene Transistors

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Introduction: Recently, it has been shown that charge carriers in atomically thin single-layer 2-dimensional graphene sheets can exhibit high electron (or hole) mobilities, long mean free paths, and very good electrostatic confinement of carriers[1]. Most of these properties stem from the inherent 2D nature of the crystal, and the unique conical zero-gap bandstructure that results from the sp^2-hybridized bonds. In spite of rapid advances in the field, not much interest has been directed towards understanding the high-field transport properties (saturation currents) in graphene. Since graphene sheets and nano-ribbons[2] (GNRs) are being touted as attractive replacements for carbon nanotubes (CNTs) for transistor applications[3], it is worthwhile investigating the high-field current-carrying capacity of these materials.

Device Fabrication: For studying high-field properties of graphene transistors, we have used single-layer exfoliated graphene sheets. The single-layer nature has been established using optical contrast analysis[4] as shown in Fig 1. These graphene sheets are located on t_{ox}=300 nm thick SiO_2/ conductive Si substrates (Fig 2), which act as the back-gate. Optical (Fig 3) and Electron-Beam Lithography (Fig 4) was used to write source-drain contacts for long and short channel graphene FETs respectively. RIE based O_2-plasma etch (in an Ar/O_2 mixture) was used to etch away the unwanted graphene regions for finalizing the FET structures.

Measurements: The transistor characteristics were measured for these devices as a function of the gate bias (V_{gs}) at 300 K (Fig 5), and the gate voltage V_{dp} corresponding to the Fermi level at the Dirac point (minimum conductivity point) was identified (Fig 6). Thereafter high drain biases were gradually applied and the current densities were observed to increase up to 1.2 A/mm for a 50 nm long channel graphene FET (Fig 7), which at the least puts graphene in the same bracket as traditional FETs in terms of current-carrying capacity. Figs 5-7 show the characteristics of a 50 nm channel length transistor. When the same measurements were repeated for a long-channel (~8 μm) device, the high-bias currents were found to be much lower (Fig 8), consistent with the scaling trend for traditional FETs and HEMTs. Another interesting effect that was observed for a ~2 μm channel length device was an effective current-induced "annealing" of the graphene: for drain biases lower than 4 V, the current reached ~ 0.2 A/mm and good gate modulation was observed (Fig 9). However, as the drain bias was increased, the maximum current abruptly jumped to ~0.6 A/mm, and stayed there till eventual burnout (Fig 10) after repeated fast sweeps. This indicates that most likely charged impurities from the surface of the exposed graphene are expelled by very high heat, and current-induced annealing can be used for improving the characteristics of graphene FETs.

Modeling: We have used a simple model for determining the fundamental current carrying capacity of 2D graphene sheets. The model builds on the seminal finding[5] that the saturation current in the diffusive limit in CNTs is determined by zone-boundary optical-phonon back-scattering of carriers. We have derived the corresponding result[5] for the 2D graphene case by using the 2D conical bandstructure and placing the restriction that the highest occupied state and the lowest unoccupied state are separated by the LO phonon energy (Fig 11). The maximum current-carrying capacity of 2D graphene sheets based on this theory is plotted in Fig 12. As might be expected, the current carrying capacity is strongly dependent on the location of the Fermi level with respect to the Dirac point. The interesting finding is that even when E_F is at the Dirac point, graphene can carry ~0.5 A/mm of saturation current, and current densities in the 1 – 4 A/mm range are easily achievable if the heat generated can be effectively coupled out. In Fig 13, we plot the maximum current densities we have observed as a function of the 2D carrier density along with the theoretical ceiling of the saturation currents. It is evident that our devices are currently a factor of 2-3 below the maximum current carrying capacity of graphene sheets.

Conclusions: The fundamental current-carrying capacity of graphene is found to be much higher than tradiational FETs (MOSFETs, pHEMTs, etc), matched only by the III-V nitride HEMTs. Currently, the device structures investigated are rather primitive and do not allow for efficient heat removal – similar effects were observed for CNTs a decade ago. However, with top-gate technology (for high 2D carrier densities with smaller gate voltages), efficient heat removal (to prevent burnout), and improvement of the purity levels of the gate dielectrics (to achieve current saturation at lower biases and thus less heat due to $I_{ds}xV_{ds}$ product lowering), 2D graphene and GNR based FETs can be expected to surpass most traditional (non-nitride) FETs in their current-carrying capacity.

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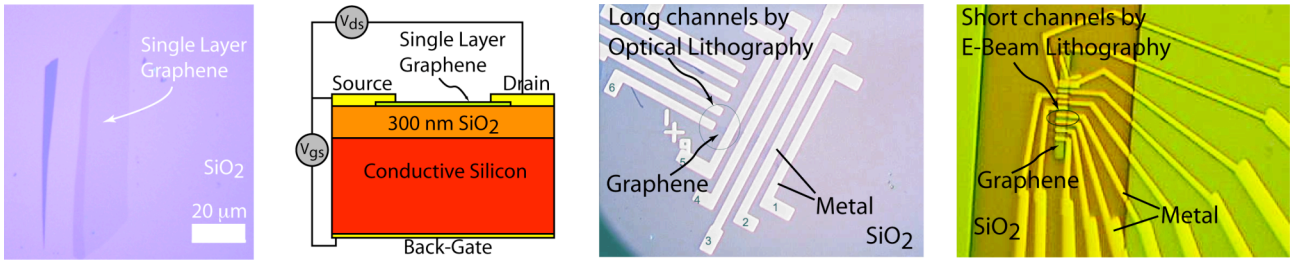
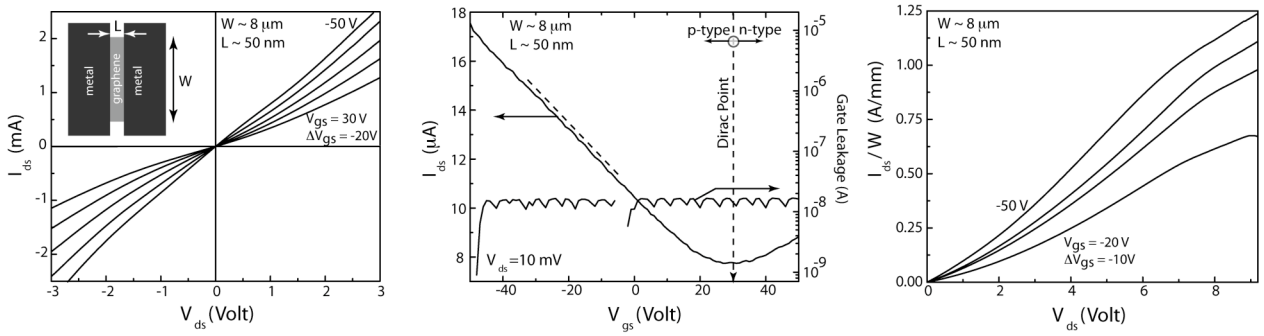
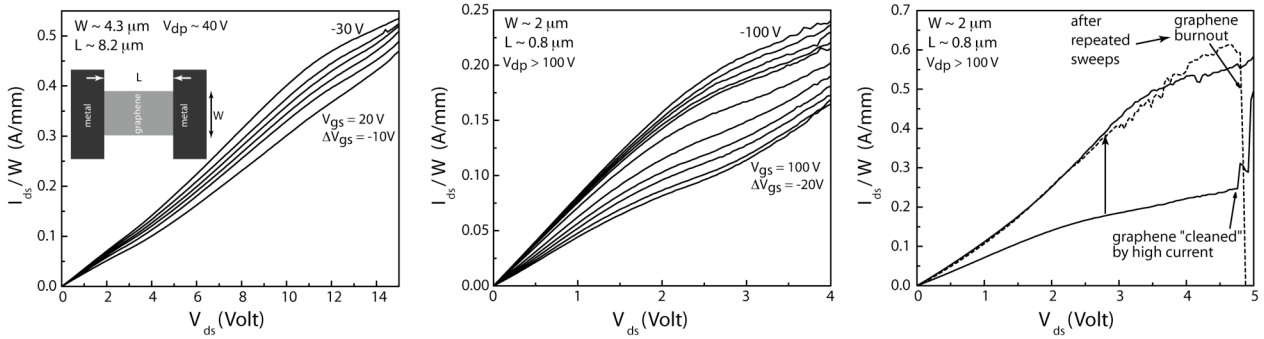


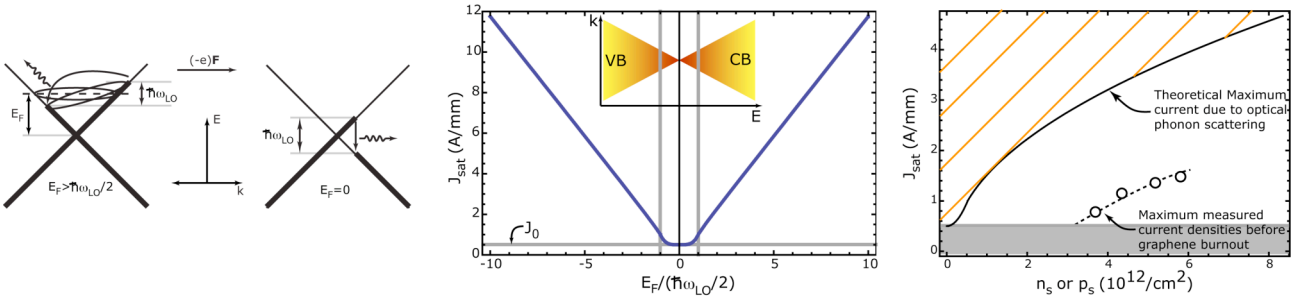
Figures 1, 2, 3, 4: Monolayer Graphene (1), FET structure (2), Optical (3) and EBL defined source-drain contacts (4). Exfoliated monolayer graphene was identified by optical contrast, and configured as shown in the figures for the measurement of high-field effects in the long- and short-channel 2D graphene transistors.



Figures 5, 6, 7: A short-channel (L ~ 50 nm) 2D graphene FET characteristics at 300 K. Clear gate modulation is observed, and current densities more than 1 A/mm are measured. The Dirac point is at V_{dp}~30 V, implying that at zero gate bias, the Fermi level is in the valence band of graphene.



Figures 8, 9, 10: As the channel length is increased, the current density drops: for a ~ 8 μm long channel (8), the current densities are ~ 0.5 A/mm before burnout at high drain biases. For a ~ 2 μm long channel (9), strong modulation was observed but at low currents; however, possible expulsion of charged impurities from the graphene surface due to heat led to an increase in current (10) before subsequent device burnout after repeated high bias sweeps.



Figures 11, 12, 13: By using zone-boundary phonon (160 meV) scattering and considering the 2D k-space (11), we have derived the theoretical limits of saturation current in graphene (12), which is found to be strongly dependent on the location of the Fermi level w.r.t. the Dirac point. Comparison of the highest experimental current densities measured here show that our devices (13) are still limited by heating and burnout; we are a factor of 2-3 below the theoretical limit in the current carrying capacity of single layer graphene sheets.