AlN/GaN Insulated-Gate HEMTs With 2.3 A/mm Output Current and 480 mS/mm Transconductance

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***Abstract*—High-electron mobility transistors (HEMTs) based on ultrathin AlN/GaN heterostructures with a 3.5-nm AlN barrier and a 3-nm Al_2O_3 gate dielectric have been investigated. Owing to the optimized AlN/GaN interface, very high carrier mobility ($\sim$1400 $cm^2/V \cdot s$) and high 2-D electron-gas density ($\sim 2.7 \times 10^{13}/cm^2$) resulted in a record low sheet resistance ($\sim$165 Ω/sq). The resultant HEMTs showed a maximum dc output current density of $\sim$2.3 A/mm and a peak extrinsic transconductance $g_{m,\mathrm{ext}} \sim 480$ mS/mm (corresponding to $g_{m,\mathrm{int}} \sim 1$ S/mm). An $f_T/f_{\max}$ of 52/60 GHz was measured on 0.25×60 μm^2 gate HEMTs. With further improvements of the ohmic contacts, the gate dielectric, and the lowering of the buffer leakage, the presented results suggest that, by using AlN/GaN heterojunctions, it may be possible to push the performance of nitride HEMTs to current, power, and speed levels that are currently unachievable in AlGaN/GaN technology.**

***Index Terms*—AlN, GaN, high-electron mobility transistors (HEMTs), insulated gate.**

I. Introduction

IN ORDER to achieve high-speed high-power transistors, it is important to do the following: 1) increase the device output current; 2) downscale the device geometry to reduce the carrier transit time; and 3) simultaneously maximize the breakdown voltage, which can be optimized by engineering the electric field near the gate on the drain side in field-effect transistors (FETs). This paradigm has been successfully applied to FETs made of all conventional semiconductors, in which the most recent is AlGaN/GaN-based FET technology. Various techniques have been developed to boost the RF performance of these FETs—for example, recessed gates [1], slanted recessed gates [2], insulated gates employing either F treatment [3] or dielectrics [4], AlInN barriers [5], InGaN [6] and AlGaN back barriers [7], ion implantation for ohmic contacts [8] and device isolation [9] etc. The device output current is normally limited by the carrier sheet density and carrier injection velocity at the source end. Therefore, a high carrier density, along with high carrier mobility, is desired. Based on these considerations, ultrathin AlN/GaN heterojunction-based high-electron mobility transistors (HEMTs) present themselves as attractive candidates for exploring the high-speed high-power limits of III–V nitride FET technologies, owing to their extremely high charge densities, high mobilities, and the intrinsic ultrascaled geometry.

The fundamental upper limit of the polarization-induced 2-D electron-gas (2DEG) density at Al(Ga)N/GaN heterojunctions is $\sim 6 \times 10^{13}/cm^2$, which is achievable only in all-binary AlN/GaN heterojunctions [10]. This density results due to the maximum possible spontaneous and piezoelectric polarization difference between the AlN epitaxial layer and the GaN layer underneath [11]. Recently, we demonstrated that these carrier densities could be achieved in ultrathin ($\sim$2–6 nm) AlN/GaN heterojunctions grown by molecular beam epitaxy [10]. At very high 2DEG densities, the 2DEG mobility was found to degrade due to strain relaxation. However, a high-mobility window was observed, within which a high 2DEG density ($2-4 \times 10^{13}/cm^2$) and a high mobility ($\sim 1000 - 1600$ $cm^2/V \cdot s$) are combined to produce the lowest room temperature (RT) sheet resistances ($\sim 150-170$ Ω/sq) reported to date in nitride HEMTs [12]. Recently, impressive speed ($f_t/f_{\max} = 107/171$ GHz) has been demonstrated, employing comparatively low-mobility ultrathin AlN/GaN heterostructures with a 2.5-nm AlN barrier and a 2-nm SiN_x gate dielectric ($2.33 \times 10^{13}/cm^2$ and 235 $cm^2/V \cdot s$; thus, a sheet resistance of $\sim$1140 Ω/sq) [13], and an impressive high current performance ($I_{\max} = 2.3$ A/mm) has been achieved in high-mobility AlInN/AlN/GaN HEMTs ($2.5 \times 10^{13}/cm^2$ and 1170 $cm^2/V \cdot s$; thus, a sheet resistance of $\sim$210 Ω/sq) [14]. Therefore, high-mobility AlN/GaN HEMTs offer a route to combine these advantages in speed, current, and transconductance in a single structure. In this letter, HEMTs fabricated from record low sheet resistance AlN/GaN heterostructures are reported. These HEMTs attain very high dc current densities ($\sim$2.3 A/mm) and extrinsic transconductances ($\sim$480 mS/mm) and provide a glimpse into the performance limits of III–V nitride HEMT technology.

II. Experiments

Ultrathin epitaxial AlN/GaN heterojunctions were grown on semi-insulating GaN-on-sapphire substrates in a Veeco Gen 930 plasma-assisted molecular beam epitaxy system. A 200-nm-thick unintentionally doped (UID) GaN buffer layer was first grown and capped with a 3.5-nm pseudomorphic UID AlN barrier. This structure resulted in a 2DEG density of $2.75 \times 10^{13}/cm^2$ and an RT mobility of 1367 $cm^2/V \cdot s$, leading to a sheet resistance of $\sim$166 Ω/sq at RT. A detailed transport study showed that the record low sheet resistance is a result of the reduction of interface roughness at the AlN/GaN heterojunction upon growth optimization [12]. A device isolation mesa of

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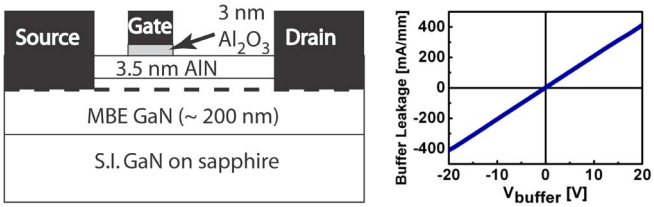

Fig. 1. (a) Schematic of the insulated-gate AlN/GaN HEMT structure. (b) Buffer I–V curve with the 2DEG channel removed.

~120-nm depth was fabricated by using BCl_3/Cl_2-based reactive ion etching. Ti/Al/Ni/Au metal stacks were then deposited and annealed to obtain ohmic contacts with a source–drain separation of 2.5 μm. Electron-beam lithography was used to define 250-nm-long gates with a source–gate distance L_{SG} of 0.4 μm. A 3-nm aluminum oxide gate dielectric was deposited by using electron-beam evaporation, which is followed by a Ni/Au gate metal layer. The devices were not passivated. An insulating gate dielectric was found to be necessary to prevent gate leakage, because our prior investigations of planar Schottky diodes revealed that a large portion of the gate leakage current on these untreated heterostructures stems from the leakage through a high density of dislocations ($\sim 10^9/\text{cm}^2$) [15]. The transmission line method measurement on 100-μm-wide pads yielded a contact resistance of ~1.1 $\Omega \cdot$ mm and a sheet resistance of ~171 Ω/sq, which is in close agreement with the Hall effect measurement. The ohmic contact formation techniques on ultrathin AlN/GaN heterostructures have been reported elsewhere [16]. The schematic device structure is shown in Fig. 1(a).

III. Results and Discussion

The dc current–voltage characteristics of the HEMTs were measured by using an Agilent 4156C semiconductor parameter analyzer, and the small signal radio frequency characteristics were investigated by using an Agilent 8722D network analyzer. Under dc conditions, a maximum current density of 2.3 A/mm was measured for a 12.5-μm-gate-width device, as shown in Fig. 2(a). The corresponding transfer characteristic of this device is shown in Fig. 2(b). In the vicinity of $V_{DS} = 4.2$ V, a peak extrinsic transconductance of 480 mS/mm is extracted. Considering a contact resistance of 1.1 $\Omega \cdot$ mm and a source resistance of 0.066 $\Omega \cdot$ mm ($L_{SG} = 0.4$ μm), the calculated intrinsic transconductance is as high as ~1 S/mm. This performance shows that both high current density and transconductance can be achieved in a single AlN/GaN HEMT with insulated gates. For comparison, in earlier papers, the highest dc current densities have been reported in AlInN/AlN/GaN HEMTs (2.3 A/mm) [14], whereas the highest transconductances have been reported in deep-recessed AlGaN/GaN HEMTs (635 mS/mm) [17].

The device pinchoff is found to be dominated by the leakage through the buffer. For instance, at $V_{DS} = 8.5$ V and $V_{GS} = -10$ V, a drain current of 60 mA/mm was measured. This introduces uncertainty in extracting the pinchoff voltage as well as the device breakdown voltage. When the 2DEG channel

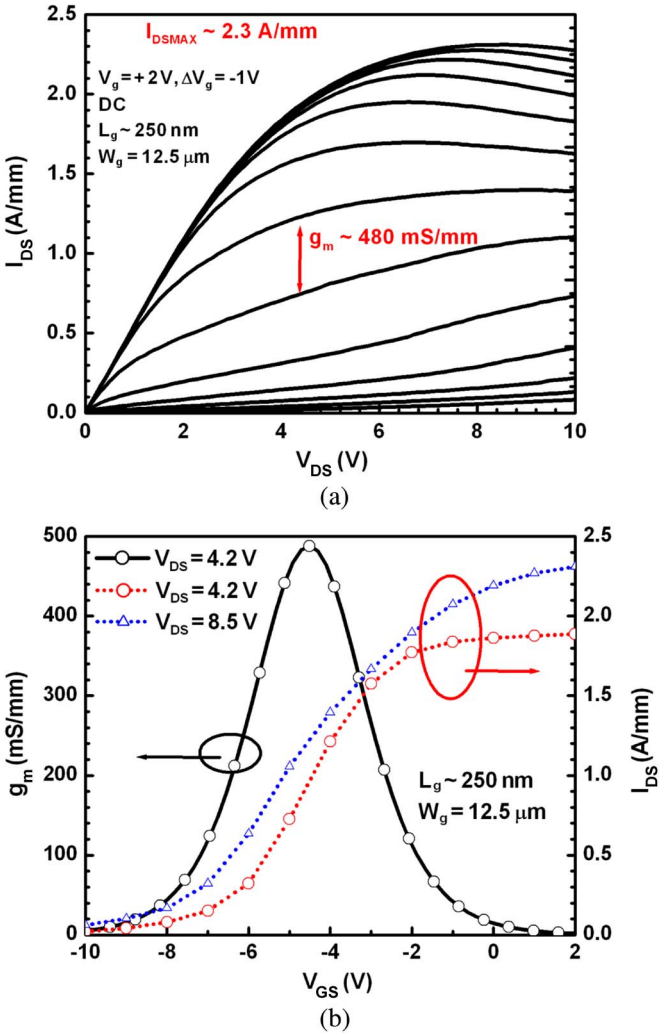

Fig. 2. (a) DC I–V curves showing a record high maximum drain–source current of ~2.3 A/mm. (b) Corresponding transfer curve showing a peak extrinsic transconductance of ~480 mS/mm.

was removed by a shallow etch, the measured buffer I–V is shown in Fig. 1(b), exhibiting ~170 mA/mm at 8.5 V. With a deeper etch, when the regrowth interface was removed, this current level decreased by more than six orders of magnitude (not shown). The leaky current path at the regrowth interface situated at ~200 nm below the surface is also confirmed by C–V measurement of test structures with thicker gate insulator. Because the gate probe pad is in contact with the leaky buffer, the actual gate leakage through the gate dielectric cannot be determined accurately, but the gate current (including buffer leakage) is approximately one to two orders of magnitude smaller than the drain current for -5 V $\leq V_{GS} \leq 2$ V. Thus, the observed high maximum output current indeed results from the 2DEG channel. The hard breakdowns of these HEMTs were also tested to be > 20 V. The devices were also characterized by using a cold pulsed I–V scheme ($V_{DS0} = 0$ V and $V_{GS0} = 0$ V) with long pulses (500 μs). Fig. 3 shows the comparison of the dc and pulsed I–V curves. At intermediate current levels, the pulsed I–Vs show a slightly higher current than the dc measurements at low drain bias but a lower current

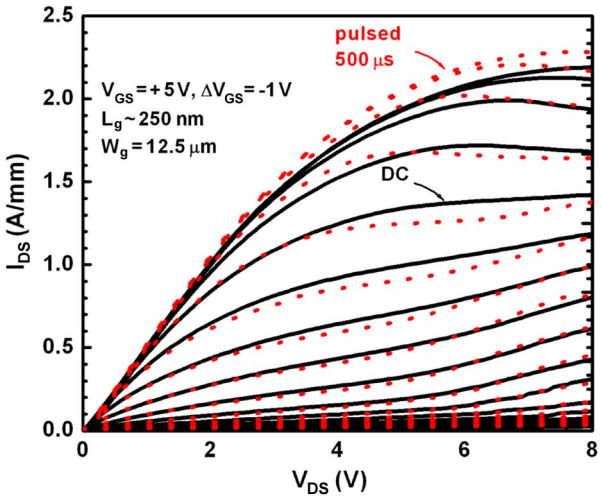

Fig. 3. Pulsed I–V measurements with relatively long pulses (500 μs, $V_{\mathrm{DS0}} = 0$ V, and $V_{\mathrm{GS0}} = 0$ V).

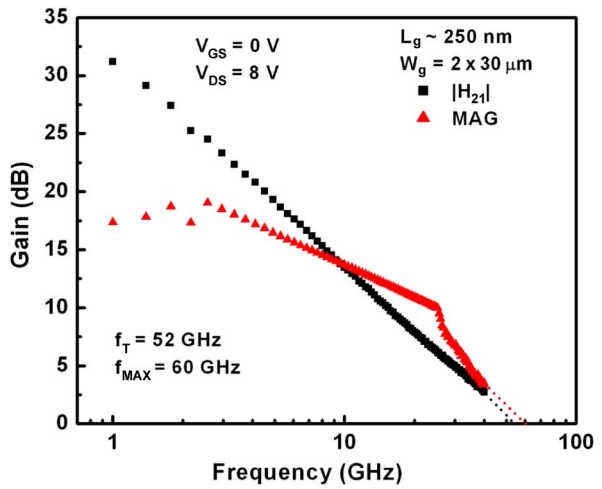

Fig. 4. RF performance of the 250-nm-gate-length HEMT showing $f_T = 52$ GHz and $f_{\max} = 60$ GHz, which is limited by contact resistance, leaky buffer, and traps.

at high drain bias when the channel is driven into depletion. We speculate that the observed dispersion may arise from the interplay between device self-heating during the measurement and trap states in the dielectric, dielectric/semiconductor interface, semiconductor surface, and/or bulk.

High-frequency characterization yielded the unity current gain cutoff frequency and power gain cutoff frequency $f_T/f_{\max}$ to be 52/60 GHz for a 0.25×60 μm^2 gate HEMT, as shown in Fig. 4. These values are lower than expected, given the observed high output current and transconductance. Further investigation revealed that it is primarily because the gate pads are directly located on the leaky buffer. Because these first-generation ultralow sheet resistance AlN/GaN heterostructures are optimized primarily for the AlN/GaN interface, the combined effects of buffer and gate leakage, traps, and relatively high contact resistance are issues that require further development. With further optimization of the material quality and processing techniques, particularly the ohmic contact and gate dielectric, significant improvement in device performance can be expected.

IV. Conclusion

HEMTs based on ultrathin AlN/GaN heterostructures with a 3.5-nm AlN barrier and a 3-nm Al_2O_3 gate dielectric have been investigated. Owing to the optimized AlN/GaN interface, very high carrier mobility ($\sim$1400 cm^2/V $\cdot$ s) and high 2DEG density ($\sim 2.7 \times 10^{13}$/cm^2) resulted in a record low sheet resistance ($\sim$165 Ω/sq). The resultant HEMTs showed a dc output current density of $\sim$2.3 A/mm, an extrinsic transconductance of $\sim$480 mS/mm, and an intrinsic transconductance of $\sim$1 S/mm. An $f_T/f_{\max}$ of 52/60 GHz was measured on 0.25×60 μm^2 gate HEMTs. The results indicate that these HEMTs are very promising to push the performance of GaN HEMTs into current, power, and speed levels that are currently unachievable in AlGaN/GaN technology. However, the minimization of the contact resistance and the reduction of gate and buffer leakages must be achieved to realize the unique potential of these novel heterostructures in high-speed high-power RF technologies of the future.

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