High Field Transport Properties of 2D and Nanoribbon Graphene FETs

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The unique electronic properties of graphene have ignited active research in the past few years. Though in theory its electronic structure and transport properties are well known the applicability as channel replacement material in conventional CMOS technology is still an open question. High mobility [1] and high current carrying capacity [2] makes graphene very attractive but on the other hand low I_{ON}/I_{OFF} ratio and the lack of sufficient saturation are yet unsolved drawbacks. In the past we were able to drive back-gated 2D graphene transistors to saturation regime [2]. Now we present the realization of these properties in double-gated graphene nanoribbon field effect transistors (GNR FETs). We were able to achieve I_{ON}/I_{OFF} ratio of 10^3 using either top- or back-gates and we analyzed the high field characteristics of such devices.

We use exfoliated graphene flakes on 300 nm SiO_2 formed on a highly conductive Si wafer, which is metalized from the back to serve as a back-gate. We have patterned graphene flakes successfully forming nanoribbons down to 30 nm. To achieve this we used 20 nm thick Al as a mask patterned by e-beam lithography using PMMA and lift-off. Cr/Au source/drain contacts and Al_2O_3/Ti/Au as top gate (t_{ox}=15 nm) have been deposited to form FETs. The channel lengths of the fabricated devices range from 2 – 8 μm and the gate length is about 0.4 μm less leaving 200 nm access regions on both sides of the gate. Temperature dependent measurements confirmed that >26 meV band-gap opened in the devices depending on the width and as a result we observed 10x top gate modulation at room temperature and 200x modulation at 4 K by varying the top gate potential between +/- 2.5V. Operating the device at high source-drain potential we observed nonlinearity in the source-drain current but the detailed analysis showed that this is not due to saturation but rather because of the relative band alignment of the p and n regions controlled by top- and back-gates. The doping of the graphene at the contact regions of the devices are possibly determined by the work function difference of the contact metal and the graphene [3]. If one chooses a metal with work function very similar to graphene this effect can be minimized and we can model the carrier density solely as a function of electrostatics. Cr was our choice ($W_{Cr} \sim W_{gr}$ = 4.5 eV) for ohmic metallization.

We observed two distinct operational modes of the device. In the cases when both the back and the top gate bias have the same sign the GNR is homogenously doped n or p type and this corresponds to a high conductivity state. If the top gate bias has an opposite sign the GNR is doped npn or pnp and this corresponds to a low conductivity state due to the barrier. In conventional semiconductor materials this would be the off-state, but due to the tiny bandgap of the GNR this barrier is just a double tunnel junction. At high enough source-drain bias the lateral field starts to compensate the vertical field of the gate and pulls back the band to homogenous state (entirely n or entirely p) and switch back the device to the high conductance state. This is a completely new phenomenon attributable to the band gap opening in the ribbons which cannot be observed in 2D graphene FETs. We weren't able to drive the GNR FETs to the same saturation regime which is observed in 2D GFETs due to high gate leakage. But we can conclude that the observed sublinear behavior is not due to phonon limited saturation, but rather due to the onset of tunneling through the GNR bandgap, a first step towards realizing GNR-based tunnel FETs [4].

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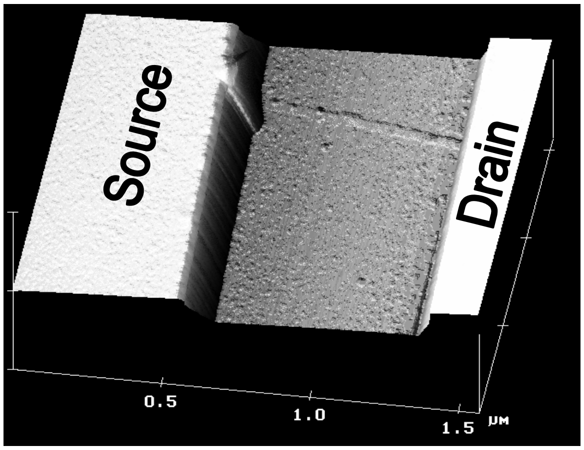

Fig. 1 AFM micrograph of 40 nm wide graphene nanoribbon before the top gate is deposited.

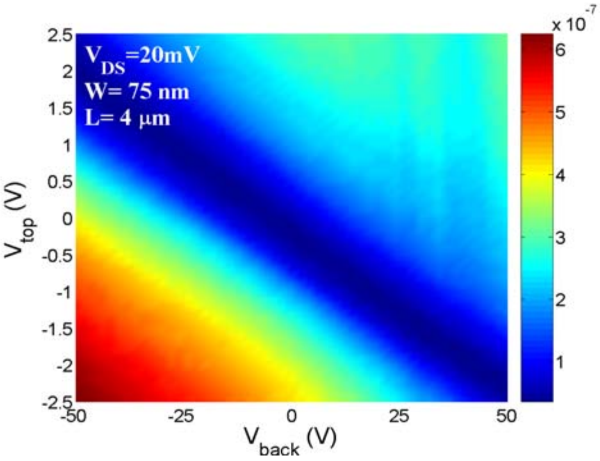

Fig. 2 Combined top- and back-gate dependence of the GNR FET drain current.

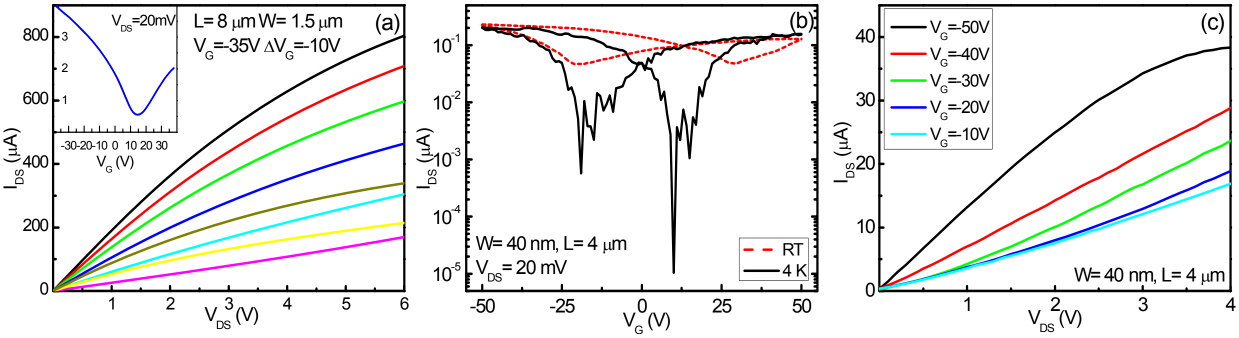

Fig. 3 (a) Tendency to saturation in the output characteristics of 2D graphene FET. Inset: Gate dependent drain current modulation of the same device. (b) 5x room temperature and 10^4x 4 K modulation of back gated (t_{ox}= 300 nm SiO_2) GNR FET. (c) Observed sublinear I-V characteristic of a back gated GNR FET possibly caused by Dirac-point shifting and not due to phonon limited saturation. (Measured at room temperature).

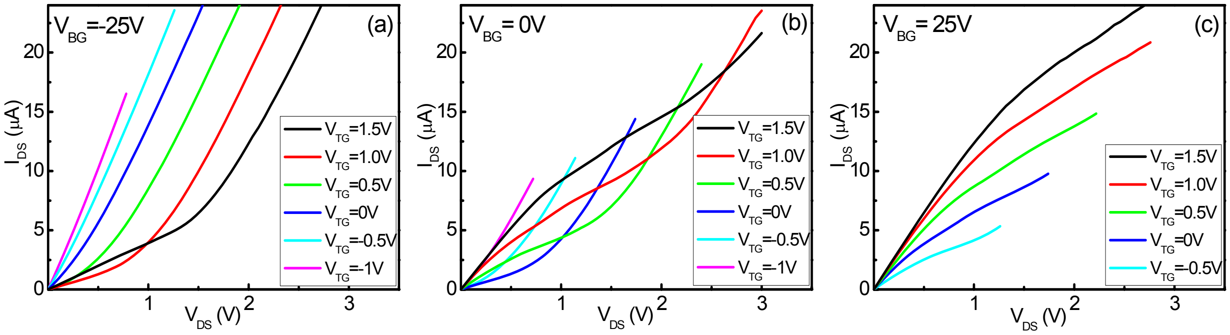

Fig. 4 Output characteristics of the GNR FET (L = 4 μm, W = 75 nm) at different top gate biases. (a) If both gate is negative the resistance is low. In case of positive top gate bias the resistance is high until the drain bias compensate the top gate bias. (b) At zero top gate bias the transition between case (a) and (c) can be observed. (c) High to low resistance transition occurs when the gate to source potential is about zero.