

Operation Regimes of Double Gated Graphene Nanoribbon FETs

Kristof Tahy, Chuanxin Lian, Huili (Grace) Xing and Debdeep Jena

Department of Electrical Engineering, University of Notre Dame, IN, USA, ktahy@nd.edu

The unique electronic properties of graphene have ignited active research in the past few years. Though in theory its electronic structure and transport properties are well known, the applicability as channel replacement material in conventional CMOS technology is still an open question. High mobility [1] and high current carrying capacity [2,3] make graphene very attractive, but on the other hand low I_{ON}/I_{OFF} ratio and the lack of sufficient saturation in I_{ON} are yet unsolved drawbacks. In the past we demonstrated these properties in double-gated graphene nanoribbon field effect transistors (GNR FETs). We successfully achieved I_{ON}/I_{OFF} ratios of 10^6 at cryogenic temperatures using either top- or back-gates and sublinear output characteristic was observed [3]. Now we present the detailed analysis of the distinct operational modes of such devices at high applied source-drain field.

We use exfoliated graphene flakes on 300 nm SiO_2 formed on a highly conductive Si wafer, which is metalized on the backside to serve as a back-gate. We have patterned graphene flakes successfully forming nanoribbons with widths down to 25 nm. To achieve this we used 20 nm thick Al as a mask patterned by e-beam lithography using PMMA and lift-off. Cr/Au source/drain contacts and $\text{Al}_2\text{O}_3/\text{Ti}/\text{Au}$ as top gate ($t_{ox}=30$ nm) have been deposited to form FETs. 1 nm e-beam deposited Al was used as seed layer for the ALD deposited Al_2O_3 . The channel length of the fabricated devices is 2 μm and the length of the top gate electrode is about 1 μm , covering half of the channel. Temperature dependent measurements have confirmed band-gap opening of $>26\text{meV}$ depending on GNR widths, and result in 20x and 10^4 x modulation at room temperature and 4 K, respectively, by varying the top gate potential between +/- 5V. Operating the device at high source-drain bias gives nonlinearity in the source-drain current but the detailed analysis shows that this is not due to velocity saturation but rather because of the relative band alignment of the p and n regions controlled by top- and back-gates.

We observed two distinct operational modes of the device. In the cases when both the back and the top gate bias have the same sign the GNR channel is homogeneously doped to n-n+ or p-p+ and this corresponds to a high conductivity state. In these states pinch-off occurs at high source-drain bias. At certain bias conditions the depletion at the drain side extends and due the small bandgap of the GNR opposite carriers starting to accumulate, which leads to ambipolar channel formation. The source-drain current is (super)linearly increasing again as we increase V_{DS} . This phenomenon has been observed in 2D graphene FETs and called 'kink effect' [2].

The other case is when the top gate bias has an opposite sign than the back gate bias therefore the GNR is doped np or pn and this corresponds to a low conductivity state due to the barrier. In conventional semiconductor materials this would be the off-state, but due to the tiny bandgap of the GNR this barrier is just an interband tunnel junction. Soon the source-drain bias starts to compensate the vertical field of the gate and pulls back the bands to homogenous state (entirely n or entirely p) and switch back the device to the high conductance state. In other words the junction of the initially ambipolar channel moves towards the drain and finally diminishes.

In conclusion, pn junction in GNR FETs has been experimentally demonstrated. The analysis of the device operation shows that at certain bias conditions weak rectification is realizable.

References

- [1] A. K. Geim and K. S. Novoselov, "The rise of Graphene," *Nature Materials*, vol. 6, pp. 183-191, March 2007.
- [2] I. Meric, M. Y. Han, A. F. Young, B. Oezylmaz, P. Kim and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," *Nature Nanotech.*, vol. 3, pp. 654-659, Sept. 2008.
- [3] K. Tahy, S. Koswatta, T. Fang, Q. Zheng, H. Xing, and D. Jena "High Field Transport Properties of 2D and Nanoribbon Graphene FETs", *IEEE DRC Conf. Digest.*, vol. 67, pp 207-208, June 2009.

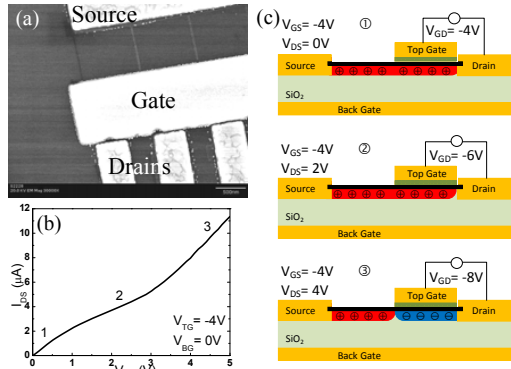


Fig. 1 (a) SEM micrograph of GNR FETs; (b) Measured I-V characteristics showing three distinct mode of operation; (c) Schematic carrier concentration along the device at the conditions noted in (b).

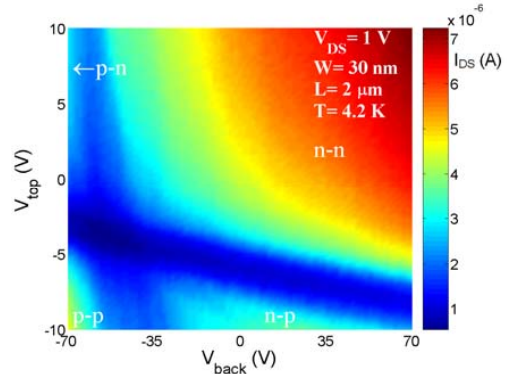


Fig. 2 I_{DS} as a function of the top- and back-gates at high ($V_{DS}=1$ V) source drain bias. Without any applied bias the channel is n-type. ($t_{ox_top}=30$ nm Al_2O_3 , $t_{ox_back}=300$ nm SiO_2)

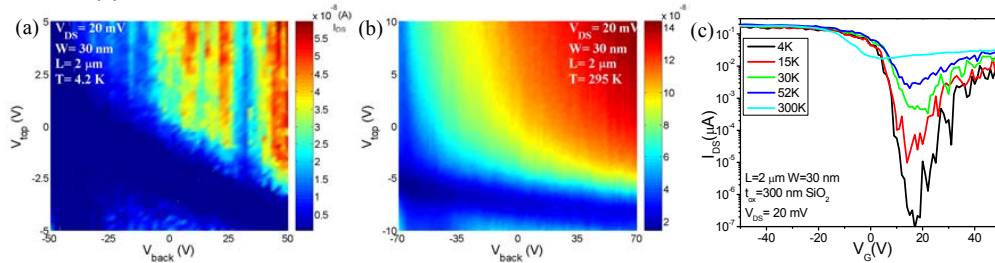


Fig. 3 (a) Conductance steps at 4.2 K at low source-drain voltage (linear scale); (b) At room temperature the modulation is smaller even at low bias ($V_{DS}=20$ mV); (c) The strong temperature dependence of the minimum conductance point is a consequence of the band gap opening.

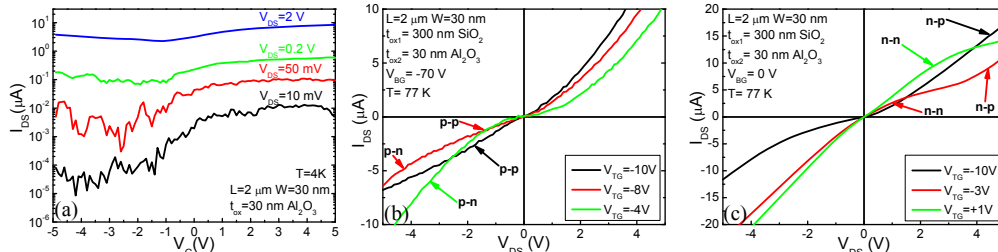


Fig. 4 (a) Drain bias dependence of the gate modulation. At high fields the modulation drops below 10x even at 4.2 K; (b) At $V_{TG}=-10$ V the device can be pushed to p-p mode. The saturation like feature is due to pinch-off at the drain end. At $V_{TG}=-8$ V the conductance increasing again after partial pinch-off at $V_{DS}=-2$ V. At $V_{TG}=-4$ V we can observe the conductance of the ambipolar channel; (c) The originally n-n channel ($V_{TG}=+1$ V) can be pinched-off at more negative top gate bias ($V_{TG}=-3$ V) until the ambipolar channel is formed even at $V_{DS}=0$ V.

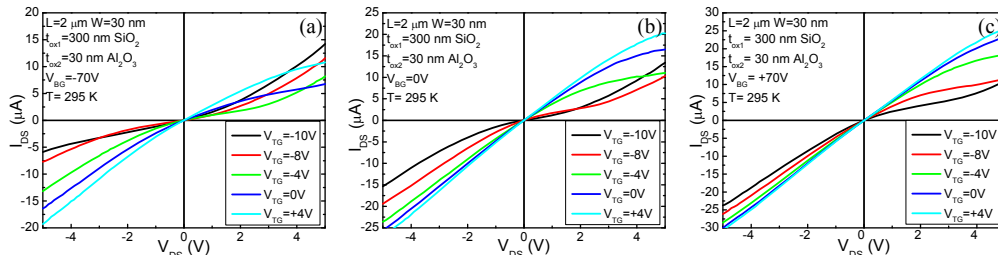


Fig. 5 Room temperature I-V measurements of the same device shown in Fig. 4 at -70 V (a), 0 V (b) and +70 V (c) back gate bias.