

# Device Characteristics of single-layer Graphene FETs grown on Copper

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The exceptional electrical properties of graphene materials have led to an explosion of research investigating the potential of graphene as the foundation for a future generation of devices as well as developing methods of producing high quality graphene materials. Material quality and our ability to manipulate the properties of graphene will ultimately determine the success of graphene as a device platform. Recently, the formation of single layer graphene via catalyzed-chemical vapor deposition (CVD) on copper foils has generated much interest [1]. A few groups have reported the CVD growth of graphene on copper, and transport properties including quantum Hall effect [2,3] in layers subsequently transferred to insulating substrates. However, there have been no careful studies of FETs fabricated from them. In this work, we report the characteristics of single-layer graphene FETs whose channels were grown by CVD on copper.

Single layer graphene films were grown using catalyzed-CVD on copper foils and on evaporated copper films. Pre-growth chemical and thermal treatment of the copper catalyst material enables single layer graphene deposition at temperatures ranging from 800-1050 °C (Fig. 1). Following CVD growth, graphene sheets are transferred to a range of host substrates using wet etch methods similar to those described earlier [1]. Using Raman mapping, large area single-layer graphene regions are verified from the signature 2D:G peak ratio of  $\sim 2$ , that is uniform over large regions (Fig. 2). Complementary SEM and AFM characterization corroborate the Raman result.

Back-gated FETs were prepared by transferring the single-layer graphene to 300 nm SiO<sub>2</sub>/conductive Si substrates, followed by conventional e-beam lithography, O<sub>2</sub> plasma etching of the graphene for device isolation, ohmic metal evaporation (Cr/Au), and lift-off. The backside of the conductive Si wafer was metalized for back gating. The channel lengths of the FETs range from 1 – 8  $\mu\text{m}$  and the channel widths vary between 1 – 4  $\mu\text{m}$ ; Fig. 2 (e) shows a schematic cross section of the devices. Based on the transfer characteristics (Fig. 3 (a)), the field-effect mobility is found to be  $\sim 4500 \text{ cm}^2/\text{Vs}$  for electrons and slightly lower for holes. The Dirac point is at  $V_{\text{BG}} \sim 2 \text{ V}$ , much closer to zero volt than in case of exfoliated graphene sheets, indicating a clean surface on both sides, and absence of large unintentional charge species. The impurity concentration is estimated from the measurement to be  $\sim 8 \cdot 10^{10} \text{ cm}^{-2}$ . The devices exhibit field-effect current modulations of  $\sim 4 - 6$  at 20 mV  $V_{\text{DS}}$  at gate sweeps of  $\pm 30\text{V}$  (Fig. 3 (a)). Interestingly at very low applied source-drain bias ( $V_{\text{DS}} = 20 \mu\text{V}$ ) the modulation increases significantly (Fig. 3 (b)). The current does not scale linearly;  $\sim 1000\text{X}$  lower bias causes less than  $\sim 10\text{X}$  smaller current. The apparent field-effect mobility is  $\sim 200\,000 \text{ cm}^2/\text{Vs}$ , but we stress that this is *not* a fundamental property of graphene, it just indicates the limitation of the traditional model to estimate the mobility of high purity graphene samples.

At high drain bias voltages (Fig. 3 (c)), the DC output characteristics of the devices were linear up to  $\sim 1 \text{ V}$   $V_{\text{DS}}$ , and deviated significantly from linearity at higher drain biases. The super-linear behavior is specially evident at gate biases close to the Dirac point, and is indicative of zero-gap single-layer graphene. We have previously reported device performance for 2D exfoliated [4] and SiC based epitaxial graphene [5]. Transfer characteristics and high field output characteristics of graphene FETs derived from these three methods will be compared.

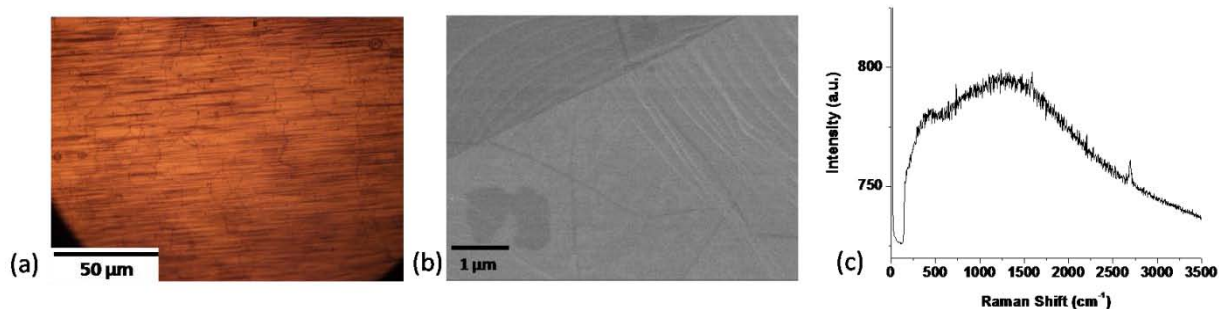
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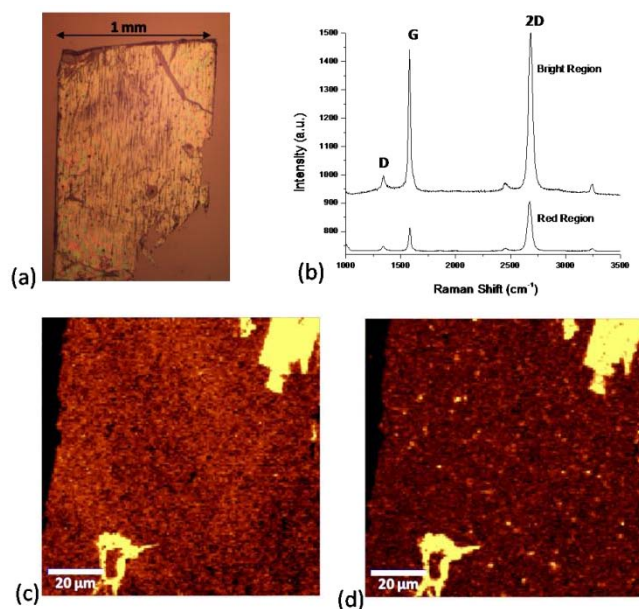
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[4] K. Tahy et al., IEEE DRC Tech. Digest **67**, p 207, 2009.

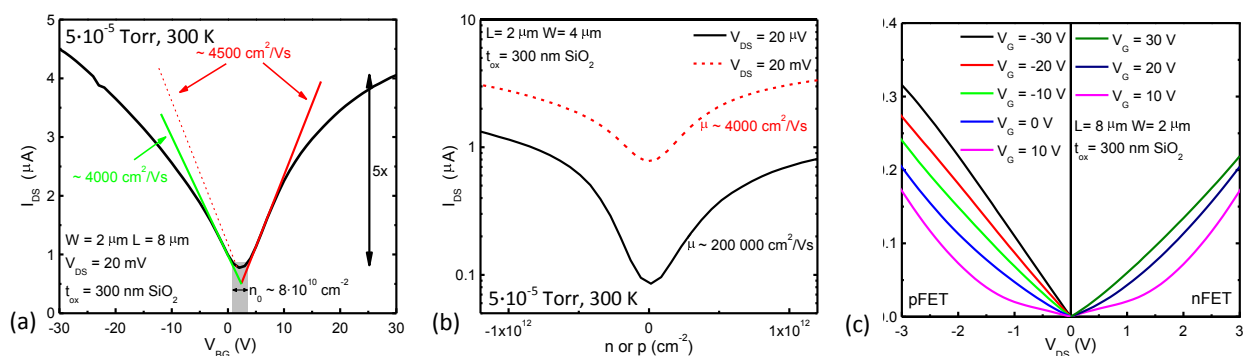
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**Fig. 1:** Graphene as grown on copper foil. (a) Optical micrograph showing underlying grain structure of copper and roll marks on copper surface. (b) SEM image showing a copper grain boundary, terraces in the copper surface, wrinkles in the overlying graphene layer, and a region with a second layer of graphene. (c) Raman spectrum of as grown graphene before transfer; the broad large peak is due to the copper foil, while the small sharp peak near  $2700\text{ cm}^{-1}$  is the 2D graphene peak.



**Fig. 2:** (a) Graphene/PMMA layer stack transferred to a  $\text{SiO}_2/\text{Si}$  wafer. (b) Raman spectrum of the transferred graphene following removal of PMMA. The lower spectrum is dominant across the graphene region with a 2D:G peak intensity ratio of approximately 2, consistent with single layer graphene. (c) Raman map of the 2D peak intensity across a region of the transferred graphene, showing uniform intensity over large areas of the sample. (d) Raman map of the G peak intensity across a region of the transferred graphene, showing uniform intensity over large areas of the sample. (e) Device schematic of a transferred graphene FET.



**Fig. 3:** (a) Transfer characteristic of a 2D graphene FET transferred to  $\text{Si}/\text{SiO}_2$  substrate. The device exhibit relatively high and symmetric mobility and 5 times modulation. The calculated impurity concentration is  $8 \cdot 10^{10}\text{ cm}^{-2}$ . (b) Very low ( $V_{\text{DS}} = 20\ \mu\text{V}$ ) applied drain bias gives an extremely high apparent field-effect mobility. Notice that the current doesn't scale with the applied voltage, indicating the limitations of traditional models of extracting carrier mobility in high purity 2D graphene samples. (c) High-field family I-V curves showing both sub-linear and super-linear behavior, characteristic of a zero bandgap single layer graphene.