High Performance E-mode InAlN/GaN HEMTs: Interface States from Subthreshold Slopes

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Due to the high two-dimensional electron gas (2DEG) concentration and high temperature stability, lattice matched InAlN/AlN/GaN high electron mobility transistors (HEMTs) have attracted tremendous amount of interest for high-power and high-frequency electronics [1-2]. Employing the gate recess technology, a popular way to develop enhancement-mode (E-mode) devices for digital and mixed signal applications, record high performance (output current density of 2 A/mm, extrinsic transconductance of 890 mS/mm, and f_t/f_{max} of 95/135 GHz for 150-nm gate length) have been very recently reported on E-mode InAlN HEMTs [3]. Temperature dependent characterization of the subthreshold slope (*SS*) can provide valuable information on the interface states and their distribution near the band edges. In this paper, we have performed the field-effect measurements on these gate-recessed E-mod InAlN HEMTs reported in Ref. 3, and extracted the interface states from the temperature dependent *SS* from 80 to 300 K.

The InAlN/AlN/GaN device structure (Fig. 1 inset) consists of an 8.7-nm InAlN barrier, a 1-nm AlN spacer and a Fe-doped GaN semi-insulating buffer on SiC substrate by MOCVD. The 2DEG concentration and mobility were measured to be 2.23×10^{13} cm^{-2} and 983 cm^2/Vs in the as-grown heterostructure. A Ti-based alloyed ohmic contact scheme resulted in a contact resistance of ~ 0.6 ohm-mm. The gate recess was realized by reactive ion etch prior to the gate metal deposition. The resultant HEMTs have a gate length of 150 nm and are passivated with SiN. The temperature-dependent field-effect measurements were carried out on a Lakeshore cryogenic probe station using a Keithley 4200-SCS system.

Shown in Fig. 1 are the representative family I-Vs and transfer curves of the HEMTs in this study, which underwent a different gate recess time from the devices with the record performance in Ref. 3. The drain induced barrier lowering (DIBL) over the drain bias range of 0.1 to 6 V was measured to be ~ 100 mV/V, which is comparable to the reported value for AlGaN HEMTs with a 0.6-μm gate length [4]. The low DIBL value indicates the short channel effect is minimal for these devices owing to the very thin barrier (~ 2 nm) upon gate recess. Over the entire temperature range in this study the contact resistance was found to be nearly constant and the sheet resistance decreases with decreasing temperature (Fig.2).

In spite of the very thin barrier, a high I_{on}/I_{off} ratio was measured, 10^7-10^8, over the bias and temperature range in this study (Fig. 2). The *SS* value was extracted at the steepest point of the I_d-V_{gs} transfer curve at V_{ds} = 2.5 V. As shown in Fig. 2, the *SS* value shows linear *T*-dependence from 80 K to 300 K, consistently 30 mV/decade higher than the theoretical limit. In the subthreshold region, the *SS* can be expressed in terms of the barrier capacitance C_b, the quantum capacitance C_q and the interface trap capacitance C_{it}, $SS = [1+(C_q+C_{it})/C_b]\,(k_BT/q)\ \ln 10$, where C_q is negligible. As a result, one can extract C_{it} and the interface trap density D_{it}, shown in Fig. 3. The measured D_{it} is 8×10^{13} cm^{-2} eV^{-1} at 80 K and it drops to 2×10^{13} cm^{-2} eV^{-1} at 300 K, about 2-10 times higher than the reported values in non-recessed AlGaN HEMTs [4], possibly due to the gate recess process. The similar *T*-dependent trend of D_{it} has been reported for Si/SiO_2 interfaces [5], attributed to the increasing D_{it} toward the conduction band edge. The gate-lag pulse I-Vs were also measured at 300 K to interrogate the effects of the interface states, with a pulse width of 0.5-ms or 1-ms, and a base of 0 V, while the drain bias was swept from 0 to 5 V, as shown in Fig. 4. The knee walkout observed under shorter pulses indicates some of the interface states have slow response time, consistent with the knee walkout observed in the DC family I-Vs at 80 K.

In conclusion, the temperature dependent subthreshold slope has been studied in the gate-recessed E-mode InAlN/GaN HEMTs. The ongoing comparative study on the non-recess HEMT structure will allow us to estimate the possible plasma damage to the gate stack in the gate-recess process, thus providing a valuable tool to guide the future device fabrication optimization. This work is supported by the DARPA NEXT program (HR0011-10-C-0015) monitored by Dr. John Albrecht.

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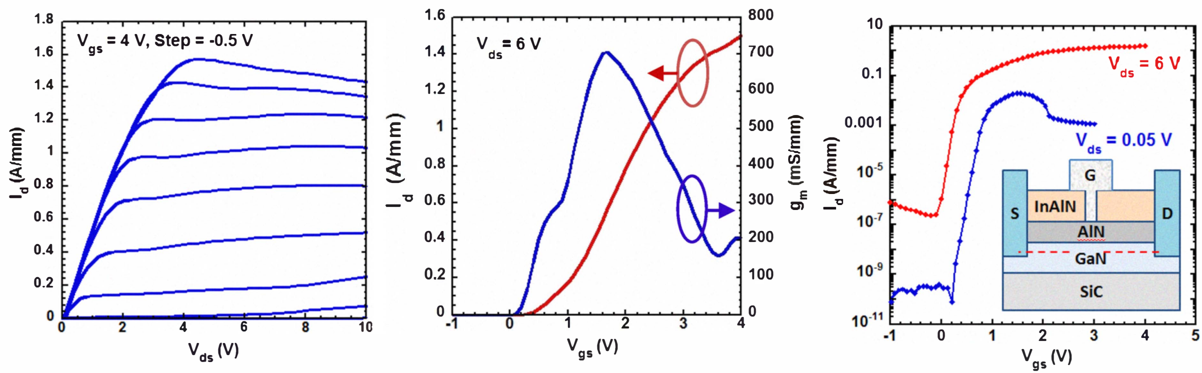

Fig. 1 Family I-Vs and transfer curves of the gate-recessed E-mode InAlN/GaN HEMTs.

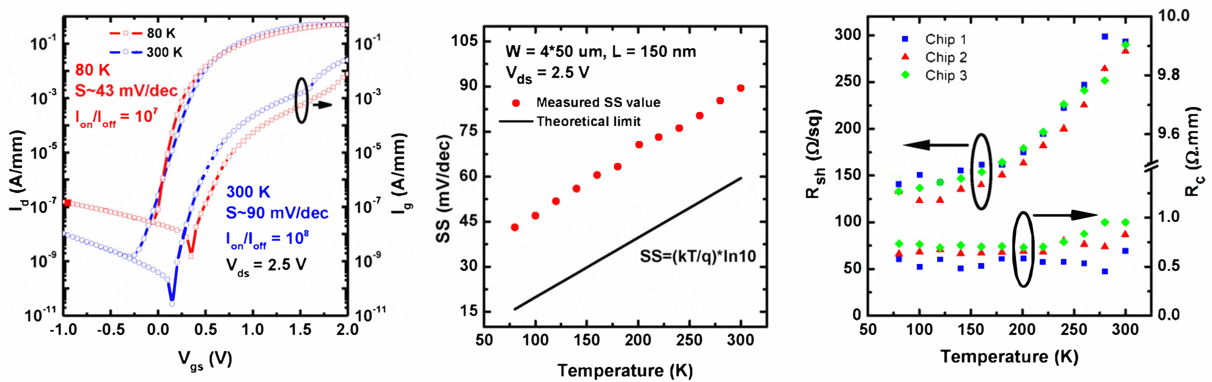

Fig. 2 Temperature dependent transfer curves, subthreshold slope and TLM sheet resistance.

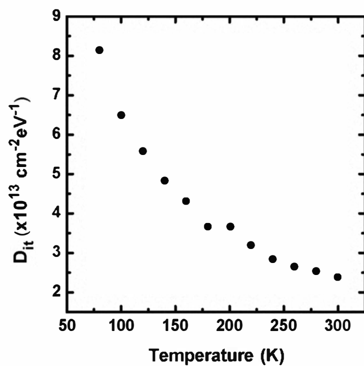

Fig. 3 Extracted interface trap density from *SS* at different temperatures.

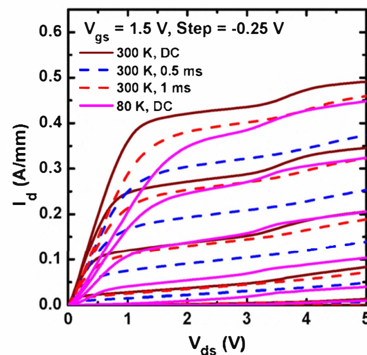

Fig. 4 Gate-lag pulsed family I-Vs at 300 K and DC I-Vs at 80 K.

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