Sub-10 nm Epitaxial Graphene Nanoribbon FETs

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Graphene is being investigated as a promising candidate for electronic devices. For digital electronic devices, a substantial bandgap is necessary. It is possible to open a bandgap in graphene by quantum confinement of the carriers in patterned graphene nanoribbons (GNRs); GNRs with width W nm have a bandgap $E_g \sim 1.3/W$ eV [1]. This implies that sub-10 nm wide ribbons can enable room-temperature operation of GNRs as traditional semiconductors, but with ultimate vertical scaling, and still take advantage of high current drives. To date, GNRs have been fabricated from exfoliated graphene [2] and operated by back gates, or nanometer scale ribbons produced by 'explosive' methods [3] that are neither controlled nor reproducible. These methods are not suitable for large-area device fabrication. In this work, we report lithographically patterned GNRs on epitaxial graphene on SiC substrates. Specifically, we show the first top-gated GNR field-effect transistors (FETs) on epi-graphene substrates that exhibit the opening of a substantial energy bandgap (exceeding ~0.15 eV at a ribbon width of 10 nm), respectable carrier mobility (700 - 800 cm²/Vs), high current modulation (10:1 at 300 K), and high current carrying capacity (0.3 mA/µm at $V_{DS} = 1$ V) at the same time. Both single GNR and GNR array devices are reported.

Epitaxial graphene was grown on Si-face 6H-SiC [4]. Raman measurements indicate predominantly single layer graphene coverage. The graphene was patterned by e-beam lithography and etched in an O_2 plasma. Hydrogen silsesquioxane (HSQ), a negative-tone electron-beam resist, was used to form sub-10 nm GNRs. A 15 nm thick ALD Al₂O₃ film on spin-coated HSQ was used as the top-gate insulator [Fig. 1]. The HSQ was used to seed the ALD deposition. The gate stack was found to have a small hysteresis in the *I-V* characteristics. E-beam evaporated Cr/Au source/drain contacts were then deposited to form FETs.

The device transfer characteristics of a top-gated 10 nm wide GNR device are shown in Fig. 2(a). Room temperature modulation is ~ 10 , but the 4 K modulation increases to $\sim 10^6$, clearly indicating the opening of a bandgap. The opening of a 0.15 eV bandgap was confirmed by temperature dependent measurements of the offstate current. Measurement of the differential conductance as a function of V_{DS} and V_{GS} at 4 K shows a transport gap exceeding 0.15 eV [Fig. 2(b)]; similar gaps were measured on multiple devices and are plotted in Fig. 1(e). The family I-V curves shown in Fig. 2(c) indicate that the GNR FETs a) switch off, b) carry ~0.3 mA/µm current density at $V_{DS} = 1$ V, and c) are yet to saturate. One way to further increase the net current drive is to use a parallel array of GNRs between the source and the drain. In Fig. 3, the characteristics of such a GNR array FET with 30 parallel 13 nm wide GNRs with a 30 nm pitch is shown. That the drain current scales with the number of ribbons is expected, but the net transfer characteristics of individual GNRs is also preserved in the array and reproducible over multiple devices. This implies that possible non-uniformities in GNR widths and edge roughnesses have a minimal effect in the measured devices. The maximum high-field current drive measured before breakdown was extremely high approaching \sim 7.5 mA/µm if scaled to the active ribbon width (390 nm). Scaling by the total channel width (30 x 13 nm + 30 x 17 nm gap) would lead to $3.25 \text{ mA/}\mu\text{m}$, which is still remarkable. Such high current drives have never been reported in graphene before. We attribute this high current carrying capability to the high electrical and thermal conductivity of the 1D graphene channels (due to absence of lateral scattering), coupled with the excellent thermal conductivity of the underlying SiC substrate.

The above results are the first report of top-gated GNR FETs on large-area epitaxial graphene exhibiting exceptionally high drive currents, the opening of a substantial bandgap, and linear scaling of properties with the number of GNRs in parallel arrays. In this light, the disadvantages typically attributed to GNRs (such as edge-scattering and resultant degradation of device performance) need to be carefully re-examined. By scaling the widths down further, substantial modulation at room temperature is expected. This work was supported by the Semiconductor Research Corporation Nanoelectronics Research Initiative and the National Institute of Standards and Technology through the Midwest Institute for Nanoelectronics Discovery (MIND) and, in part, by the Office of Naval Research (ONR).

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Fig. 1. (a) SEM micrograph of a GNR FET showing the 10 nm HSQ mask and the source/drain electrodes. (b) The 10 nm graphene channel after the removal of the HSQ mask. (c) Schematic of GNR FET with Au/Al₂O₃/HSQ gate stack. (d) Wafer-scale optical image of the GNR FETs. (e) The scaling of the band gap E_{gap} with respect to decreasing GNR width follows the expected $1.3/W_{GNR}$ trend.



Fig. 2. (a) Transfer characteristic of a 10 nm GNR FET on room temperature and at 4 K. **(b)** Differential conductance dI_D/dV_{DS} as a function of V_{DS} and V_{GS} . The color bar is the exponent, $\log_{10}(dI_{DS}/dV_{DS})$ in Ω^{-1} . Transport gap of ~ 0.15 eV is observed. **(c)** Low temperature family *I-V* of the same device showing good on/off ratio.



Fig. 3. (a) Gate dependence of I_{DS} in a FET with 30 parallel 13 nm GNR channel with a 30 nm pitch. Despite the possible width variations, an on/off ratio of 10⁴ is achieved at low temperature. (b) Output characteristics of the 30 GNR array-FET at 4 K. (c) The current drive of the 30 GNR array-FET is approximately 30 times of the current of a single GNR FET. The very high measured maximum current density of ~7.5 mA/µm is attributed to the excellent thermal conductivity of the SiC substrate. Current density is scaled for the active ribbon area (390 nm). Scaling by the total channel width (30 x 13 nm + 30 x 17 nm gap) would lead to 3.25 mA/µm, which is still remarkable.