220-GHz Quaternary Barrier InAlGaN/AlN/GaN HEMTs

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***Abstract*—Depletion-mode high-electron mobility transistors (HEMTs) based on a quaternary barrier $In_{0.13}Al_{0.83}Ga_{0.04}$ N/AlN/GaN heterostructure on SiC substrate were fabricated. The 66-nm-long gate device shows a dc drain current density of 2.1 A/mm, a peak extrinsic transconductance of 548 mS/mm, and a record current gain cutoff frequency f_T of 220 GHz for quaternary barrier GaN-based HEMTs, which is also among the highest f_T for all GaN-based HEMTs. The large $L_g \cdot f_T$ product of 14.5 GHz $\cdot\ \mu$m with a gate-length-to-barrier-thickness aspect ratio of 5.8 indicates a high effective electron velocity of 0.9×10^7 cm/s, attributed to a high electron Hall mobility (1790 cm^2/V $\cdot$ s at an n_s of 1.8×10^{13} cm^{-2})—the highest reported in GaN-channel HEMTs with In-containing barriers. An intrinsic electron velocity of 1.7×10^7 cm/s, extracted from conventional Moll delay-time analysis, is comparable to that reported in the state-of-art AlGaN/GaN HEMTs.**

***Index Terms*—AlN, cutoff frequency, electron velocity, GaN, high-electron mobility transistor (HEMT), HFET, InAlGaN, mobility, quaternary.**

I. Introduction

LATTICE-MATCHED $In_{0.17}Al_{0.83}$N/AlN/GaN high-electron mobility transistors (HEMTs) have drawn intensive attention as an alternative to conventional AlGaN/GaN HEMTs due to their excellent dc and RF performance [1]–[9]. However, improving the 2-D electron gas (2-DEG) mobility in InAlN-based heterostructures has remained a challenge. This is possibly due to increased interface roughness scattering [10] arising from microscopic variations in the strain field driven by the immiscibility between AlN and InN [11]. The highest reported mobility $\mu_0 = 1635$ cm^2/V $\cdot$ s (sheet concentration, $n_s \sim 1.1 \times 10^{13}$ cm^{-2}) in InAlN/AlN/GaN [8] is lower than 1850 cm^2/V $\cdot$ s($n_s \sim$ 1.1-1.9 $\times 10^{13}$ cm^{-2}) reported for AlN/GaN at comparable 2-DEG concentration [12]. It has been predicted that InAlGaN quaternaries have narrower immiscibility gaps than all ternary alloys except AlGaN [11], and thus, higher mobilities can be expected. Good transport properties, with $\mu_0 > 1700$ cm^2/V $\cdot$ s and $n_s \sim 1.8 \times 10^{13}$ cm^{-2}, have been obtained in lattice-matched $In_{0.16}Al_{0.74}Ga_{0.10}$N/AlN/GaN heterostructures [13], but no RF data were reported. Nearly lattice-matched $In_{0.07}Al_{0.40}Ga_{0.53}$N HEMTs grown by molecular beam epitaxy [14] showed a 2.3-A/mm drain current density, a 675-mS/mm peak transconductance, and a 5.6-W/mm power density at 10 GHz, but the current gain cutoff frequency f_T was relatively low, 54 GHz for a 150-nm gate. Quaternary nitrides also provide additional freedom to adjust the strain and bandgap, which is attractive for applications such as UV light emitting diodes [15] and enhancement-mode HEMTs.

In this letter, we report high 2-DEG concentration and mobility achieved in slightly tensile strained quaternary barrier $In_{0.13}Al_{0.83}Ga_{0.04}$N/AlN/GaN heterostructures. Depletion-mode (D-mode) HEMTs on SiC substrate without gate recess showed a record f_T of 220 GHz with a 66-nm-long gate and an 11.3-nm-thick top barrier. An $L_g \cdot f_T$ product of 14.5 GHz $\cdot\ \mu$m was achieved for a gate-physical-length-to-barrier-thickness aspect ratio of 5.8, also among the highest reported to date for GaN-based HEMTs.

II. Experiments

The InAlGaN/AlN/GaN HEMT structure consists of a 10.3-nm $In_{0.13}Al_{0.83}Ga_{0.04}$N barrier, a 1.0-nm AlN spacer (total barrier thickness $t_{\rm bar} = 11.3$ nm), a 55-nm unintentionally doped GaN channel, and a 1.8-μm semi-insulating GaN buffer on SiC substrate, grown by metal organic chemical vapor deposition at Kopin Corporation. The layer composition and thickness were extracted from high-resolution X-ray diffraction, secondary ion mass spectrometry, and high-resolution transmission electron microscopy (HRTEM).

The process follows the same flow as presented in [9]: mesa isolation using chlorine-based reactive ion etching, followed by alloyed ohmic contacts using a Si/Ti/Al/Ni/Au stack annealed at 860 °C in N_2 ambient; rectangular Ni/Au (40/90 nm) gates without gate recess were defined by electron-beam lithography, followed by lift-off. The devices were finally treated with an O_2-containing plasma in the access region for dielectric-free

Manuscript received March 17, 2011; revised May 20, 2011; accepted May 23, 2011. Date of publication June 27, 2011; date of current version August 24, 2011. This work was supported in part by the Defense Advanced Research Projects Agency (John Albrecht, the NEXT program HR0011-10-C-0015), by the Air Force Office of Scientific Research (Kitt Reinhardt), and by AFRL/MDA (John Blevins). The review of this letter was arranged by Editor G. Meneghesso.

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Digital Object Identifier 10.1109/LED.2011.2158288

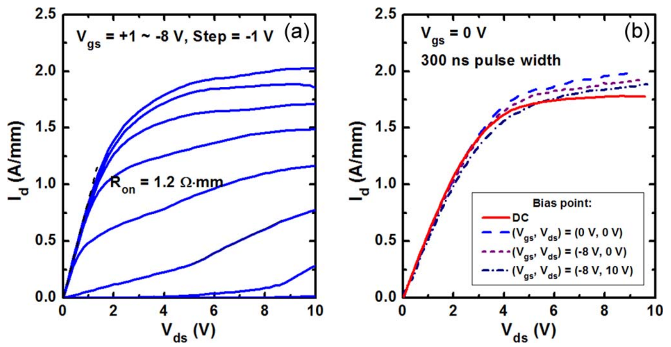

Fig. 1. (a) Common-source family of I–Vs on the quaternary HEMT with $L_g = 66$ nm and $L_{\mathrm{sg}} = 300$ nm. (b) Pulsed I–V measurements at $V_{\mathrm{gs}} = 0$, with a 300-ns pulsewidth and a 0.5-ms period of the same device shown in (a). The apparent R_{on} and knee voltage from the as-measured I–Vs are slightly larger in (b) due to a higher parasitic resistance of the setup.

passivation (DFP). The impact of DFP on device performance has been discussed elsewhere [9]. Transmission line method (TLM) measurements yielded a contact resistance of 0.36 $\Omega \cdot$ mm after processing. Room-temperature Hall effect measurements on a Van der Pauw test structure reveal a sheet resistance $R_{\mathrm{sh}} = 227\ \Omega/\mathrm{sq}$, $n_s = 1.5 \times 10^{13}\ \mathrm{cm}^{-2}$, and $\mu_0 = 1900\ \mathrm{cm}^2/\mathrm{V} \cdot \mathrm{s}$ before DFP; after DFP, $R_{\mathrm{sh}} = 190\ \Omega/\mathrm{sq}$, $n_s = 1.8 \times 10^{13}\ \mathrm{cm}^{-2}$, and $\mu_0 = 1790\ \mathrm{cm}^2/\mathrm{V} \cdot \mathrm{s}$. These mobilities are both among the highest reported, leading to the lowest sheet resistance in InN-containing HEMT structures [3], [14]. The small drop in mobility after DFP is due to enhanced scattering with increased n_s. The device presented here has a source–drain distance of 1.6 μm, a source–gate distance of 300 nm, a gate width of $2 \times 50\ \mu$m, and a gate length L_g of 66 nm, which has been confirmed by HRTEM.

III. Results and Discussion

Fig. 1(a) shows the common-source family of I–Vs of the device, measured for $V_{\mathrm{ds}} = 0$–10 V and $V_{\mathrm{gs}} = 1$ to -8 V. The device has an on-resistance $R_{\mathrm{on}} = 1.2\ \Omega \cdot$ mm extracted at $V_{\mathrm{gs}} = 1$ V. The maximum output current density $I_d = 2.0$ A/mm at $V_{\mathrm{gs}} = 1$ V is comparable with the dc performance of lattice-matched ternary InAlN HEMTs [9]. Although suffering from short-channel effects, the device can be pinched off with the gate leakage limiting the off-current [see Fig. 2(b)]. The two-terminal gate breakdown voltage was measured to be $\sim$20 V at $I_g = 1$ mA/mm. Pulsed I–V measurements were performed in air using a 300-ns pulsewidth and a 0.5-ms period, as shown in Fig. 1(b). The cold pulsed drain current density I_d at $V_{\mathrm{gs}} = 0$ is higher than that at dc, indicating that the device suffers from self-heating under dc operations. I_d pulsed from (-8 V, 0) and (-8 V, 10 V) showed only modest gate and drain lags of 2.8% (highest at $V_{\mathrm{ds}} = 8$ V) and 4.1% (highest at $V_{\mathrm{ds}} = 5$ V), respectively. The drain leakage current density of 0.1 mA/mm at (-8 V, 10 V) is sufficiently low for a valid pulsed I–V measurement.

The linear-scale transfer characteristic for V_{gs} swept from 3 to -8 V at $V_{\mathrm{ds}} = 6$ V is shown in Fig. 2(a). A measured $I_{\mathrm{d,max}} = 2.1$ A/mm at $V_{\mathrm{gs}} = 3$ V, with a threshold voltage $V_{\mathrm{th}} = -4.8$ V as extracted from the linear extrapolation of

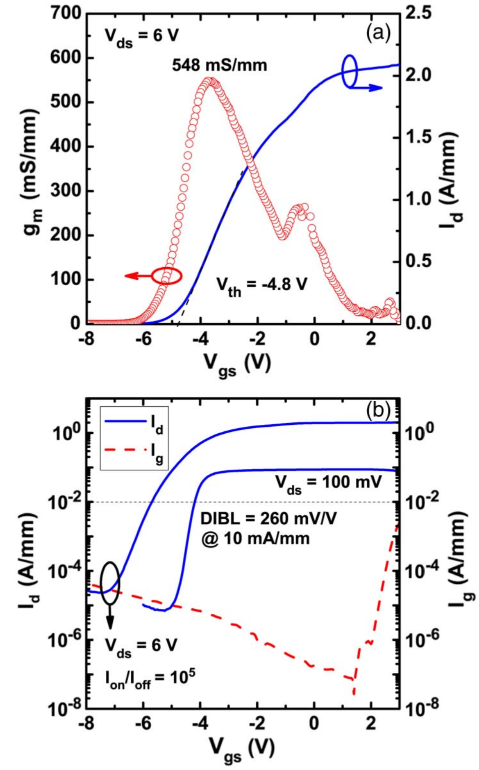

Fig. 2. Transfer characteristics of the device with $L_g = 66$ nm and $L_{\mathrm{sg}} = 300$ nm, measured at $V_{\mathrm{ds}} = 6$ and 0.1 V, in (a) linear scale and (b) semi-log scale.

I_d, has been obtained. The peak extrinsic transconductance $g_{\mathrm{m,peak}}$ is 548 mS/mm, corresponding to an intrinsic value of 710 mS/mm, for a source resistance $R_s = 0.42\ \Omega \cdot$ mm (estimated from the device geometry and TLM measurements). This extrinsic peak g_m is among the highest reported in GaN-based HEMTs with $t_{\mathrm{bar}} > 10$ nm [3]. The physics responsible for the second peak in g_m at $V_{\mathrm{gs}} = -0.5$ V, which has also been observed in InAlN/GaN HEMTs [5], [7], [9], is still under investigation. Fig. 2(b) shows the semi-log scale transfer curves measured at $V_{\mathrm{ds}} = 6$ and 0.1 V. The drain-induced barrier lowering is $\sim$260 mV/V measured at $I_d = 10$ mA/mm, indicating strong short-channel effects. However, the device maintains an ON/OFF current ratio of $\sim 10^5$ and good pinchoff ability within this bias range.

On-wafer device RF measurements were taken with an Agilent E8361C vector network analyzer in the frequency range from 250 MHz to 60 GHz. The network analyzer was calibrated using LRM off-wafer impedance standards, and measured S-parameters were de-embedded by subtracting on-wafer open pad parasitic capacitance. Fig. 3(a) shows the current gain $|h_{21}|^2$ and unilateral gain U of the device as a function of frequency at the peak f_T bias condition, $V_{\mathrm{ds}} = 4.7$ V, and $V_{\mathrm{gs}} = -3.7$ V. The extrapolation of both $|h_{21}|^2$ and U with a -20 dB/dec slope gives the current gain cutoff frequency/maximum oscillation frequency $f_T/f_{\max}$ of $\sim$220/60 GHz after de-embedding, from pre-de-embedding values of 153/54 GHz. The low $f_{\max}$ is attributed to the resistive rectangular gate. A small-signal equivalent circuit with RF intrinsic transconductance $g_{\mathrm{m,i}} = 718$ mS/mm, $R_s = 0.39\ \Omega \cdot$ mm, $R_d = 0.64\ \Omega \cdot$ mm, and $g_{\mathrm{ds}} = 135$ mS/mm was found to match

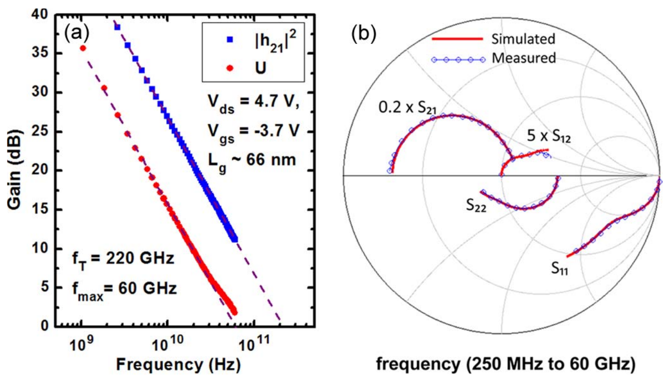

Fig. 3. (a) Current gain and unilateral gain of the device with $L_g = 66$ nm, showing $f_T/f_{\max} = 220/60$ GHz. (b) Comparison of simulated and measured S-parameters at $V_{\rm ds} = 4.7$ V and $V_{\rm gs} = -3.7$ V.

the measured and simulated S-parameters in the 0.25–60-GHz range, as shown in Fig. 3(b). These parameters agree well with dc measurements, and the simulated $f_T = 224$ GHz is in good agreement with the measured value.

To the best of our knowledge, $f_T = 220$ GHz reported in this letter is the highest achieved in quaternary barrier GaN-based HEMTs to date and is also among the highest reported in all GaN-based HEMTs [16], [17]. Accordingly, a high $f_T \cdot L_g$ product of 14.5 GHz $\cdot\, \mu$m was achieved for a gate-length-to-barrier-thickness aspect ratio of 5.8. The effective electron velocity $v_{\rm e-eff} = 2\pi \times L_g \times f_T$ was calculated to be 0.9×10^7 cm/s, slightly higher than $v_{\rm e-eff} = 0.8 \times 10^7$ cm/s in the ternary InAlN/GaN HEMTs fabricated under the same conditions [9]. Since the 2-DEG density and contact resistance are similar in the two devices, but μ_0 in the quaternary barrier HEMTs is 38% higher due to the reduced interface roughness and alloy scattering [10], [12], the higher effective electron velocity in quaternary barrier HEMTs most probably resulted indirectly from its higher mobility. Mobility and peak velocity are typically coupled in III–V compound semiconductors, with peak velocity proportional to $\sqrt{\mu_0}$ [18]. A conventional Moll analysis of delay-time components [19] resulted in an intrinsic delay time $\tau_{\rm int} = 0.39$ ps. The intrinsic electron velocity $v_{\rm e-int} = L_g/\tau_{\rm int}$ is calculated to be 1.7×10^7 cm/s, close to the value reported for state-of-the-art AlGaN/GaN HEMTs [17], [20]. To suppress the observed short-channel effects, use of back barriers and thinner top barriers is needed [8].

IV. Conclusion

D-mode $In_{0.13}Al_{0.83}Ga_{0.04}N$/AlN/GaN HEMTs with a tensile strained quaternary barrier were fabricated on SiC substrate. A device with a 66-nm physical gate length shows a record high f_T of 220 GHz in quaternary barrier HEMTs; this is also among the highest reported values in all GaN-based HEMTs. The device also shows good dc performance, with $I_{\rm d,max} = 2.1$ A/mm and extrinsic $g_{\rm m,peak} = 548$ mS/mm. The effective electron velocity of $\sim 0.9 \times 10^7$ cm/s is 12.5% higher than that in comparable lattice-matched ternary InAlN/AlN/GaN HEMTs, attributed to the higher mobility and low sheet resistance in quaternary barrier HEMTs.

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