Improvement of f_T in InAl(Ga)N barrier HEMTs by Plasma Treatments

Ronghua Wang[1], Guowang Li[1], Tian Fang[1], Oleg Laboutin[2], Yu Cao[2], Wayne Johnson[2],
Gregory Snider[1], Patrick Fay[1], Debdeep Jena[1], Huili (Grace) Xing[1,*]
[1]Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556
[2]Kopin Corporation, Tauton, MA 02780, USA * Email: hxing@nd.edu

GaN-based high electron mobility transistors (HEMTs) have been developed for high-temperature, high-frequency and high-power applications. To improve the transistor speed, various techniques have been explored in addition to scaling down the gate length and top barrier thickness: ultrathin SiN passivation to reduce access resistance and parasitic capacitances [1]; re-grown ohmic contacts and self-alignment to minimize access resistances [2, 3]; O_2 plasma treatment in the gate region prior to the metal deposition to suppress rf transconductance collapse [4]; and dielectric-free passivation (DFP) by a O_2-containing plasma treatment in the access region to shorten the gate extension in InAlN HEMTs [5]. Here we report a comparative study on the impact of various plasma treatments in the access region (DFP) as well as under the gate for InAl(Ga)N barrier HEMTs, and propose a model for the observed f_T improvement.

The HEMT heterostructures (Fig. 1) consist of either a lattice-matched ternary $In_{0.17}Al_{0.83}N$ (10.3 nm) or a tensile-stained quaternary $In_{0.13}Al_{0.83}Ga_{0.04}N$ (10.8 nm) barrier, a 0.5 nm AlN spacer and a C-doped semi-insulating GaN buffer on SiC substrate grown by metal organic chemical vapor deposition at Kopin Corporation. A Si/Ti/Al/Ni/Au ohmic stack annealed at 860 °C in N_2 resulted in a contact resistance R_c of 0.38 for InAlN barrier HEMTs (Group A), 0.36 & 0.50 Ω-mm for InAlGaN barrier (Group B & C) HEMTs, respectively. Rectangular Ni/Au gates were defined by electron-beam lithography and lift-off. As-fabricated devices in Group A and B were treated with an O_2-containing plasma in the access region only for DFP, while devices in Group C were treated with O_2, CF_4, or BCl_3 plasma in the gate region prior to the metal deposition. 2D electron gas (2DEG) transport properties monitored on wafer are shown in Table 1. All the devices have a nominal source-drain separation of 1.5 μm and a gate width of 2 x 50 μm.

As an example of the effectiveness of DFP on f_T improvement, small signal rf performance of an InAlN barrier HEMT with L_g = 60 nm is shown in Fig. 2 (a) before and after DFP. The increase in f_T from 125 to 210 GHz after the DFP treatment is attributed to the passivation of surface states in the access region and thus a shortened gate extension. Since a virtual gate forms due to surface states near the gate trapping electrons under large drain-gate electric field, high output resistance was observed in the I-Vs characteristics before DFP; after DFP of the surface states, strong short channel effects were seen [5]. The f_T dependence on gate length L_g for the InAlN and InAlGaN HEMTs (Group A and B) processed in parallel is shown in Fig. 2 (b), which suggests it is promising to achieve f_T > 250 GHz with L_g < 50 nm by employing the DFP technique. Fig. 2 (c) shows the trend of f_T as a function of V_{ds} at a gate bias near peak g_m before and after DFP for an InAlGaN barrier HEMT in Group B. The f_T of post-DFP devices increases quickly with V_{ds} transiting from the linear region to the saturation region, reaches a maximum value of 220 GHz at V_{ds} = 4.8 V, and then slightly drops at higher V_{ds}, ascribed to the widened gate depletion region toward the drain. In contrast, the pre-DFP f_T gradually increases with increasing V_{ds}, which suggesting that for large V_{ds} the transit time increase across the lengthened gate extension region is overcompensated by the transit time reduction under the shortened effective gate with increasing V_{ds}.

Four different plasma treatments under the gate only were applied to the devices in Group C, including O_2, CF_4, BCl_3, and BCl_3 followed by O_2. It is found that the impact of the gate-only plasma treatment on the device performance, except for the BCl_3-only treatment, is similar to that of DFP – an access-region-only plasma treatment [5], and surprisingly the device rf performance stayed the same when subsequent DFP treatments were applied. An example of CF_4 plasma treatment on HEMTs with gate lengths of ~100 nm is shown in Fig. 3. After the plasma treatment, short channel effects became more severe; threshold voltage shifted by -0.7 V, peak $g_{m,ext}$ increased from 380 to 420 mS/mm; the reverse biased gate leakage dropped by one order of magnitude, and drain induced barrier lowing (DIBL) increased from 50 to 170 mV/V; f_T also increased from 90 to 130 GHz. We thus postulate that the 2DEG density increase after plasma treatment (Table 1) is not the major contributor for the observed electrical gate length reduction. Instead, a conduction path on or near the surface of the HEMT barrier connects the metal gate and the surface states in the virtual gate region; when this conduction path is cut off by the plasma treatment, the electrical gate length is shortened thus the transistor speed improved. The conduction path could be related to N-vacancies that could then be filled by F or O during the plasma treatment [4]. This work has been supported by DARPA-NEXT (John Albrecht, HR0011-10-C-0015), AFOSR (Kitt Reinhardt), AFRL/MDA (John Blevins) and AFOSR-YIP (Kitt Reinhardt).

[1] M. Higashiwaki, et al., *Appl. Phys. Express*, vol. 1, no. 2, p. 021103, 2008.
[2] Nidhi, et al., *IEDM Tech. Dig.*, p. 20.5, 2009.
[3] K. Shinohara, et al., *IEDM Tech. Dig.*, p. 30.1, 2010.
[4] J. W. Chung, et al., *IEDM Tech. Dig.*, p. 30.2, 2010.
[5] R. Wang, et al., submitted to *IEEE Electron Device Lett.*, 2011.

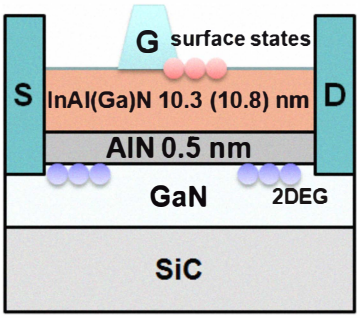

Table 1 Hall transport properties of HEMT structures before and after DFP.

	Before DFP			After DFP		
	R_{sh} (Ω/sq)	n_s (x 10^{13} cm^{-2})	μ (cm^2/ V.s)	R_{sh} (Ω/sq)	n_s (x 10^{13} cm^{-2})	μ (cm^2/ V.s)
InAlN (A)	290	1.62	1330	257	1.86	1300
InAlGaN (B)	227	1.45	1900	190	1.83	1790

Fig. 1 Schematic cross section of D-mode InAl(Ga)N/AlN/GaN HEMTs, showing surface states near the gate.

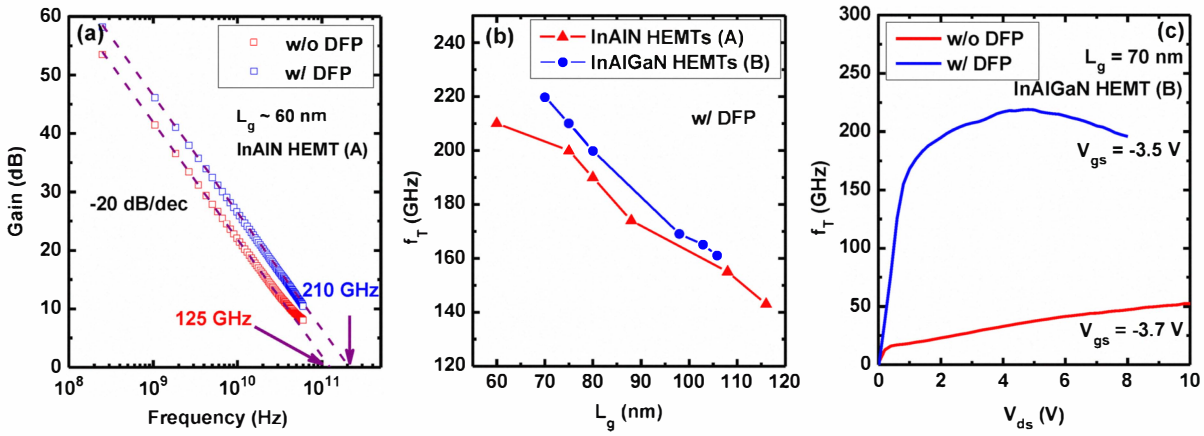

Fig. 2 (a) Current gain as a function of frequency for an InAlN barrier HEMT with L_g = 60 nm and L_{sg} = 400 nm, showing f_T increased from 125 to 210 GHz after DFP. (b) Dependence of f_T on L_g, indicating the scalability of InAlN barrier HEMTs (Group A) and InAlGaN barrier HEMTs (Group B) after DFP. (c) f_T as a function of V_{ds} near peak g_m gate bias of an InAlGaN barrier HEMT with L_g = 70 nm, and L_{sg} = 300 nm, before and after DFP, respectively.

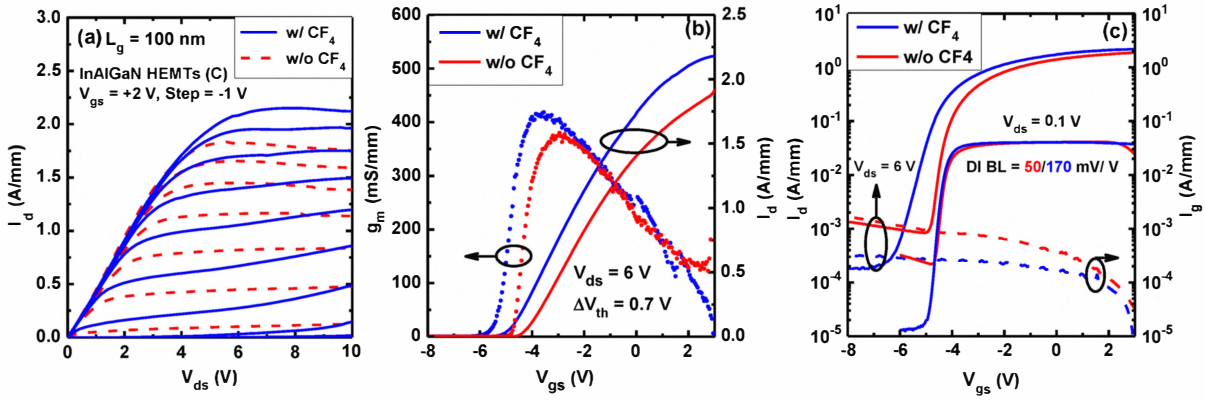

Fig. 3 InAlGaN barrier HEMTs (L_g = 100 nm) with and without CF_4 plasma treatment in the gate region only: (a) common source family of I-Vs; (b) linear-scale transfer characteristics at V_{ds} = 6 V, showing a negative V_{th} shift of 0.7 V and an extrinsic peak g_m increase from 380 to 420 mS/mm; (c) semi-log-scale transfer characteristics at V_{ds} = 6 and 0.1 V, showing CF_4 treatment under the gate reduces the gate leakage while DIBL increased from 50 to 170 mV/V.