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Resonant Clocking Circuits for Reversible Computation

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***Abstract*—A mechanism for the reduction of dynamic energy dissipation in the computing circuit is described. The resonant circuit with controlled switches conserves the stored energy by recovering upto 90% of energy that would be otherwise lost during logic state transitions. This energy-conserving approach preserves thermodynamic entropy, ideally preventing heat generation in the system. This approach is used in a proposed resonant clocking and logic application without dynamic energy dissipation.**

I. Introduction

SCALING semiconductor transistors (MOSFET, HEMT etc.) improves the device performances. These improvements have driven integrated circuit (IC) performance gains for over 40 years. However, static and dynamic energy dissipation have become the main limiting factors for further device scaling in Complementary Metal Oxide Semiconductor (CMOS) circuits [1-4]. This dissipation and the associated heat generation can exceed the limits of practical cooling and impede the scaling of device speed and packing density in ICs [2,5]. Reversible computing can reduce the dissipation to heat, but requires carefully controlled waveforms to obtain low dissipation. This work presents a clocking circuit that can produce the needed waveforms and recycle the energy used to encode information. In particular the circuit enables arbitrary timing of logic transitions.

The field effect transistors (FETs) in CMOS logic are used as switches by controlling the internal potential energy barrier with an applied gate voltage [2,4,6]. The irreversible operation of conventional CMOS destroys the information at each transition, resulting in energy dissipation to heat in the system even with ideal switches (zero I^2R_{on} loss and zero off current) [6-7]. This can be explained by Landauer's Principle. The irreversible logic operation computes single output logic state from many input states (i.e. many inputs to one output mapping). Based on thermodynamic principles, this results in a decrease of entropy in a computing system. According to Landauer, this decrease in entropy must be compensated by an equal or greater amount of entropy increase in a power supply and other parts of the information processing system [7, 8]. This entropy increase generates the large amount of heat in the system, and thus limits the performance. Reversible logic avoids the destruction of information and can therefore reduce the dissipation to heat [6-9].

In order to maintain continuous scaling for terascale integration with CMOS logic, it is necessary to dramatically reduce heat generation by reducing energy dissipation in a computing system [2]. Reusing or conserving the stored energy (used to represent the information) during logic transitions can reduce the heat generation in a computing system. This means that the computing systems in thermodynamic equilibrium with its environment. Reversible computation strictly preserves the thermodynamic entropy. The requirement for implementing reversible logic is to avoid any destruction of information, and to drastically reduce the energy dissipation of all operations in the system so that they approach physical reversibility [9,10].

In this paper, we present an energy conserving resonant circuit with externally controlled FET switches that generates an energy-efficient 'flat-topped' (quasi-trapezoidal) output waveform. This clocked voltage waveform is required for performing digital logic computation in a thermodynamically reversible fashion to recycle the energy from cycle to cycle, and to reduce clock jitter and skew. In addition, we also present a building block for a reversible logic architecture based on a resonant circuit with properly timed input and control signals. This idea has also been used to realize a logic inverter.

II. Ideas and Implementation

A. Conventional CMOS Logic

We first discuss a conventional CMOS inverter shown in Fig. 1(a). When the input voltage is low (logic zero), the output voltage becomes V_{dd} (logic '1') by charging the load capacitor C_L through the PMOS transistor S1. Similarly, for high input voltage with logic '1', the output node is discharged to $-V_{dd}$ level (logic '0') through the NMOS transistor S2. To calculate the energy dissipation, we use a simplified RC model of the logic circuit, shown in Fig.1(b) and (c). For an abrupt transition, analysis of this circuit gives the charging current, $i(t) = (V_{dd}/R_{on}) \exp(-t/R_{on}C_L)$. The energy stored in the load capacitor C_L during the charging phase is,

$$E_{stored} = \frac{V_{dd}^2}{R_{on}} \int_0^\infty e^{-\frac{2t}{(R_{on}C_L)}}\, dt = \frac{1}{2} C_L V_{dd}^2. \quad (1)$$

An equal amount of energy is dissipated as heat in the PMOS transistor. During discharge phase, the stored energy is dissipated in the NMOS transistor switch as heat. In CMOS logic, energy is dissipated during a logic state transition, but, ignoring leakage current, no energy is required to hold the state for logic 1 or logic 0 [6].

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B. Resonant Energy conserving Logic

The dynamic energy dissipation in a computing circuit, that associated with processing information, can be reduced to zero in reversible computation, but the energy used to encode information in the circuit must be recovered and reused. This can be accomplished by incorporating a series resonant circuit to provide energy to, and recover energy from, the logic circuit in a gradual and controlled manner. Fig. 2(a) depicts the schematic of the proposed energy-conserving circuit that generates an output pulse with a sinusoidal ramp at the rising and falling edges. The resonant circuit incorporates a high-Q inductor L_{ER} connected in series with capacitors C_L and C_{ER}, along with switching transistors. Energy is taken from C_{ER} and delivered to the load capacitor C_L during the charging phase and is returned in the discharge phase, as shown in Fig. 2(a). The operation of the proposed circuit for clocking is based on the input control signals and inductor current waveforms shown in the timing diagram of Fig. 3.

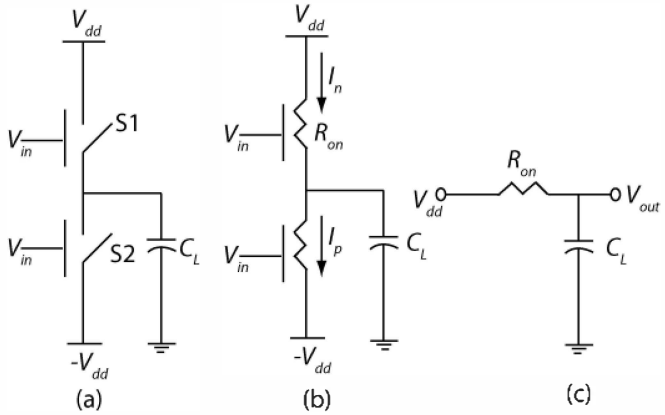

Fig. 1. a) Conventional CMOS logic inverter, b) Resistive models of switching transistors (pull-up & pull-down) in CMOS logic inverter, c) RC circuit model of inverter during logic operation for one-half cycle of input control signal.

The novelty of this approach is the controlled switching operation using transistors in the resonant circuit. This aids the reversible energy transfer between the load capacitor and non-dissipative inductor during logic state transitions. An externally controlled switch S3 controls the energy transfer during each state transition. The other two controlled switches S1and S2 are responsible for holding the output at logic 0 or 1. The capacitor C_{ER} is precharged voltage of $V_{dd}/2$. In the charging phase, the switch S3 is turned on by applying control signal V_{ctr} to the gate of transistor S3 according to timing diagram as shown in Fig. 3. Current flows into the load capacitor C_L and an electromotive force (EMF) is generated in L_{ER}. When the output voltage V_{out} reaches the same potential ($V_{dd}/2$) as the storage capacitor C_{ER}, the EMF of L_{ER} begins to collapse and the current is forced to flow in the same direction through the inductor L_{ER}, forcing the V_{out} to approach V_{dd}. The output voltage of V_{dd} is independent of the values of L_{ER} and C_L in the circuit, and their values serve to control the transition periods of output pulse.

The output voltage V_{out} reaches V_{dd} at the point when the current I_L in the series inductor becomes zero. At this time, the switch S3 is turned off, and the switch S1 is turned on. This holds the output voltage at V_{dd} for finite time, giving the flattop of the output pulse. A small amount of energy will be drawn from V_{dd} through switch S1 to bring the output to the full logic 1, and replenish any energy dissipated in the resonant circuit. In the discharge phase, the switch S3 is turned on while the other switches are turned off.

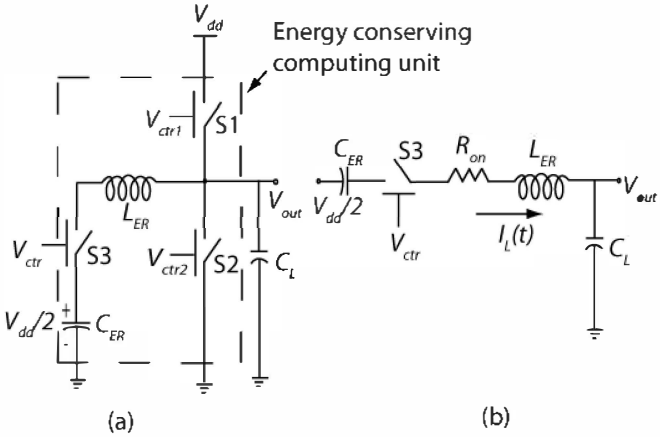

Fig. 2. a) Energy conserving (Reversible) resonant circuit used as a logic computation with ideally zero energy dissipation, b) Series resonant RLC circuit model for Energy conserving computing unit.

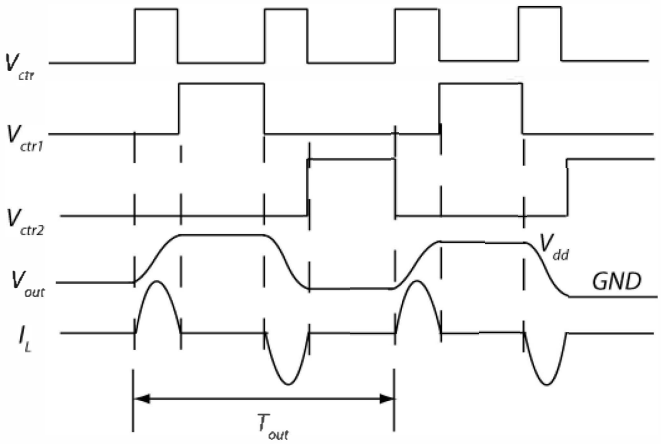

Fig. 3. Timing diagram for generating pulse with finite 'flattop' used for 'Clocking' in reversible computation. The period of clocked waveform can be determined by the designed values of inductance and capacitances in a circuit.

L_{ER}, C_{ER} and C_L again form a series resonant circuit for energy transfer from C_L to the inductor L_{ER} by current flowing out of C_L through L_{ER}. This causes a build up of EMF in L_{ER} in a direction opposite to the charging phase, returning charge to the capacitor C_{ER}. When V_{out} decreases to $V_{dd}/2$, the EMF of L_{ER} collapses and forces the current in same direction through the L_{ER}, forcing V_{out} to reach ground. At this point the current I_L becomes zero and the switch S3 is turned off, and the switch S2 is turned on to hold the output voltage to ground. In this way, the resonant driver with externally controlled switches generates a sequence of output voltage pulse with finite flat tops. This circuit can be used for adiabatic clocking [12,13], and especially 'Bennet clocking' [14] in reversible logic computation. The capacitor C_{ER} is initially charged to $V_{dd}/2$ voltage before

starting the computation. The restoring voltage ($V_{dd}/2$) in the storage capacitor (C_{ER}) is assumed to be stable during charging and discharging of C_L, requiring that the designed value of C_{ER} is larger than that of C_L. Here, the energy recovery capacitor C_{ER} is used as an electrical reservoir, providing energy back and forth to load capacitor C_L, without requiring an additional power supply.

C. Derivation of energy dissipation & Recovery efficiency

The proposed method for conserving the stored energy during digital switching of states is based on an energy recovery mechanism using a series resonant circuit with controlled switching. The switching action of transistor switch S3 controls the flow of current through the circuit, thus gradually storing energy in the inductor. Here the inductor behaves as an "electrical flywheel" assisting the transfer of energy between C_{ER} and C_L. For a practical circuit model, the resistance R_{on} associated with the transistor switch is included with inductance L_{ER}, and capacitances C_{ER} and C_L in the circuit. The resistance in the circuit introduces the damping in the oscillating waveforms, and results in some energy dissipation. In order to calculate energy dissipation, the output voltage ($V_{out}(t)$) and current ($I_L(t)$) flowing through the circuit can also be computed based on the series RLC analysis of the circuit shown in Fig. 2(b). From Kirchhoff's Voltage Law (KVL), we find the relation for voltage as,

$$1/C_{ER} \quad I_L\ t\ dt + I_L R_{on} + L_{ER}\,(dI_L\ dt) + 1/C_L \quad I_L\ t\ dt = V_{dd}\ \ 2, \tag{2}$$

Which leads to second order differential equation for current $I_L(t)$, and can be expressed as,

$$\frac{d^2 I_L(t)}{dt} + \frac{R_{on}}{L_{ER}}\frac{dI_L(t)}{dt} + \frac{C_L + C_{ER}}{C_L C_{ER}}\frac{I_L(t)}{L_{ER}} = 0. \tag{3}$$

By using initial conditions for current and output voltage of $I_L(0)=0$ and $V_{out}(0)=V_{dd}/2$ at $t=0$, the solution for transient current $I_L(t)$in eq. 3can be written as [10],

$$I_L\ t\ = \frac{V_{dd}}{2} C_L \frac{\omega_0^2}{\omega_d} e^{-\alpha t}\, sin(\omega_d\, t), \tag{4}$$

Where $\alpha=R_{on}/2L_{ER}$ is the attenuation frequency, $\omega_d = \sqrt{\omega_0^2 - \alpha^2}$ is the angular frequency of oscillation and $\omega_0 = 1/\sqrt{(L_{ER}C_{tot})}$ is a resonant frequency with total capacitance,$C_{tot} = C_L C_{ER}/(C_L + C_{ER})$. Finally, the output voltage $V_{out}\ t\ = \ 1/C_L \quad I_L\ t\ dt$is calculated by [10],

$$V_{out}\ t\ = \frac{V_{dd}}{2} e^{-\alpha t}\ \ cos(\omega_d\, t) + \frac{\alpha}{\omega_d} sin(\omega_d\, t)\ . \tag{5}$$

Without switches S1 and S2, the output voltage is oscillating with a frequency ω_d for the under damped condition ($\alpha < \omega_0$) met by an appropriate choice of the lumped parameters of L_{ER}, C_L, and C_{ER} in the energy conserving computing circuit. The output waveform of the series resonant circuit combines with S1 and S2 to generate a 'flat-topped' (quasi-trapezoidal) energy-efficient final output pulse at each rising and falling edges. The resistive losses associated in the circuit can be calculated from $I_L^2 R_{on}$ in the switches to find in energy dissipation. Using eq. 4, the energy dissipation per complete cycle of oscillation can be expressed as $2\int_0^{\pi/\omega_d} I_L^2(t) R_{on}\ dt$[10] which calculates to,

$$E_{diss} = \frac{1}{4} C_L V_{dd}^2.\ 1 + \frac{C_L}{C_{ER}}\ .\ 1 - e^{-\frac{2\pi\alpha}{\omega_d}}\ . \tag{6}$$

Fig. 4 plots the energy dissipation as a function of inductance, L_{ER}, for different values of series on-resistances, R_{on}, with conventional abrupt switching and energy recovery resonant switching. The dissipation is smaller for resonant switching as compared to conventional abrupt switching. At resonance, the inductive reactance is used to cancel the capacitive reactance, resulting in a reduction of energy dissipation and improvement of the phase stability (reducing skew and jitter in clock period) of the output clocking waveform.

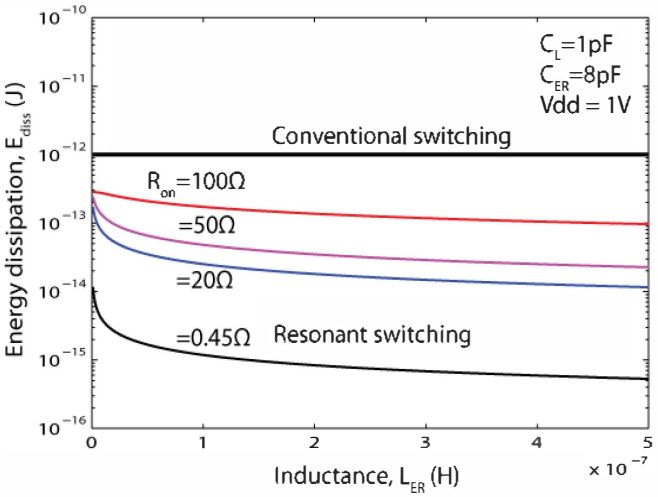

Fig. 4. Energy dissipation as a function of inductance for various values of series on-resistances, Ron, load and energy recovery capacitances, C_L and C_{ER}, assumed in the computing circuit. Energy dissipation is higher for conventional abrupt switching than for resonant switching with energy recovery mechanism. For resonant switching, energy dissipation is smaller for smaller values of R_{on}.

A figure of merit for a computing circuit can be defined as the energy recovery efficiency $\eta_{rec}=[E_{stored} - E_{diss}]/E_{stored} \times 100\%$. For conventional CMOS with no energy recovery mechanism, the stored energy in the load capacitor C_L during charging phase is completely lost as heat in the switching transistor during discharging phase, resulting in $E_{stored}= E_{diss}$ and recovery efficiency of $\eta_{rec}= 0\%$. Using resonant switching, in a lossless high-Q circuit asymptotically recovers all the energy leading to $E_{diss}=0$ and $\eta_{rec}= 100\%$. Practically, there is resistive loss (i.e. $I_L^2 R_{on}$) in the switches, leading to some dissipation. Using eq. 6, the energy recovery efficiency η_{rec} taking into account the resistive loss, can be calculated by,

$$\eta_{rec} = 1 - \ 1 + \frac{C_L}{C_{ER}}\ .\ 1 - e^{-\frac{2\pi\alpha}{\omega_d}}\ , = 1 - \frac{1}{4}\ \ 1 + \frac{C_L}{C_{ER}}\ \ \ 1 - e^{-\frac{2\pi R_{on}\ \sqrt{C_{tot}}}{\sqrt{4L_{ER} - R_{on}^2 C_{tot}}}} \times 100\%. \tag{7}$$

The energy recovery efficiency depends on the lumped components in a computing circuit. In order to achieve high recovery efficiency, the resistive losses should be minimized by incorporating high precision switches with very low on resistance and high-Q lossless inductor. The quality of an

inductor is measured by a quality factor Q, which represents the amount of energy stored in the form of magnetic field to the amount of energy dissipated in an inductor per cycle [15,16]. The value of Q is limited by energy loss due to parasitics in the inductor. In order to obtain a high Q value of inductor, the values of parasitics (resistance and capacitance) in the inductor have to be lowered.

D. Design of energy recovery system & calculation of energy recovery efficiency

The energy recovery circuit is designed for a technology with fixed resistance associated with a transistor switch and load capacitance. The inductance L_{ER} can be adjusted to form a series resonant circuit at a required frequency of operation with minimum energy loss. In the circuit of Fig.2, the only component that dissipates energy is the transistor switch. The calculated energy dissipation in eq. 5 has included the non-zero on resistance of MOS switch. The resistance of an N-channel MOSFET, $R_{on} = V_{ds}/I_d$, operating in linear region (i.e. $V_{ds} << V_{gs} - V_t$ for quasi-static switching) is given by [10,11],

$$R_{on} = \frac{L^2}{\mu_n c_0 \ Vgs - Vt}, \quad (8)$$

Where L is the channel length of MOS transistor, μ_n is the effective carrier mobility in the channel, $c_0 = WLc_{ox}$ is the gate capacitance, W is the channel width of transistor and c_{ox} is the oxide capacitance. For a typical 50nm node, the gate overdrive voltage (V_{gs}-V_t)~1V, μ_n=500cm^2/V.S, L=50nm, W=100um and $c_0 = 100\times10^{-6}*50\times10^{-9}*3.9*8.85\times10^{-12}/1.5\times10^{-9} = 1.1\times10^{-13}$ F with 1.5nm gate oxide thickness, the on-resistance calculated by eq. 8 gives R_{on}=0.45Ω. The load capacitance C_L in the circuit is assumed to be 1pF. From the analysis of output voltage and current waveforms of resonant circuit in equations 5 and 4, for under-damped or critically damped condition, ω_d increases as L_{ER} decreases up to a maximum, $\omega_{dmax} = 1/R_{on}C_{tot}$, and then decreases, thus requiring the value of minimum inductance, $L_{ER,min}$, in the circuit is $L_{ER,min} = R_{on}^2 C_{tot}/2$. For designing of energy recovery resonant circuit, the inductance (lossless high-Q factor) value should be larger than the $L_{ER,min}$, thus providing underdamped oscillation and recovers most of the energy. From the circuit analysis, the energy dissipation due to charging and discharging the gate of two transistor switches in a conventional logic gate is equal to $C_L V_{dd}^2$. By incorporating resonant energy conserving mechanism, the restored energy in the energy recovery capacitor C_{ER} with $V_{dd}/2$ forcing voltage is equal to $(1\ \ 8)\, C_{ER} V_{dd}^2$. From these two relations, the value of C_{ER} should at least be 8× larger than C_L ($C_{ER} \geq 8C_L$) in order to maintain stable $V_{dd}/2$ forcing voltage in the C_{ER} during switching. Using eq. 6, and assuming the values of C_L=1pF, C_{ER}=8pF and R_{on}=0.45Ω, 20Ω, 50Ω, the energy recovery efficiency η_{rec} is calculated and plotted with inductance L_{ER} with values in the range of 1 to 500nH. The results are shown in Figs. 5 and 6. In Fig. 5, it is shown that the energy recovery efficiency is higher (closed to 100%) for R_{on}=0.45Ω, while the efficiency is reduced with increasing R_{on} (because of more resistive losses). More than 90% of the energy can be recovered for resonant switching at proper designing conditions. The operating conditions for circuit design can be optimized at L_{ER}=1-20nH with fixed load capacitance, C_L for a technology, generating an energy-efficient GHz clock pulse. Fig. 6 shows the plot of energy recovery efficiency as a function of inductance for different values of C_{ER} at R_{on}=10Ω and C_L=1pF. The recovery efficiency remains constant for the values of energy recovery capacitor C_{ER} =8, 20, 30 and 50pF (our predicted designed value $C_{ER} \geq 8C_L$), with little reduction even at value of C_{ER}=4pF. For C_{ER}=0.1pF (i.e. $C_{ER} < C_L$), the recovery efficiency is reduced. From the analysis and Fig. 6, the designed value of energy recovery capacitor C_{ER} can be optimized to $C_{ER} \geq 8C_L$ in order to maintain high recovery efficiency and stable $V_{dd}/2$ voltage during logic operation.

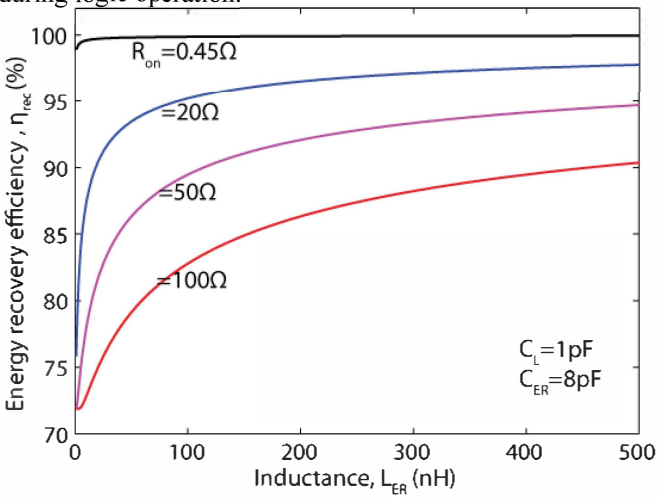

Fig. 5. Energy recovery efficiency as a function of inductance for different values of series on-resistances, Ron, load and energy recovery capacitances, C_L and C_{ER}, in the computing circuit. Recovery efficiency is higher for smaller values of R_{on}.

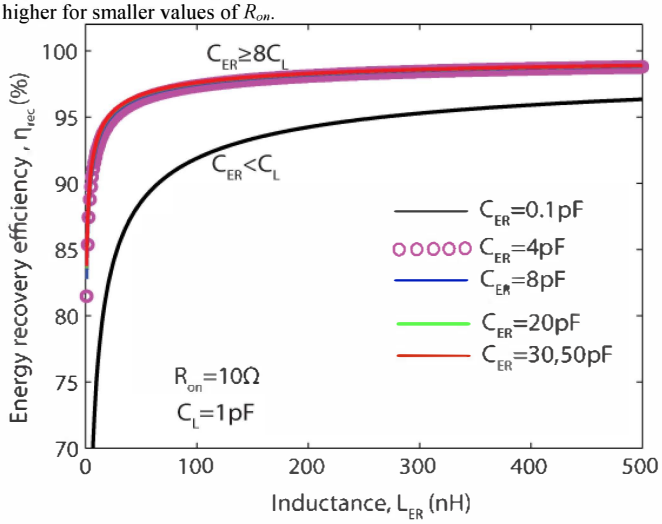

Fig. 6. Energy recovery efficiency as a function of inductance for different values of energy recovery capacitances, C_{ER}=0.1, 4, 8,20,30,50pF at R_{on}=10Ω and C_L=1pF in the computing circuit. Recovery efficiency remains constant for C_{ER}= 8, 20, 30 and 50PF (i.e. $C_{ER} \geq 8C_L$).

The inductor in a resonant circuit can physically be realized as the distributed spiral thick metal layers in an on-chip [15-18]. Using the value of on-chip spiral inductor of L_{ER}~7.4nH (with Q ~ 6.76, total parasitic resistance, R_p~15kΩ, and capacitance, C_p~1.3pF) at 1GHz frequency

[15], 71% of the energy can be recovered based on our energy recovery circuit and its analysis. A high-Q (low parasitic loss) inductor is required for operating this energy recovery circuit with high recovery efficiency. An off-chip discrete inductor with high-Q can also be used to generate resonant clocking pulse.

III. Building Block For Reversible Logic Architecture And Realization of Logic Inverter

In addition to clocking circuits, this approach can be applied to logic gates. Figs. 7(a) and (b) show a schematic of a resonant logic inverter with control signals. Fig. 7(c) shows the building block for reversible logic architecture with corresponding input, output and special control signals. This whole block can be considered as a reversible state machine for performing logic operation in an ASIC (Application Specific Integrated Circuit) design style. In the state machine block diagram, the output logic states (O_0, O_1,….,O_n) are generated by Boolean algebraic operation on input logic states (I_0, I_1,….,I_n). Based on these input and output bits, the special control signals (V_{ctr3}, V_{ctr4}, V_{ctr5}) are generated to provide timing signals to the resonant energy conserving computing unit that results in low energy dissipation.

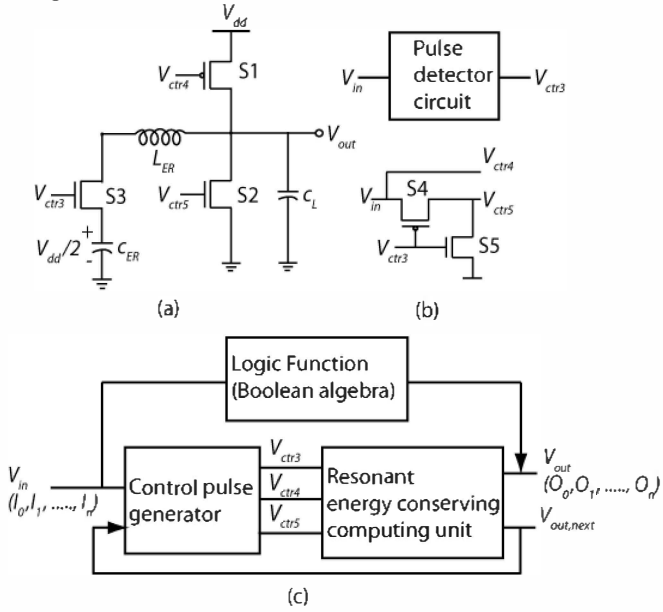

Fig. 7. a), b) Schematic of logic inverter and control signals generation from input logic pulse, c) Building block for reversible logic architecture with input, output and control logic pulses (considered as a state machine). Generation of special control signals (V_{ctr3}, V_{ctr4} and V_{ctr5}) should be correlated with input and output logic bits.

Operation of the inverter uses the control signals as shown in the timing diagram of Fig. 8. Control pulses (V_{ctr3}, V_{ctr4} and V_{ctr5}) are correlated with the input and output logic pulse as shown in Fig.8. V_{ctr3} is the sequence of pulses that triggers the rising (0→1) and falling (1→0) edges of the output logic pulse, can be generated by a standard pulse detector circuit. V_{ctr4} and V_{ctr5} are generated by input V_{ctr3} using the circuit in Fig. 7(b). The control pulse, V_{ctr4}, is the same as input logic pulse that controls the gate of PMOS switch S1. At T1, T3, T5, and T7, the PMOS switch S1, and NMOS switch S2, are turned off, while NMOS switch S3 is turned on for resonant energy transfer during logic transitions. In Fig.(8), at T2, T6, the switch S2 is turned on for holding an output to logic "0" (ground), while the other switches, S1 and S3 are turned off. Similarly, at T4, the PMOS switch, S1 is turned on to hold V_{out} to logic 1 (V_{dd}), while other switches, S2 and S3 are turned off. In this fashion, the logic gate generates an output logic pulse V_{out}, which is an inverse function of the input logic pulse as shown in Fig. 8.

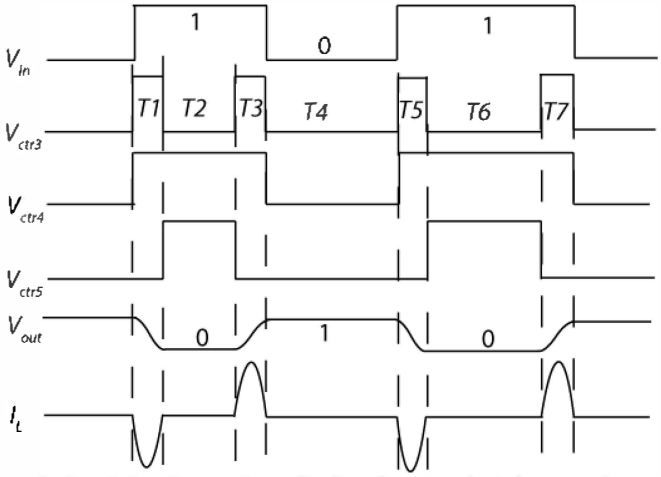

Fig. 8. Timing diagram for realization of resonant logic inverter without dynamic energy dissipation ideally or very low power dissipation for logic computation.

IV. Conclusion

In summary, an energy recovery mechanism based on a resonant circuit with controlled switching during logic transitions is presented. This method is used for conserving the stored energy during switching of states, thus aiding computation in thermodynamically reversible fashion with asymptotically zero energy loss. The proposed resonant circuit with FET switches generates a "flat-topped" output waveform, which is needed to enable low energy, reversible, computation. We also derived the energy recovery efficiency and showed that more than 90% of energy can be recovered by resonant switching with proper design of the circuit. In addition to low energy clocking waveform generation, this approach can be applied to logic gates. Special control signals with proper timing are required to realize the logic gates. Additionally, this energy efficient switching approach can also be applied to high voltage drive circuitry used in consumer electronics, such as field emission displays, Liquid crystal displays (LCD) backlighting driving, and the interfacing of a circuit to the external world.

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