# Ultrathin Body GaN-on-Insulator Quantum Well FETs With Regrown Ohmic Contacts

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***Abstract*—A technology similar to silicon-on-insulator is highly desirable for III–V electronics to support scaling for future generations. This letter reports the first realization of strained GaN quantum-well transistors embedded in unstrained AlN as the insulator. The molecular beam epitaxy (MBE)-grown heterostructure consisting of an ultrathin GaN channel buried in strain-free AlN barriers is favorable for scaling by the suppression of short-channel effects. Ohmic contacts are realized with MBE-regrown heavily Si-doped $n^+$ GaN. For long-channel devices, a saturation drain current of ∼0.7 A/mm at $V_{GS} = +3$ V and a peak extrinsic transconductance of ∼160 mS/mm around $V_{GS} = +1$ V are measured at $V_{DS} = +10$ V. No hysteresis is observed in the $C$–$V$ measurement, indicating the high quality of all binary nitride heterostructures. The demonstrated device structure offers a high promise for high-frequency and high-power applications in the future. The strain-free barrier has the potential to enhance the reliability of GaN transistors.**

***Index Terms*—Aluminum nitride (AlN), gallium nitride, molecular beam epitaxy (MBE), quantum well (QW), transistor, ultrathin body (UTB).**

## I. Introduction

SCALING requirements of silicon CMOS technology have driven the need for ultrathin body (UTB) in many forms. The recent advances in Si FinFETs and UTB silicon-on-insulator (SOI) devices offer ways for the tight electrostatic and quantum confinement of charge carriers to nanoscale dimensions. This is necessary for short-gate-length devices to prevent the degradation in performance by a slew of short-channel effects including drain-induced barrier lowering (DIBL), subsurface punchthrough, etc. Such methods are highly desirable for III–V semiconductors. Although amorphous dielectrics such as $SiO_2$ and high-$\kappa$'s have served this drive in silicon, the III–V semiconductors, particularly GaN, offer great benefits in using epitaxial wide-bandgap "dielectrics" such as aluminum nitride (AlN). AlN is an ideal building block for group-III nitride electronics. To better meet the scaling requirement of inducing high 2-D electron gas (2DEG) density with minimum barrier thickness, the large polarization charge of AlN is highly desired. Its wide direct bandgap (∼6.2 eV) can keep the gate tunneling leakage current low. With its wide bandgap and large band offsets, AlN provides the maximal carrier confinement for nitride channels of all compositions both as a top and back barrier to suppress short-channel effects. The high thermal conductivity of 3.4 $W/(cm \cdot K)$ [1] enables excellent heat dissipation. This is a major advantage over SOI-type structures, where the "insulator" layer is both electrically and thermally insulating. AlN is an excellent electrical insulator but, simultaneously, an excellent thermal conductor by virtue of the light masses of Al and N atoms [2]. Given that heat dissipation is a major challenge in current electronics, AlN substrates provide an attractive alternative. GaN-based high-electron mobility transistors (HEMTs) have made significant progress [3], [4], and AlN offers new paradigms in device design to further boost the device performance.

There have been reports on thick ($> 50$ nm) GaN channel HEMTs on AlN [5], [6] where the GaN channels were relaxed. In N-polar GaN HEMTs, AlN has been used to induce the 2DEG and as a back barrier [7]. In this letter, we report the device performance of UTB GaN quantum-well (QW) field-effect transistors (FETs) on AlN with regrown ohmic contacts. The active device layers comprise of ultrathin ($< 25$ nm) GaN channel sandwiched between two AlN layers. Analogous to SOI or compound semiconductor-on-insulator [8] technology, GaN sits strained on wide-bandgap AlN. The large conduction band offset between GaN and AlN as well as the high built-in polarization-induced electric field confines carriers inside the GaN QW. All nitride layers in the heterostructures are binary, eliminating the effect of alloy scattering. However, the method presented here lends naturally to the integration of ternary or even quaternary channels in the future. The GaN channel is strained, which allows thick unstrained AlN barrier layers. This is highly attractive for improving the device reliability since device degradation has been linked to the strain relaxation and crystallographic defect formation in the barrier layers [9]. High-quality ohmic contacts are possible by molecular beam epitaxy (MBE) regrowth, as seen in the ultralow ($\leq 0.1\ \Omega \cdot$ mm) contact resistance for wide-bandgap AlN barrier HEMTs [3]. Such low contact resistances are beyond the reach of conventional alloyed ohmic contacts. The choice of regrown materials (for example, AlGaN or InGaN) provides an additional freedom of adjusting the strains in the GaN QW, particularly for

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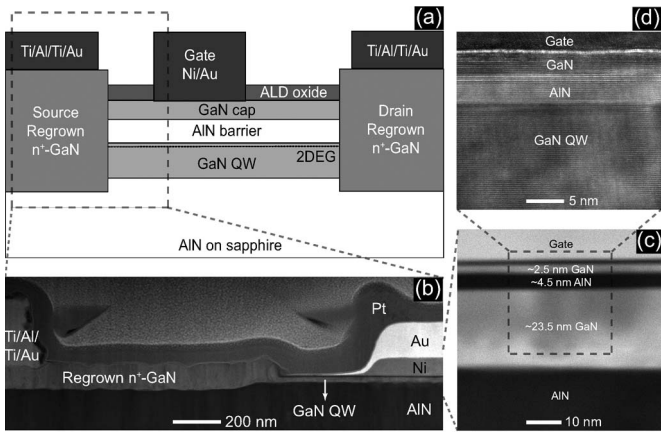


Fig. 1. (a) Schematic of device structures (not to scale). (b) Z-contrast STEM image of gate-to-source regions, showing regrown GaN connected to the GaN QW channel. (c) Z-contrast STEM image of active layers under the gate, resolving the sharp interfaces between binary III nitrides. (d) HRTEM image of top AlN/GaN QW interface at the 2DEG channel region.

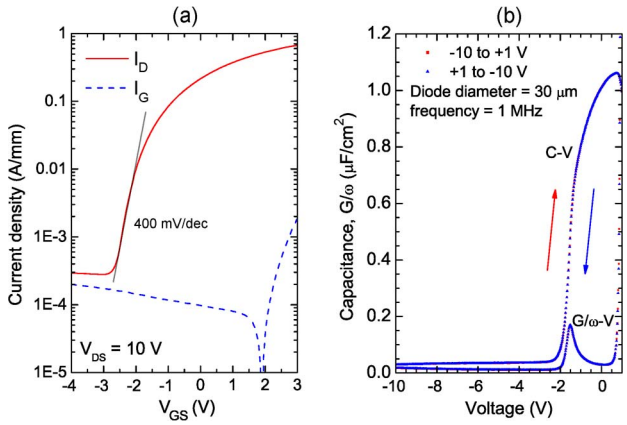


Fig. 2. (a) Semilog plot of transfer characteristics and gate current for a GaN QW device with $L_g = 2.1$ $\mu$m at $V_{\rm DS} = 10$ V. (b) $C$–$V$ and $G/\omega$–$V$ plots of a circular Schottky diode measured at 1 MHz, showing no hysteresis.

self-aligned devices. This letter presents the first demonstration of a strained GaN QW FET on AlN.

## II. Experiments

The nitride heterostructures used here were grown on $\sim$ 1-$\mu$m-thick semi-insulating metal-polar AlN templates on sapphire by MBE in a Veeco Gen 930 system. As shown in Fig. 1(a), a 210-nm-thick unintentionally doped AlN buffer was epitaxially grown, followed by a $\sim$23-nm GaN QW channel. Then, a $\sim$4.5-nm-thick AlN barrier layer was grown and capped with a $\sim$2.5-nm-thick GaN layer. The full-width at half-maximum of the AlN (0002) peak is $\sim$80 arcsec, obtained from an X-ray diffraction rocking curve measurement. The resultant surface (not shown) exhibits a smooth morphology, with $\sim$0.5-nm rms roughness for $10 \times 10$ $\mu$m$^2$ regions. The sheet resistance of the As-grown structures measured at room temperature (RT) by Hall effect is $\sim$ 1250 $\Omega/\Box$, with a 2DEG density of $\sim 1.77 \times 10^{13}$ cm$^{-2}$ and a mobility of $\sim$280 cm$^2$/V $\cdot$ s. We note that although the carrier mobility is low at this point, it is projected to improve significantly with a better epitaxial control, for example, by increasing the growth temperature and growth rate. The 2DEG density is lower than what is achieved with the same top barriers ($\sim$4.5-nm AlN and $\sim$2.5-nm GaN cap) for AlN/GaN heterostructures grown on GaN substrates. This is consistent with the fact that on an AlN substrate, the GaN QW is under in-plane compressive strain and the piezoelectric polarization *opposes* the spontaneous polarization field. The negative polarization charge at the bottom GaN/AlN interface may also cause depletion of the 2DEG.

For ohmic contacts, we have employed a regrowth process [10]. A $\sim$280-nm-thick $SiO_2$ mask was deposited, and the nitride regrowth regions were etched for $\sim$40 nm. The regrowth of a $\sim$120-nm-thick heavily Si-doped ($\sim 1 \times 10^{20}$ cm$^{-3}$) n$^+$ GaN was performed in the MBE system. Ti/Al/Ti/Au ohmic metal stacks were deposited and annealed at 600 °C for 10 min in $N_2$ ambient. Ni/Au (80/160 nm) gate metal stacks were deposited, followed by $Al_2O_3/HfO_2$ (1/6 nm) surface passivation for access regions using atomic layer deposition (ALD). Low-$\kappa$ materials would be used for passivation in the future. After the passivation, a sheet resistance of $\sim$ 1700 $\Omega/\Box$, a channel mobility of $\sim$ 210 cm$^2$/V $\cdot$ s, and a 2DEG density of $\sim 1.73 \times 10^{13}$ cm$^{-2}$ were obtained by the RT Hall-effect measurement. The device dimensions measured using scanning electron microscopes are as follows: $W_g/L_g = 49.5/2.1$ $\mu$m and $L_{\rm gs}/L_{\rm sd} = 0.4/6.9$ $\mu$m, where $L_{\rm sd}$ is defined by the regrown n$^+$-GaN edges. The devices were then electrically characterized and thereafter used for cross-sectional imaging to reveal the layer structure and geometrical details.

## III. Results and Discussion

A uniform transition from the regrown n$^+$-GaN ohmic regions to the GaN QW channel is observed in the Z-contrast scanning transmission electron microscopy (STEM) image of the gate-to-source regions in Fig. 1(b). The n$^+$ GaN grown over the slanting sidewall of the etched nitrides forms the raised source and drain contacts, which is highly desirable for high-performance devices [11]. The GaN QW confined by double AlN barriers is clearly resolved by the Z-contrast STEM image of active layers under the gate in Fig. 1(c). The $\sim$2.5-nm-thick GaN cap was used to protect the AlN surface from oxidation. The dark line (low-average atomic mass) on top of the GaN cap may be related to the oxygen plasma treatment process prior to gate metal deposition, although we have not been able to confirm its precise origin. Energy-dispersive X-ray spectroscopy analysis confirmed that all nitrides are binary and no grading of the Al composition was observed. The high-resolution TEM (HRTEM) image of the top AlN/GaN QW interface is shown in Fig. 1(d), resolving the smooth interface at the 2DEG channel region.

Fig. 2(a) shows the transfer characteristics of a long-channel ($L_g = 2.1$ $\mu$m) GaN QW FET device with $V_{\rm DS} = 10$ V. The device pinched off at $V_{\rm GS} = -2.4$ V with the criteria of $I_D^{\rm off} \leq 1$ mA/mm. A DIBL value of $\sim$40 mV/V is extracted for $V_{\rm DS} =$ 0.5 and 10 V at $I_D = 10$ mA/mm, showing long-channel characteristics. Owing to the large conduction band offset between AlN and GaN, the AlN top barrier is capable of sustaining a high forward $V_{\rm GS}$ bias and enables a low leakage current. The buffer leakage is $\sim$0.5 mA/mm at 15 V, and the subthreshold slope is $\sim$400 mV/dec, which may result from unintended

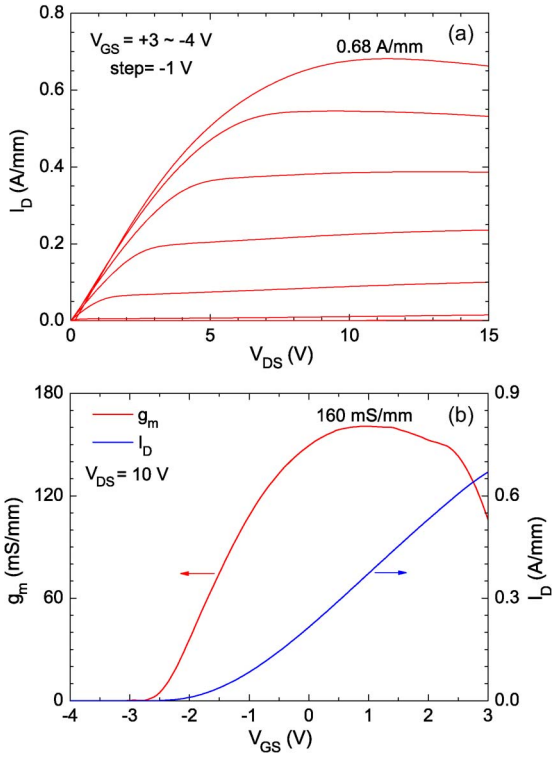


Fig. 3. (a) Output characteristics of a GaN QW device with $L_g = 2.1$ $\mu$m. (b) Transfer characteristics at $V_{\rm DS} = 10$ V.

dopants and traps in nonoptimal buffer layers. Fig. 2(b) shows the capacitance–voltage ($C$–$V$) curves measured at 1 MHz for a circular Schottky diode with a diameter of 30 $\mu$m for the gate stack shown in Fig. 1(c). Corresponding conductance/angular frequency ($G/\omega$) plot shows that the Schottky diode turns on around +0.6 V and the conductance increases [12]. No measureable hysteresis is observed, indicating the high quality of the nitride interfaces.

As shown in the family of $I$–$V$ curves of the 2.1-$\mu$m-long device in Fig. 3(a), the saturated drain current at $V_{\rm GS} = +3$ V reaches ~0.68 A/mm. An on-resistance $R_{\rm on}$ of ~8.7 $\Omega \cdot$ mm is extracted at $V_{\rm GS} = +2$ V, consistent with the long channel and high resistance of the structure. The $R_{\rm on}$ of ~12.3 $\Omega \cdot$ mm at $V_{\rm GS} = 0$ V, combined with the sheet resistance of ~1700 $\Omega/\square$ and $L_{\rm sd}$ of 6.9 $\mu$m, gives an upper limit of ~0.3 $\Omega \cdot$ mm for the contact resistance. The Ni/Au Schottky contacts at $V_{\rm GS} = 0$ V induce more depletion of the 2DEG under the gate than the ALD-passivated surface of the van der Pauw cross bridges. The transfer characteristics of the device in linear scale are shown in Fig. 3(b). The extrinsic transconductance peaks at ~160 mS/mm with $V_{\rm DS} = 10$ V. The pinchoff characteristic is consistent with the $C$–$V$ measurement in Fig. 2(b).

## IV. Conclusion

In conclusion, this letter has reported the first demonstration of UTB-strained GaN QW HEMTs with regrown ohmic contacts. A saturation drain current of ~0.7 A/mm at $V_{\rm GS} = +3$ V with the peak extrinsic transconductance of ~160 mS/mm around $V_{\rm GS} = +1$ V is measured for a device with $L_g = 2.1$ $\mu$m and $V_{\rm DS} = 10$ V. $C$–$V$ measurement indicates the high quality of nitride interfaces. Although the device performance lags current state-of-the-art GaN HEMTs, it is important to note that this is the first realization of a novel device structure that offers substantial opportunities for scaling. By scaling down the thicknesses of the GaN QW and/or top AlN barrier, an enhancement-mode operation can be a natural outcome in a self-aligned device. The AlN back barrier is the highest achievable in GaN devices and, at the same time, enhances heat dissipation compared to other competing back-barrier technologies that use the alloys of InGaN or AlGaN. The QW channel composition can be scaled to a lower bandgap (InGaN) for high speed, or to a higher bandgap (AlGaN) for high-breakdown devices. For reaping the most benefit, the whole device structure needs to be ported to a bulk AlN substrate. This report is intended to demonstrate the feasibility toward achieving these goals.

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