Perspectives of TFETs for low power analog ICs

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***Abstract*— In this paper we show that tunnel field effect transistors (TFETs) biased in the subthreshold region promise several advantages for low-power/high-frequency analog IC applications (e.g. GHz operation with sub-0.1 mW power consumption). Analytical and TCAD models for graphene nano-ribbon (GNR) and InAs/GaSb nanowire TFETs are employed, respectively, for the first time in subthreshold analog circuit examples using the g_m/I_d integrated circuit (IC) design technique. From comparison of these TFET technologies with traditional FETs it is observed that due to the higher currents per unit gate width at low voltage for TFETs, smaller, higher speed, and lower power analog circuits are enabled.**

***Index Terms*— TFET, low-power electronics, analog circuits, sub-threshold, design space exploration, graphene.**

I. Introduction

Although there is significant research dealing with the advantages of TFETs for digital circuits [1], the benefits of employing these devices in analog applications, besides the possibility of operating at lower V_{DD} (< 0.1 V), have remained largely unexplored until recently [2]. Low power circuit design often requires transistors to operate in the regions where they are more efficient as generators of transconductance hence bandwidth, i.e. in the subthreshold region [3]. In this context, a usual parameter of interest for analog IC designers is the g_m/I_d ratio [4]. Due to the possibility of achieving < 60 mV/decade subthreshold swing [1], [5], TFETs can outperform traditional FETs in transconductance generation efficiency; the g_m/I_d ratio in traditional FETs is theoretically limited to $< 1/nU_t < 38.5$ V^{-1} at room temperature (where n is the subthreshold slope factor and U_t the thermal voltage), whereas TFETs promise $g_m/I_d >>$ 100 V^{-1}. Using two example circuits: an intrinsic amplifier and a Miller operational transconductance amplifier (OTA) [6], the promised performance of two TFET technologies (GNR nano-ribbon and InAs/GaSb nano-wire based) for low power analog applications is compared and discussed.

II. TFETs

III. Shown in Fig. 1 is a schematic device cross section and a pair of energy band diagrams illustrating the operation principle of the *p*-TFET. With zero volts applied to the gate the transistor is off (Fig. 1b), the channel is fully-depleted so that tunneling from source to channel is prohibited. With negative voltage applied to the gate (Fig. 1c) electrons can tunnel from source to channel. Since the current turn-on mechanism in TFETs is by interband tunneling rather than by thermionic emission as in traditional FETs, the subthreshold swing is not limited to 60 mV/decade at room temperature.

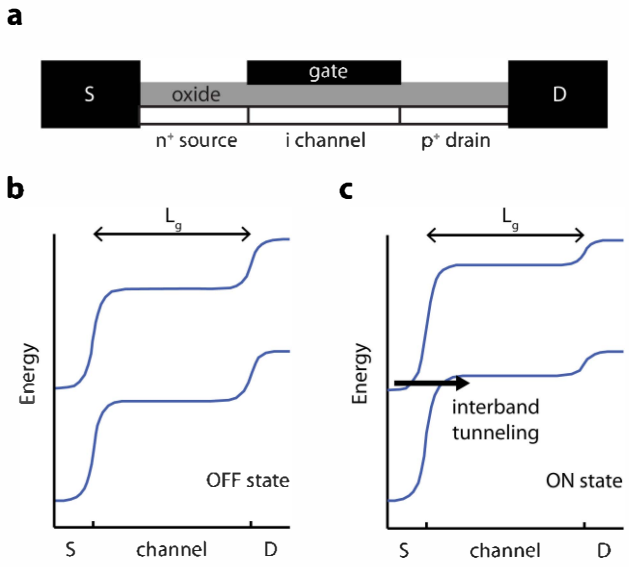

Fig. 1. Cross section of a GNR TFET (a) and energy band diagram when the device is biased in (a) ON and (b) OFF-state. Figure adapted from [5].

GNR TFETs were simulated as in [5] with gate lengths of 20 and 15 nm, ribbon widths of 3 and 2 nm, and 0.6 and 0.5 nm equivalent-oxide thickness (EOT). InAs/GaSb nanowire TFETs with 15 nm gate-length, 0.6 nm EOT, and 3.5 nm diameter were simulated using Synopsis TCAD. In analogy to traditional FETs, the g_m/I_d ratio was found to be weakly dependent on V_{ds} for a fixed V_{gs} (figure not shown), which allows for the use of the g_m/I_d design methodology [4]. Shown in Fig. 2a is g_m/I_d as a function of current per unit width $J_d = I_d/W$ for the analyzed TFET technologies, and several MOSFET and FinFET technologies [7], [8]. GNR TFETs should provide superior current drive relative to other TFET technologies. Moreover, as also pictured in Fig. 2a, the subthreshold region current densities in the GNR TFETs for a given g_m/I_d ratio are larger than those attainable in comparable

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gate length traditional FETs (e.g. 22-nm Si MOSFET technology [7]).

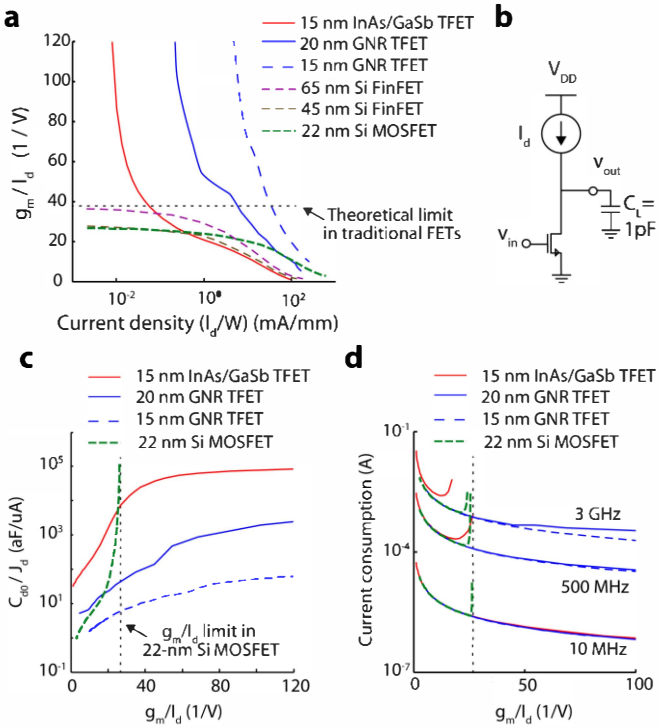

Fig. 2. (a) g_m/I_d as a function of drain current density. (b) Schematic circuit of an intrinsic amplifier. (c) C_{d0}/J_d as a function of g_m/I_d. (d) Current consumption versus g_m/I_d for different target gain-bandwidth product (GBW) values in an intrinsic amplifier (C_L = 1pF is assumed)

IV. Example Circuits

A. Intrinsic Amplifier

An intrinsic amplifier, consisting of a current biased transistor in a common source configuration loaded by a capacitance C_L, is shown in Fig. 2b [4]. In this configuration, the current consumption (as a function of the transistor g_m/I_d) can be expressed as:

$$I_d = \frac{2\pi \times GBW \times C_L}{\frac{g_m}{I_d} - 2\pi \times GBW \times \frac{C_d}{J_d}}, \qquad (1)$$

where gain-bandwidth product (GBW) and C_L are set by the design requirements, and J_d and C_{d0} are functions of g_m/I_d (see Fig. 2a and 2c). C_d is defined as the capacitance seen from the transistor drain to ground in the absence of load capacitance (i.e. the capacitance that adds to C_L), and $C_{d0} = C_d/W = (C_{gd}+C_{bd})/W$ in traditional FETs (where C_{bd} is the bulk-to-drain capacitance) and approximately equal to C_{gd0} in TFETs (where C_{gd0} is the gate-to-drain capacitance per unit width).

When comparing current consumption for intrinsic amplifiers employing the two TFETs and the 22-nm Si CMOS, it is observed (Fig. 2c) that for low GBW requirements (e.g. 10 MHz) both TFETs promise lower current consumption than the CMOS because of the possibility of operating TFETs in the subthreshold region with very large g_m/I_d (>38.5 V^{-1}). Under this constraint of low GBW, the second term of the denominator in Eq.(1) is small so current consumption is a monotonically decreasing function of g_m/I_d. Thus, the most power efficient technologies are the ones able to achieve the largest g_m/I_d.

The current consumption increases with increasing GBW (Fig. 2b). For high GBW (i.e. 3 GHz), the key to minimize current consumption is to employ a technology with high g_m/I_d while keeping C_{d0}/J_d as low as possible, as dictated by the denominator of Eq. (1). To this end, we plot C_{d0}/J_d vs. g_m/I_d in Fig. 2c for various transistor technologies, where the advantages of the GNR TFET become more evident. In this case, for a given g_m/I_d, because of the larger attainable J_d in the GNR TFET, the second term in the denominator of Eq. (1) is smaller for the GNR TFETs even though TFETs tend to higher C_{gd0} than conventional FETs [9]. For instance, at a GBW of 3 GHz, lower current consumption (>2 times) can be obtained by employing GNR TFETs in comparison to the other technologies. In addition, the GNR TFETs allow for the smallest device areas for a given design specification due to their superior current drives (J_d) for a given g_m/I_d.

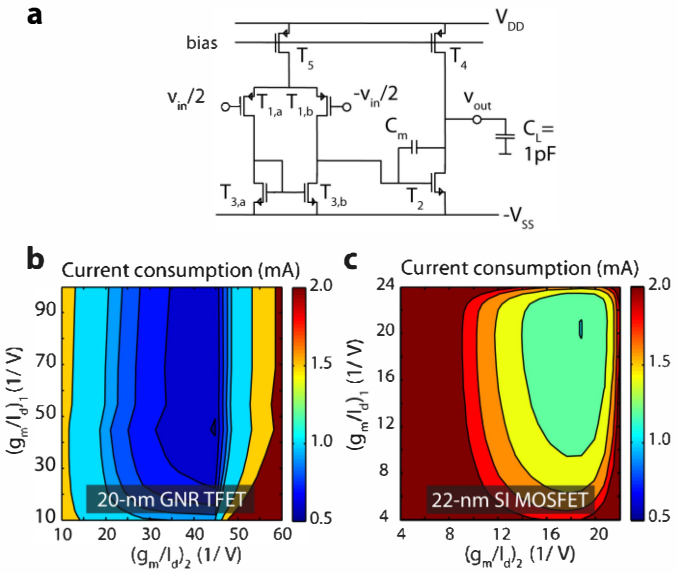

Fig. 3. Schematic circuit of a Miller OTA (a). And design space exploration for GBW = 1 GHz and PM = 60 ° employing: (b) 20-nm GNR TFETs, and (c) 22-nm Si MOSFETs. Current consumption for the optimal design employing GNR TFETs is about the minimum theoretically achievable in this circuit if employing ideal traditional FETs (C_s=C_g=C_d=0), which is >2X lower than the minimum achievable in the 22-nm Si MOSFET technology.

B. Miller OTA

A Miller OTA shown in Fig. 3a is analyzed employing n and p-type 20-nm GNR TFETs as well as 22-nm Si MOSFETs. GNR TFETs are chosen over other TFETs because of their large subthreshold current densities, but also because they provide similar characteristics for both n and p-type transistors resulting from the symmetric band structure of graphene [5, 10], which is desirable for circuit design.

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This amplifier topology has two poles and a right half plane zero; usual requirements for more than 60° phase margin (*PM*) in this circuit are: *NDP* = 2.2, *Z* = 10, where *NDP* = ω_{p2} / *GBW* (ω_{p2} is the frequency of the non dominant pole), and *Z* = ω_z / *GBW* (ω_z is the frequency of the zero). The current consumption in this amplifier can be expressed as:

$$I = 2I_{d1} + I_{d2} = 2\frac{GBW \times C_m}{(g_m / i_d)_1} + \frac{Z \times GBW \times C_m}{(g_m / i_d)_2}, \quad (2)$$

where I_{d1} is the DC current through the transistors at the input differential pair (T_{1a}, T_{1b}), I_{d2} is the current through the transistor at the output stage (T_2), and C_m is the Miller compensation capacitance, which is calculated as:

$$C_m = \frac{NDP}{2Z}\left(C_1 + C_2 + \sqrt{(C_1 + C_2)^2 + \frac{4Z \times C_1 \times C_2}{NDP}}\right), \quad (3)$$

where $C_2 = C_{out} + C_L$ is the total output capacitance of the amplifier (C_{out} is the capacitance seen looking from the node V_{out} to ground in the absence of load capacitance), and C_1 is the effective capacitance from the gate of T_2 to the AC ground.

From Eqn. (2) and (3), we find that the minimum achievable current consumption in ideal traditional FETs based Miller OTA, i.e. the current consumption considering the transistors with zero capacitances and maximum g_m/I_d, is thus given by:

$$I = \frac{(2+Z) \times GBW \times U_T \times C_L \times NDP}{Z}, \quad (4)$$

The synthesis mechanism described in Ref. [6] was employed to determine the amplifier design achieving the minimum current consumption. For a 500 MHz *GBW* and 60° *PM* design requirements, the optimal current consumption employing the 20-nm-gate GNR TFETs was found to be 35% smaller than the minimum theoretically achievable by ideal traditional FETs under the same design constraints, Eq. (4). When setting the GBW requirement to 1GHz, the current consumption employing GNR TFETs was found to be about the minimum theoretically achievable in this circuit if employing ideal traditional FETs (2% lower). Moreover, when comparing the current consumption with respect to that achievable employing a similar gate-length Si-FET technology (22-nm), we see that the current consumption of the Miller OTA with GNR TFETs can be > 2X smaller, i.e. the minimum achievable current consumption in the GNR/Si-MOSFET amplifiers is ~ 0.5/1.2 mA, respectively (Fig. 3b-c).

V. Conclusion

Since TFETs can operate in the sub-threshold region with larger g_m/I_d than traditional FETs, low power analog circuits with lower current consumption can be designed. In particular, GNR TFETs promise large bandwidth at low voltage drive due to their high current density in the subthreshold region. Based on this analysis, GNR TFETs seem to be very promising among all the field effect transistors proposed to date for ultra-low power analog applications.

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