Monolithically Integrated E/D-mode InAlN HEMTs with f_t/f_{max} > 200/220 GHz

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Although recent years have seen impressive progress on high speed GaN HEMTs [1-3], fabrication approaches allowing for monolithic integration of E and D-mode devices with simplicity and low-cost, such as gate recess and plasma treatment, remain challenging. Carrier mobility in channels subject to gate recess or plasma treatment generally degrades, which is difficult to fully recover even after post-processing annealing etc. In this work, we report high-performance monolithically integrated D-mode and gate-recessed E-mode InAlN/AlN/GaN HEMTs with a nominal gate length of 30 nm (Fig. 1) and 2-level metal interconnects. The D-mode HEMTs show an extrinsic g_m of 920 mS/mm and f_t/f_{max} of 194/220 GHz. The gate-recessed E-modes show an extrinsic g_m of 1306 mS/mm and f_t/f_{max} of 225/250 GHz. The higher speed of the E-modes stems from the higher intrinsic g_m, which is also found to be comparable to that reported in epitaxially defined E-modes with a 4.5 nm barrier and 20-nm gate length by Shinohara *et al.* [1], ~ 1700 mS/mm, suggesting that the carrier mobility likely suffers from negligible degradation in our monolithically integrated E-mode HEMTs.

Schematic cross sections of the monolithically integrated D and E-mode HEMTs are presented in Fig. 1, consisting of a 6.1-nm lattice-matched ternary $In_{0.17}Al_{0.83}N$ barrier, a 1-nm AlN spacer, a 200-nm unintentionally doped GaN channel and a 1.6-μm semi-insulating (SI) GaN buffer on SiC substrate. The devices do not include a back barrier. Graded n^+InGaN/GaN regrown ohmic contacts [4] were employed and a dielectric etch-back process was performed to remove part of the SiON dielectric around the gate after the T-gate fabrication. The gate recess process is the same as reported in [5], with the InAlN barrier selectively removed to achieve E-mode operation. The source-drain distance L_{sd} is 0.6 μm. TLM measurements yielded a contact resistance R_c of 0.13 Ω·mm and a sheet resistance R_{sh} of 310 Ω/sq .

The common-source family of I-Vs of the D and E-mode devices is shown in Fig. 2. The D(E)-mode HEMTs exhibit a high current density of 1.9(1.6) A/mm and a low on-resistance of 0.56(0.55) Ω·mm, owing to the low contact resistance and small L_{sd}. Also shown in Fig. 2 are the device transfer characteristics with V_{gs} swept from -2 to 2 V at V_{ds} = 2 V; the peak extrinsic transconductance $g_{m,ext}$ is 920(1306) mS/mm at I_d ~ 0.6(0.7) A/mm and the threshold voltage V_{th} is ~ -1.0 (+0.5) V for the D(E) mode devices, respectively. On-wafer RF measurements were taken from 250 MHz to 30 GHz at the peak f_T bias condition. RF gains and equivalent-circuit-parameters (ECP) for both devices are presented in Fig. 3 and Table 1, respectively. Also included in Table 1 for comparison are ECPs of the epitaxially defined 20-nm gate length E- and D-mode devices reported in [1]. The intrinsic transconductance ($g_{m,int}$) values from the ECPs are found to be similar for the devices in this work and those reported in [1]: 1040 vs. 1148 for the D-mode HEMTs and 1680 vs. 1725 mS/mm for the E-mode devices, respectively, which suggests similar device speed is attainable when driving comparable device capacitances. However, we note that the C_{gs} values are higher in these devices due to a longer gate foot print (30 nm vs. 20 nm in [1]) and partly due to the flared gate profile revealed in the TEM image (Fig. 1); in our E-mode devices, the top barrier is also thinner (though leading to a favorably smaller output conductance). The higher C_{gs} and R_s+R_d values (40 to 70% larger) can mostly explain the difference in the device speed. These results indicate that f_T > 350 GHz is achievable by further scaling down the gate length in InAlN HEMTs by gate recess.

[1] K. Shinohara *et al. IEEE IEDM,* (2011). [2] Y. Yue et al. *IEEE EDL,* on line (2012). [3] D. Denninghoff *et al.*, *IEEE EDL,* on line (2012). [4] J. Guo *et al. IEEE EDL,* 33,525 (2012). [5] R. Wang *et al. IEEE EDL*, 32, 309 (2011).

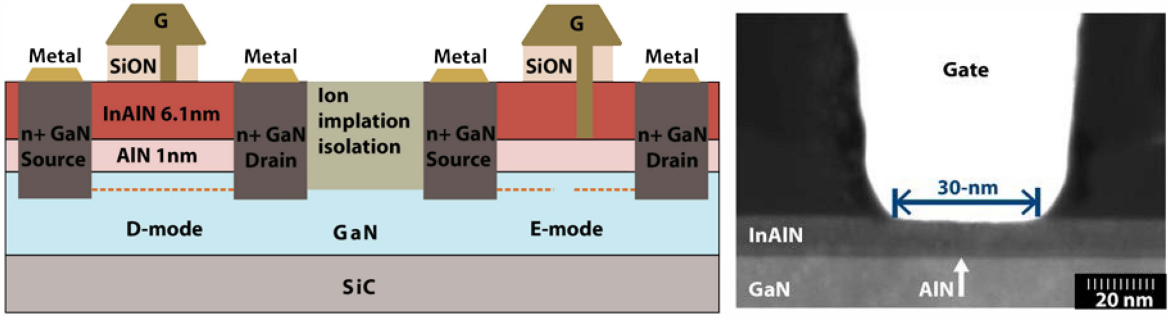

Fig. 1 (left) Schematic cross-section of monolithically integrated D/E mode InAlN/AlN/GaN HEMTs.
(right) Representative TEM image of the gate profile showing a bottom foot print of 30-nm in the HEMTs.

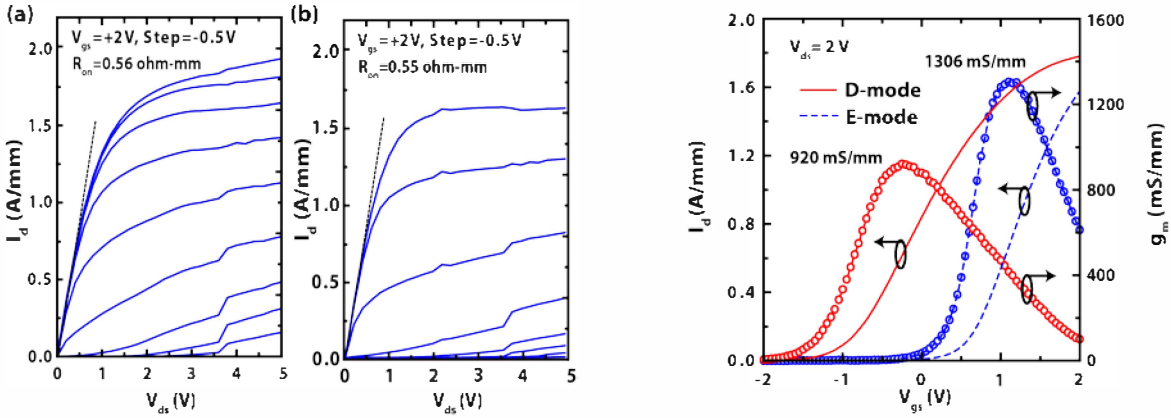

Fig. 2 (left) Common source family of I-Vs of 30-nm D-mode (a) and E-mode (b) HEMTs.
(right) Transfer characteristics of the 30-nm D- and E-mode HEMTs.

	30-nm		20-nm [1]	
	D-mode	E-mode	D-mode	E-mode
g_m (mS/mm)	1040	1680	1148	1725
g_{ds} (mS/mm)	202	169	173	258
C_{gs} (fF/mm)	520	811	408	513
C_{gd} (fF/mm)	176	178	116	145
R_s (Ω.mm)	0.25	0.23	0.15	0.15
R_d (Ω.mm)	0.27	0.26	0.16	0.20
Top barrier(nm)	7.1	2	6	4.5
f_T (GHz) ECP	192	220	311	345
f_{max} (GHz) ECP	221	245	362	240
f_T (GHz) meas.	194	225	310	343
f_{max} (GHz) meas.	225	250	364	236

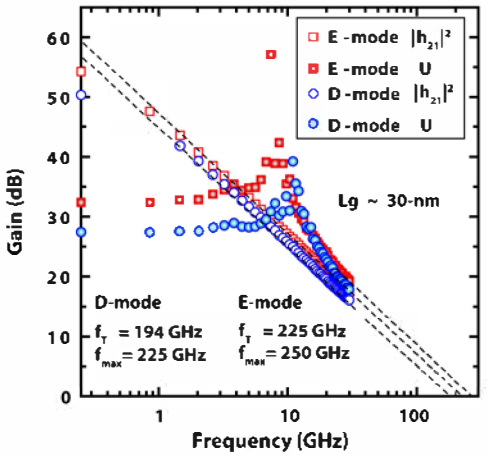

Fig. 3 Small signal RF characteristics of the 30-nm D/E- mode HEMTs.

Table.1 Extracted equivalent circuit parameters (ECP) for the monolithically integrated 30-nm D- and E-mode HEMTs along with the ECPs of the epitaxially defined 20-nm D- and E-mode HEMTs reported in [1] for comparison.