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Graphene nanoribbon FETs for digital electronics: experiment and modeling

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ABSTRACT

One-dimensional nanostructures of graphene such as graphene nanoribbons (GNRs) can prove attractive for digital electronics in the form of interband tunneling transistors, as they are capable of high drive currents. Here, we report on the transport properties of p-n junctions formed in GNR field effect transistors (FETs). It is found that the current density in the devices is indeed high; in the 1–1.5 A/mm range have been measured, comparable to Si-MOSFETs and III-V Nitride HEMTs. The observed unique current–voltage characteristics of the double-gated GNR FETs having a lateral p-n junction as their channel is explained by a field-effect model. Due to the lack of sufficiently large bandgap in the 30 nm wide GNR, the device still cannot be turned off completely, but rectification is achieved. The results suggest that the fabrication of tunneling FETs made out of graphene is possible and their characteristics may meet the expectations. Copyright © 2012 John Wiley & Sons, Ltd.

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KEY WORDS: graphene; nanoribbon; transistor; p-n junction; high-field transport

The recent discovery of graphene [1], a single atomic sheet of graphite, has ignited intense research activities to explore the electronic properties of this novel two-dimensional (2D) electronic system. Charge transport in graphene differs from that in conventional 2D electronic systems as a consequence of the linear energy dispersion relation near the charge neutrality (Dirac) point in the electronic band structure [2]. Though in theory, its electronic structure and transport properties are well known, the applicability as channel replacement material in conventional CMOS technology is still an open question. High mobility [3] and high current carrying capacity [4,5] make graphene very attractive, but on the other hand, low I_{ON}/I_{OFF} ratio and the lack of sufficient saturation in I_{ON} are yet unsolved drawbacks. In the past, we demonstrated these properties in double-gated graphene nanoribbon field effect transistors (GNR FETs). We successfully achieved I_{ON}/I_{OFF} ratios of 10^6 at cryogenic temperatures using either top or back gates, and sublinear output characteristic was observed [5]. Graphene has been studied mostly at low biases till date. For the application in practical devices, it is essential to investigate the high-field transport properties. In this letter, we present on the high field characteristics and the modeling of double-gated GNR devices biased partially n-type and partially p-type forming p-n junction such way.

Exfoliated graphene flakes on heavily n-type doped silicon wafers with $t_{ox} = 300$ nm thick thermal oxide from Graphene Industries were used for the experiments. The wafers were backside-metalized after oxide removal in buffered HF to form back gate contacts. The graphene flakes were patterned successfully by O_2 plasma reactive ion etch forming nanoribbons with widths down to 20 nm [6]. To achieve this, 20 nm thick Al as a mask was used patterned by e-beam lithography using PMMA and lift-off. Cr/Au source/drain contacts and Al_2O_3/Ti/Au as top gate ($t_{ox} = 30$ nm) have been

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deposited to form FETs. After the source/drain metal deposition and lift-off, the samples were annealed in forming gas at ~400 °C for ~2 h to remove the e-beam resist residue [7]. 1 nm e-beam deposited Al was used as seed layer for the ALD-deposited Al_2O_3. The channel length of the fabricated devices is 2 µm, and the length of the top gate electrode is about 1 µm, covering half of the channel.

The SEM image in Figure 1 (a) shows a typical GNR FET, and a schematic cross section can be seen on Figure 1 (b). High current annealing [8] was performed to drive off impurities for some FETs to recover their intrinsic performance. The devices were measured using a semiconductor parameter analyzer in ambient environment and in vacuum (5×10^{-5} Torr), at room temperature at 77 K and at 4 K.

In this paper, we present the measurements of a single device with 30 nm GNR width at room temperature and on 4 K. It is found that at high applied source-drain current, the temperature has very little effect on the device performance, namely at cryogenic temperatures, the high-field modulation is only ~10% more. We fabricated many similar devices, and we observed similar characteristics in all cases. Figure 2 (a) and (b) shows the source-drain conductance at $V_{DS} = 20$ mV and at $V_{DS} = 1$ V, respectively, as a function of the top gate and the back gate. The back gate capacitance is ~11 nF/cm^2 assuming $\kappa = 3.9$, and the top gate capacitance is 209 nF/cm^2 calculated based on the measurement of the minimum conductance (Dirac) point as shown in Figure 2 (b). The Dirac point is defined by the ratio of the applied voltages on both gate, the slope defining the value of C_{top}/C_{back} ~19. From both a constant back gate or constant top gate slice, we can determine $V^0_{TG} = -5$ V and $V^0_{BG} = -45$ V,

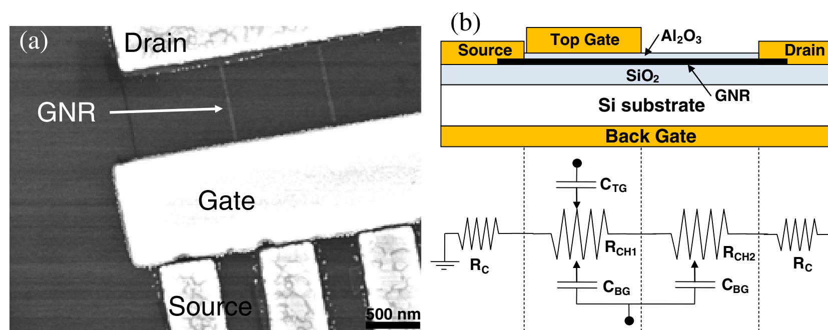

Figure 1. (a) SEM micrograph of GNR FETs. Half of the channels are top gated, while the whole device is back gated. The channel length is 2 µm, the gate width is 1 µm. The width of the GNR is 30 nm. (b) Device schematics and wiring diagram of the device model showing the critical resistances and the influence of the gates on the two parts of the channel.

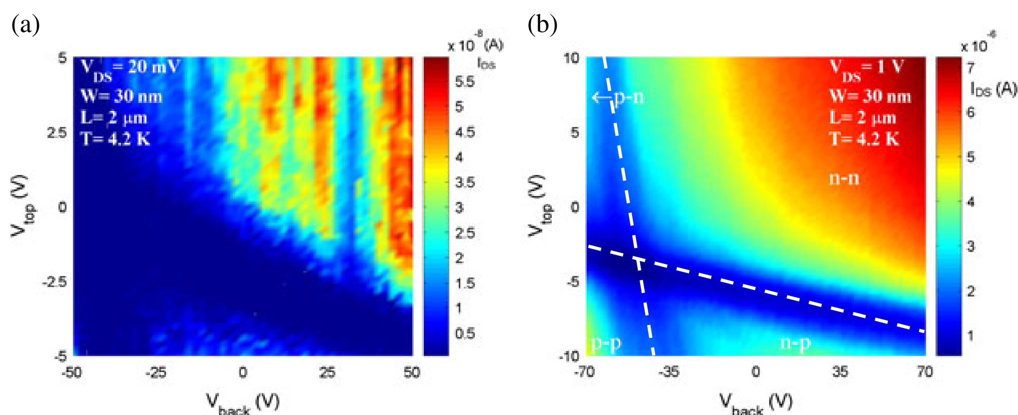

Figure 2. (a) Conductance steps at 4.2 K at low source-drain voltage (linear scale); (b) At higher bias ($V_{DS} = 1$ V), the modulation is smaller. This high bias conductance is not influenced by the temperature; room temperature measurement yields the same result.

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indicating strong n-type doping. While the devices before the top gate deposition were slightly p-type doped, we can conclude that the strong n-doping is due to trapped charges in the top gate oxide and other impurities on the graphene oxide interface. A comparison of the transfer characteristics before and after the top gate oxide deposition can be seen on Figure 3 (a) and (b).

Temperature-dependent measurements of the off-state conductance have confirmed bandgap opening of >26 meV depending on GNR widths and result in 20x and 10^3x modulation at room temperature and 4 K, respectively, by varying the top gate potential between +/− 5 V (Figure 3). Quantized conductance was observed at low temperature, which is clearly indicates that the carriers in the GNR channel are one dimensionally confined as observed before [9]. This phenomenon also gives us a tool to extract the value of the GNR bandgap; details of these measurements and modeling are detailed in an earlier report [6].

The source and drain contacts are in touch with a large 2D graphene region to ensure low contact resistance. The 2D graphene has no bandgap so the Cr/Au metal can form good ohmic contacts easily. The back gate may vary the carrier concentration of the graphene at the contacts, but due to its large size, it will have always much lower resistance than the GNR channel, always supplying the channel with high enough number of carriers.

Figure 4 (a), (b), and (c) shows the measured I_{DS} for different top gate voltages at V_{back} = -70 V, 0 V, and +70 V, respectively. To understand the device operation, we have to examine the device structure in detail. The channel of the devices can be separated into two distinct regions: one having back gate only and the other having both top and back gates. A model has been developed to explain the transistor characteristics of the p-n channel GNR FET by extending the work of Meric *et al*. [4].

We applied a field effect model to both sides of the junction separately. The applied gate and source-drain voltages determine the carrier concentration on both parts of the channel according

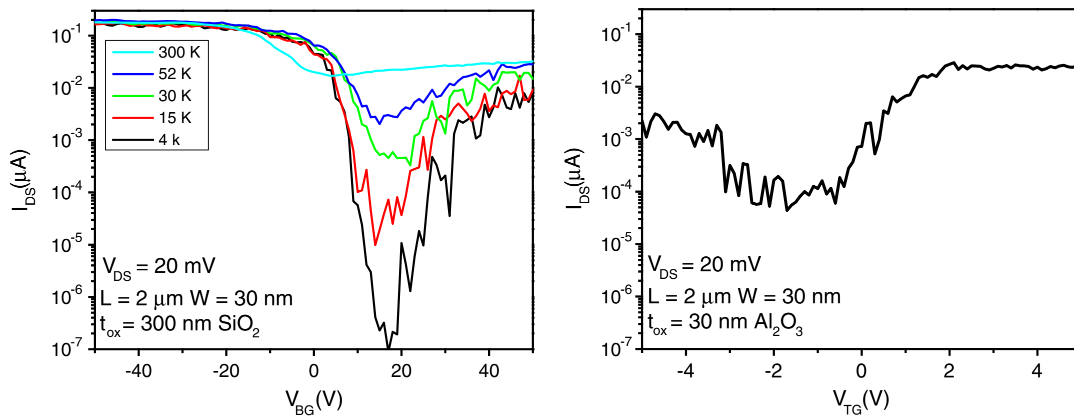

Figure 3. Comparison of the transfer characteristics (a) before and (b) after the top gate oxide deposition. The initially p-doped device shifted to n-doped. The I_{ON}/I_{OFF} ratio decreased by several orders of magnitude. (a) shows the temperature dependence of I_{DS}, which is used as the base of the bandgap extraction.

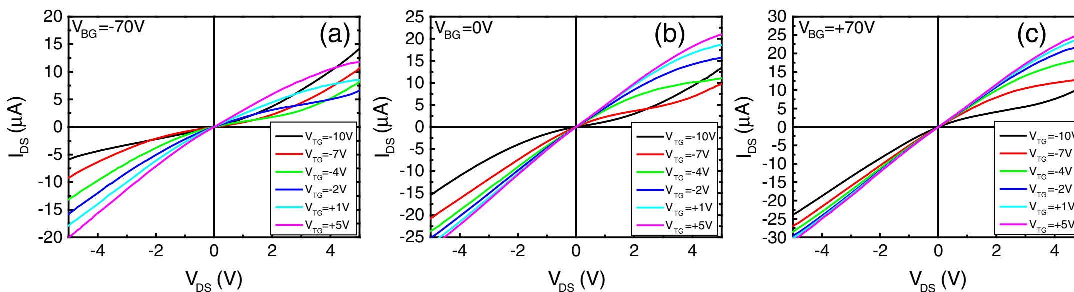

Figure 4. Measured room temperature I_{DS} versus V_{DS} at −70 V (a), 0 V (b), and +70 V (c) back gate bias.

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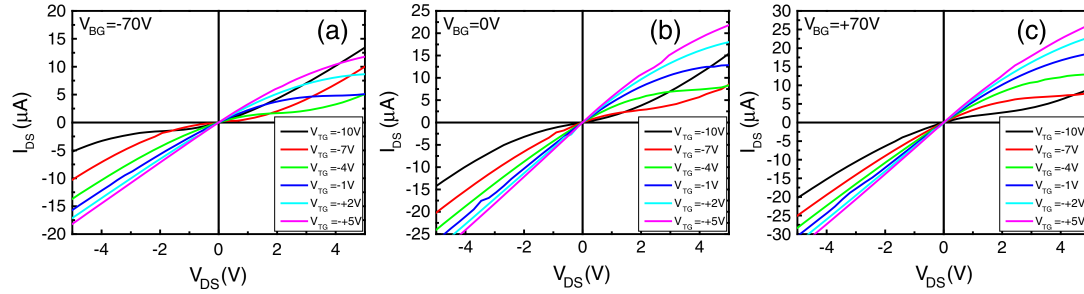

Figure 5. Simulated device characteristic at the same bias conditions as the device shown in Figures 3 and 4. I_{DS} versus V_{DS} at −70 V (a), 0 V (b), and +70 V (c) back gate bias.

$$n(x) = \sqrt{n_0^2 + \left(\frac{C_{tg}}{q}\left(V_{tg} - V_{tg0} - V(x)\right) + \frac{C_{bg}}{q}\left(V_{bg} - V_{bg0} - V(x)\right)\right)^2}$$

where x is the distance along the channel and $V(x)$ is the potential in the channel due to the applied source-drain voltage. A schematic of the model is shown on Figure 1 (b). The current in the channel is expressed by

$$J(x) = qn(x)\mu F(x)$$

where μ is the mobility and $F(x)$ is the electric field along the channel. The I-V characteristics are obtained by forcing current continuity in a self-consistent electrostatic and transport model

$$I(V_{DS}) = q\frac{W}{L}\mu\int_0^{V_{DS}} n(x)dV(x)$$

where L is the channel length, and W is the GNR width. Carrier drift velocity and mobility saturation are considered depending on the carrier concentration based on the work of Dorgan *et al*. [10].

$$v_{sat} = \frac{\omega_{op}}{\sqrt{\pi n(x)}}$$

where ω_{op} is the optical phonon wavelength of the dominant scattering phonons, which are surface optical phonons of the high-κ oxide. And

$$\mu = \frac{\mu_0}{\sqrt{1 + \left(\frac{\mu_0 V_{DS}}{L v_{sat}}\right)^2}}.$$

For simplicity, we assumed equal mobility and saturation velocity to describe both the electrons and holes. The solution not only provides the I-V characteristics of the device but detailed information about the carrier concentration under various bias conditions. Figures 4 and 5 demonstrate the experimental and modeling data, showing close agreement. As input parameters in the model, we used mobility of 300 cm^2/Vs, a minimum carrier density of $5 \cdot 10^{11}$ cm^{-2}, and source-drain series resistance of 0.5 Ω.mm. The saturation of current at high positive bias is caused by depletion of the carriers even in those cases when the gate biases set a high initial carrier concentration. At high negative drain bias, on the other hand, lack of saturation is observed. This is because the drain bias in this case further increases the carrier concentration instead of depleting. Depending on the gate bias conditions, the flattening of the current occurs at different applied source-drain bias. If

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$V_{BG} = -70$ V ((a) on Figures 3 and 4) as V_{TG} increases, one can see that plateau of the I_{DS} occurs at higher and higher positive bias. At positive V_{TG} pinch-off occurs at V_{DS} =5 V only. At more positive back gate biases ((b) and (c) on Figures 3 and 4), the plateauing of the current occurs at highly negative top gate biases only. Superlinear current increase is caused together by the sharp increase of carrier concentration close to the Dirac point and the increase of the accelerating field.

In conclusion, p-n junction in GNR FETs has been experimentally demonstrated. The analysis of the device operation shows that sublinear and superlinear features observed in the I-V characteristics are due to the device electrostatics. The p-n junction channels are practically transparent to interband tunneling of carriers due to the small bandgap and high applied bias but offer an exciting novel structure for configuring and designing device characteristics with various functionalities.

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