Exfoliated $MoTe_2$ Field-Effect Transistor

Sara Fathipour[1], Wan Sik Hwang[1,2], Thomas Kosel[1], Huili (Grace) Xing[1], Wilfried Haensch[2],
Debdeep Jena[1], and Alan Seabaugh[1]

[1]Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556, USA
[2]IBM T. J. Watson Research Center, Yorktown Heights, New York 10598, USA

Transition metal dichalcogenides (TMD) are materials with the form MX_2 where M is a metal and X can be Se, S, or Te. These materials have covalent bonding within the layers and Van der Waals bonding between the layers [1]. Unlike graphene, the existence of a band gap eliminates the need to form nanoribbons for two-dimensional crystal tunnel field-effect transistors (TFETs). Among TMDs, molybdenum ditelluride $MoTe_2$ has the lowest band gap (1 eV) which makes it highly suitable for TFET application. In this paper, we report the first fabrication and electrical characteristics of a $MoTe_2$ FET, made on exfoliated multilayer crystals.

The $MoTe_2$ process flow for forming back-gated FETs begins with the formation of a 30 nm atomic-layer-deposited Al_2O_3 back-gate dielectric on a *p*+ Si substrate. The multilayer $MoTe_2$ crystals were mechanically exfoliated from bulk $MoTe_2$ (from American Elements Company with 99.9% purity) and transferred onto the Al_2O_3 using scotch tape. Electron beam deposited Ti followed by Au was used to form source, drain and back gate metallization.

Energy dispersive X-ray analysis (EDX) shows that the exfoliated $MoTe_X$ (x=1.88) flakes mainly consist of Mo and Te (C, O, and Cu are observed, but they are from the mounting grid). Transmission electron micrographs of the $MoTe_2$ flakes have been examined. Both high-resolution images and electron diffraction patterns confirm the crystal structure with a lattice parameter of 0.35 nm, the same as the bulk lattice parameter. Other lattice parameters are as follows: b=3.53Å, c=13.88Å, α=β=90˚, γ= 120˚ and space group P63/mmc (#194).

The transfer characteristic, i.e. drain current vs. back gate voltage, I_D-V_{BG} shows that conductance is achieved at positive gate voltages consistent with *n*-type channel conduction. Although at different back gate voltages both on and off currents are different, here, we define the on/off current ratio to be the maximum achievable on to off current ratio. The on/off current ratio increases as temperature decreases from 1.98 at room temperature to 320.95 at 4K. At room temperature the off current is high, 4.75 µA, presumably due to residual positive charge at the $Al_2O_3/MoTe_2$ interface. At 300K the current is not saturated and the delayed turn-on shows evidence of a Schottky contact behavior.

This work was supported by the Semiconductor Research Corporation (SRC), Nanoelectronics Research Initiative (NRI) and the National Institute of Standards and Technology (NIST) through the Midwest Institute for Nanoelectronics Discovery (MIND), STARnet, an SRC program sponsored by MARCO and DARPA, and by the Office of Naval Research (ONR) and the National Science Foundation (NSF).

[1] S. Kim, A. Konar, W. S. Hwang, J. Hak Lee, J. Lee, J. Yang, C. Jung, H. Kim, J. B. Yoo, J.Y. Choi, Y. W. Jin, S. Y. Lee, D. Jena,W. Choi, K. Kim, "High-mobility and low-power thin-film transistors based on multilayer MoS_2 crystals," *Nature Communications 3*, 1011, (Aug 2012).

978-1-4799-0814-1/13/$31.00 ©2013 IEEE

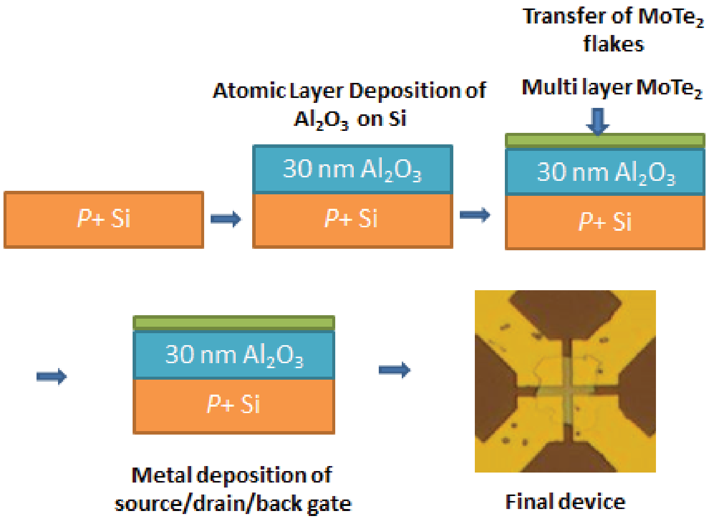

Figure 1: Fabrication process of $MoTe_2$ transistor

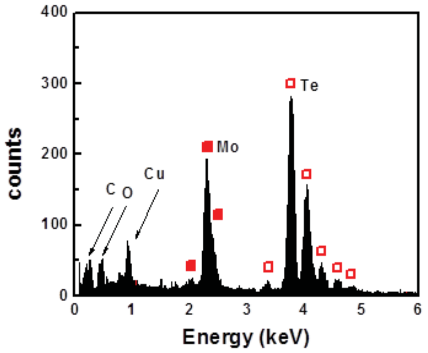

Figure 2: Energy dispersive X-ray analysis (EDX)

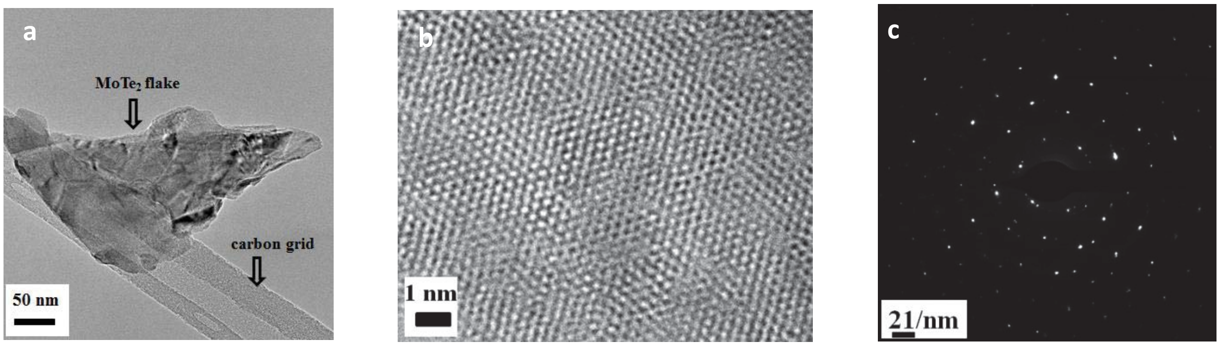

Figure 3: (a) Transmission electron micrograph (TEM) of a $MoTe_2$ flake, (b) high-resolution TEM, and (c) electron diffraction pattern

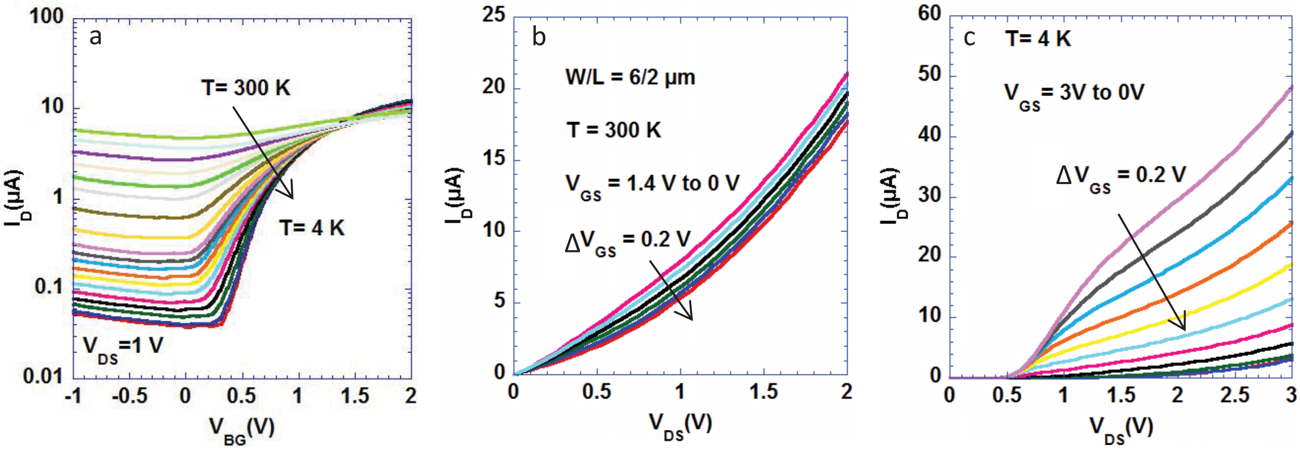

Figure 4: $MoTe_2$ transistor characteristics for W/L=6/2 μm. (a) Temperature dependence of the transfer characteristic, I_D-V_{BG} characteristics, and the common-source transistor characteristics at (b) 300 K, and at (c) 4 K.