## Nanomembrane β-Ga<sub>2</sub>O<sub>3</sub> High-Voltage Field Effect Transistors

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There is considerable excitement recently in the field of transparent conducting-oxide-semiconductors due to the successful realization of large-area single crystals of the wide-bandgap semiconductor  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> by bulk growth methods [1]. The availability of bulk  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> crystals led to the rapid demonstration of high-voltage metalsemiconductor field-effect transistors (MESFETs) by controlled Sn-doped epilayers grown by molecular beam epitaxy (MBE) [2].  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has an energy bandgap of ~4.9 eV, significantly larger than both GaN and SiC. Coupled with the availability of low-cost bulk crystals, this material is highly attractive for high-voltage switching applications. Here we show preliminary results that show that similar to layered crystals [3] and rather surprisingly, one can peel-off nanoscale layers of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> from a nominally undoped bulk single-crystal. Conducting channels can then be created electrostatically in these nanomembranes with a back-gate, and the resulting transistors are able to sustain very high voltages and still switch by several orders of magnitude.

The process-flow for the fabrication of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanomembrane field-effect transistors is shown in Fig. 1. The crystal  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> was grown by Czochralski method at IKZ Berlin [1]. Nanomembranes ~50 to 100 nm thick were mechanically exfoliated and transferred to a back-gated substrate. The source and drain contacts were defined by electron beam lithography (EBL) using Ti/Au (5/150 nm) contacts. The final device went through an annealing process in Ar/H<sub>2</sub> at 300 °C for 3 hours to reduce the contact resistance. Optical transmission spectra of the flake are shown in Fig. 2 and it clearly shows an optical bandgap of 4.8 eV. Figure 3(a) shows the drain current versus gatesource bias,  $I_D vs. V_{GS}$ , at room temperature at three drain biases. The gate modulation is ~10<sup>7</sup>x and the device shows n-type semiconducting behavior. Electron-beam evaporated Ti/Au contacts do not result in ohmic contacts, but rather show leaky Schottky barrier characteristics. Nevertheless, from the transfer characteristics, we extract an "extrinsic" field-effect mobility of ~  $10 \text{ cm}^2/\text{Vs}$  as shown in Fig. 3(b). This value represents a lower limit; it should be possible to obtain  $\sim 300 \text{ cm}^2/\text{V}$ s with de-embedding for this device or better still by lowering the contact resistance [2]. The subthreshold swing (SS) of the device in Fig. 3(c) can approach ~150 mV/dec, not significantly different from two-dimensional transition-metal dichalcogenide semiconductor FETs. The family of  $I_D$ - $V_{DS}$  curves at various  $V_{BG}$  in Fig. 3(d) shows a typical transistor performance including resistive behavior at low  $V_{DS}$  and current saturation at high  $V_{DS}$ . Figure 4(a) shows a comparison of electrical breakdown voltage of various thin-film channel materials (β-Ga<sub>2</sub>O<sub>3</sub>, MoS<sub>2</sub>, and MoTe<sub>2</sub>) of similar geometries and back-gates. A MoTe<sub>2</sub> FET shows the lowest breakdown voltage around 0.05 MV/cm due to the lowest bandgap (~0.6 eV). For the MoS<sub>2</sub> FET, avalanche breakdown field occurs around 0.1 MV/cm.  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FETs shows a decent gate modulation even under a high drain voltage of 40 V. These properties of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FET are attractive for high-power and high-voltage device applications. The cross-section TEM image in Fig. 5 shows the crystalline nature of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> and the contact metals and the back gate SiO<sub>2</sub> dielectric. The low subthreshold value observed may be related to the qualitatively sharp interface observed between  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> and SiO<sub>2</sub> but more studies are needed to quantify this observation.

In summary, nanomembrane high-voltage FETs with  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> channels were fabricated and characterized for the first time. The large bandgap leads to a high on/off ratio. A flat interface between  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> and SiO<sub>2</sub> leads to a steep slope of ~ 150 mV/dec. The high breakdown field of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> allow significantly higher voltages to be applied to the drain, while still switching by orders of magnitude. Since  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has been found to have a rather poor thermal conductivity, nanoscale membranes might offer opportunities for efficient heat removal. Nanoscale membranes can also be self-depleted even when doped lightly, and thus form semi-insulating layers, which may make it possible to make FETs without controlled epitaxy. A primary challenge is the formation of ohmic contacts.

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FIG. 1. Schematic process flow for nanomembrane  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> field-effect transistors. The nanomembrane thicknesses are in the range of 50 to 100 nm.

FIG. 2. Optical transmission spectra of  $Ga_2O_3$  flake indicating bandgap of 4.8 eV.



FIG. 3. Transport properties of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> field-effect transistor with  $W/L = 2/2 \mu m$ . (a) Drain current,  $I_D vs$ . back gate-tosource voltage,  $V_{BG}$ , showing ~10<sup>7</sup> on/off current ratio and *n*-type semiconductor behavior. (b) Field-effect mobility and (c) subthreshold swing *vs*.  $V_{BG}$ . (d) Common-source transistor characteristics,  $I_D vs$ .  $V_{DS}$ , showing current saturation.



FIG. 4. (a) Comparison of breakdown voltage of various multilayered channel materials (Ga<sub>2</sub>O<sub>3</sub>, MoS<sub>2</sub>, and MoTe<sub>2</sub>). (b) Transfer characteristic of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FET at high drain voltage. Insert show a family of  $I_D$  vs.  $V_{DS}$  showing robust device characteristic even at high  $V_{DS}$ .

FIG. 5. Cross-sectional TEM image of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FET, showing a flat interface between Ga<sub>2</sub>O<sub>3</sub> and the SiO<sub>2</sub> dielectric, as well as between the Ga<sub>2</sub>O<sub>3</sub> and the Ti/Au electrode.