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Time delay analysis in high speed gate-recessed E-mode InAlN HEMTs

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ABSTRACT

Delay analysis providing an alternative physical explanation on carrier transport, which may be more applicable to high electron mobility transistor (HEMT) channels with moderate carrier mobilities, has been applied to enhancement-mode (E-mode) and depletion-mode (D-mode) InAlN/AlN/GaN HEMTs with comparable f_T at room and cryogenic temperatures. It was found that the speed of the E-mode HEMTs with 33-nm long T-gate is dominated by parasitic delays, >40% of the total delay; channel mobility might have degraded due to gate recess.

1. Introduction

GaN based enhancement-mode (E-mode) transistors have attracted great interest due to their advantages in high power high frequency applications, including single polarity voltage supply, normally off operation, and direct coupled logic based on E-mode and depletion (D)-mode devices [1–4]; however, high-speed E-mode HEMTs monolithically integrated with D-mode devices remains challenging [4–6]. Though high quality monolithically integrated E-mode devices can be fabricated employing selective molecular beam epitaxy (MBE) regrowth, its fabrication and regrowth processes are complex [7]. On the other hand, approaches such as gate-recess [8] and plasma treatments are more amenable to low-cost fabrication, while possible carrier transport property degradation is always a key concern employing these treatments. To extract carrier transport properties in E-mode HEMTs, gated Hall effect measurements can be utilized. However, due to loading effects during the gate recess etch, the gate region of a submicron HEMT may experience different degree of damage from the large area gated Hall effect test structures. As a result, there is a need to understand carrier transport from the HEMT characteristics directly for assessing the possible gate damage.

In this letter, we present a modified time delay analysis method that provides an evaluation of possible gate damage in addition to insight on the RF performance and speed limits of highly scaled E-mode InAlN HEMTs based on a 33-nm-long recessed gate device with a T-gate.

2. Experimental

Comparative analysis of time delays was carried out at 77 K and RT on E-mode and D-mode InAlN HEMTs that exhibit similar f_T. Shown in Fig. 1 are schematic and transmission electron microscopy (TEM) cross sections of the E-mode InAlN/AlN/GaN HEMT. It consists of a 4.9-nm lattice-matched InAlN barrier, 1.0-nm AlN spacer, 200-nm undoped GaN channel and a 1.6-µm semi-insulating (SI) GaN buffer on SiC substrate. The E-mode HEMTs were processed at TriQuint Semiconductor, using a process similar to that reported in Ref. [2]. This process includes a recess-etched T-gate with a foot length of 33-nm, a source-drain distance L_{sd} of 1.2 µm, and SiO_2 passivation. The D-mode InAlN barrier HEMTs were processed at the University of Notre Dame, using a similar process reported in Ref. [6], featuring a rectangular gate with foot lengths of 80 nm, L_{sd} of 1.7 um and 5-nm Al_2O_3 passivation

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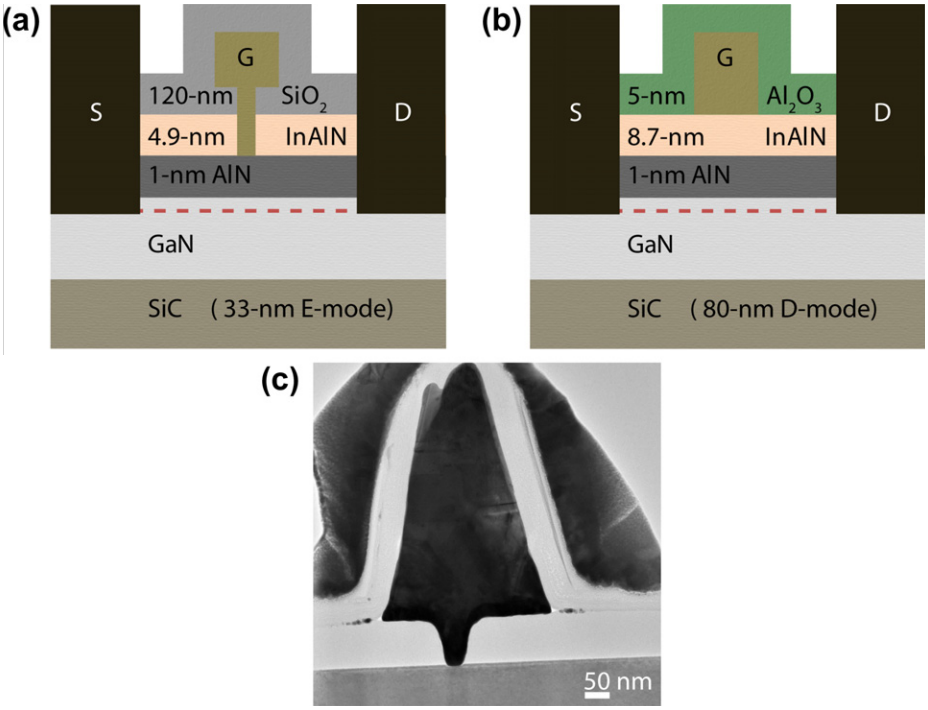

Fig. 1. Schematic of (a) E-mode and (b) D-mode InAlN/AlN/GaN HEMT cross section, and (b) transmission electron microscope (TEM) image of the E-mode device showing the T-gate and 33-nm gate length.

(Fig. 1b). The D-mode HEMT structure consists of an 8.7-nm lattice-matched InAlN barrier and 1.0-nm AlN spacer on GaN//SiC. Both the E-mode and D-mode HEMT structures were grown by IQE RF LLC, and the gate lengths confirmed by TEM. Although the structures of the E- and D-mode devices are different, analyzing the difference in the delay distribution allows us to clarify the effects of parasitic components and possibly damage from the gate-recess process in the E-mode device, since both exhibit similar total delay ($1/2\pi f_T$).

Transmission line method (TLM) measurements taken after processing yielded similar RT contact resistances R_c of 0.36(0.35) Ω mm and sheet resistances R_{sh} of 271(292) Ω/sq for both the E-mode (D-mode) devices. Typical 3-terminal breakdown voltage at a drain current I_d of 1 mA/mm is 15 V and 25 V for E-mode and D-mode devices when biased at $V_{gs} \ll V_{pinchoff}$, respectively. RT Hall effect measurements on a Van der Pauw test structure on the D-mode sample reveal a 2D electron gas (2DEG) mobility μ of 983 cm^2/V s and a concentration n_s of 2.23×10^{13} cm^{-2}. Representative RT Hall values of the HEMT epitaxial structure that the E-mode devices were fabricated on, are μ of ~1200 cm^2/V s and a concentration n_s of 2×10^{13} cm^{-2}. HEMT DC and RF measurements were also taken at 4 K, and no appreciable differences in device behavior were observed between 4 K and 77 K since the carrier mobility and device contact resistances were found to be constant over this temperature range [9]. On-wafer device RF measurements were taken with an HP 8510C vector network analyzer (VNA) in the frequency range from 250 MHz to 30 GHz. Calibration of the VNA was performed using LRM off-wafer impedance standards at corresponding temperatures. The device S-parameter measurements were de-embedded employing on-wafer open and short test structures.

3. Results and discussion

DC common-source and transfer characteristics of the HEMTs at RT and 77 K are shown in Fig. 2. It is observed that, at 77 K for all the devices, the on resistance R_{on} decreases ~10–15% and the peak extrinsic transconductance g_m increases ~15–20% from their RT values. These changes are consistent with the TLM and ColdFET measurement results showing a decrease of the total access resistance $R_s + R_d$:0.8/0.6 and 1.1/0.7 Ω mm at RT/77 K in the E-mode and D-mode HEMTs, respectively. The origin of the kink in the I_d–V_{ds} curves is not fully understood. However, its impact on the delay analysis reported here is negligible since these measurements were taken at bias conditions well away from this feature.

For the E-mode HEMT, extrapolation of both $|h_{21}|^2$ (current gain) and U (unilateral gain) at the corresponding peak f_T bias conditions with a −20 dB/dec slope gives f_T/f_{max} of 191/240 GHz at 77 K and 172/180 GHz at RT (Fig. 2d). The equivalent circuit parameters (ECPs) extracted from the measured S-parameters at 77 K/RT are tabulated in Table 1 for both devices along with the measured and simulated f_T/f_{max} values. These ECPs were extracted via fitting and numerical optimization employing Agilent ADS software. As shown in this table, at 77 K f_T increased by 20% for the 80-nm D-mode HEMT but only 10% for the 33-nm E-mode devices, relative to the RT values.

Time delay analysis was performed using the method described by Suemitsu (Fig. 3), where two de-embedding steps were used to remove the reactive effects of the probe pads and the effects of the device access parasitics ($R_s + R_d$) and extrinsic gate-source and gate-drain capacitances ($C_{gs,ext}$ and $C_{gd,ext}$) prior to computing the delay components [10,11]. Hence, the resultant delay ($\tau_{T,int}$) describes the intrinsic device, which is composed of an intrinsic gate delay component (τ_{int}, related to the transit time through the gate region), and a drain delay component (τ_d, related to the transit time through the extension of the depletion region towards drain). By plotting $\tau_{T,int}$ as a function of $V_{ds,int} = V_{ds} - I_d(R_s + R_d)$, the drain delay can be extracted, as shown in Fig. 4. The parasitic delay (τ_{par}) is computed by subtracting $\tau_{T,int}$ from the total delay calculated from f_t. In Refs. [10,11], the gate transit time (τ_g in Fig. 4) was calculated after subtracting a “channel charging time” (τ_{cc} in Fig. 4) and the drain delay from $\tau_{T,int}$, and subsequently used to extract

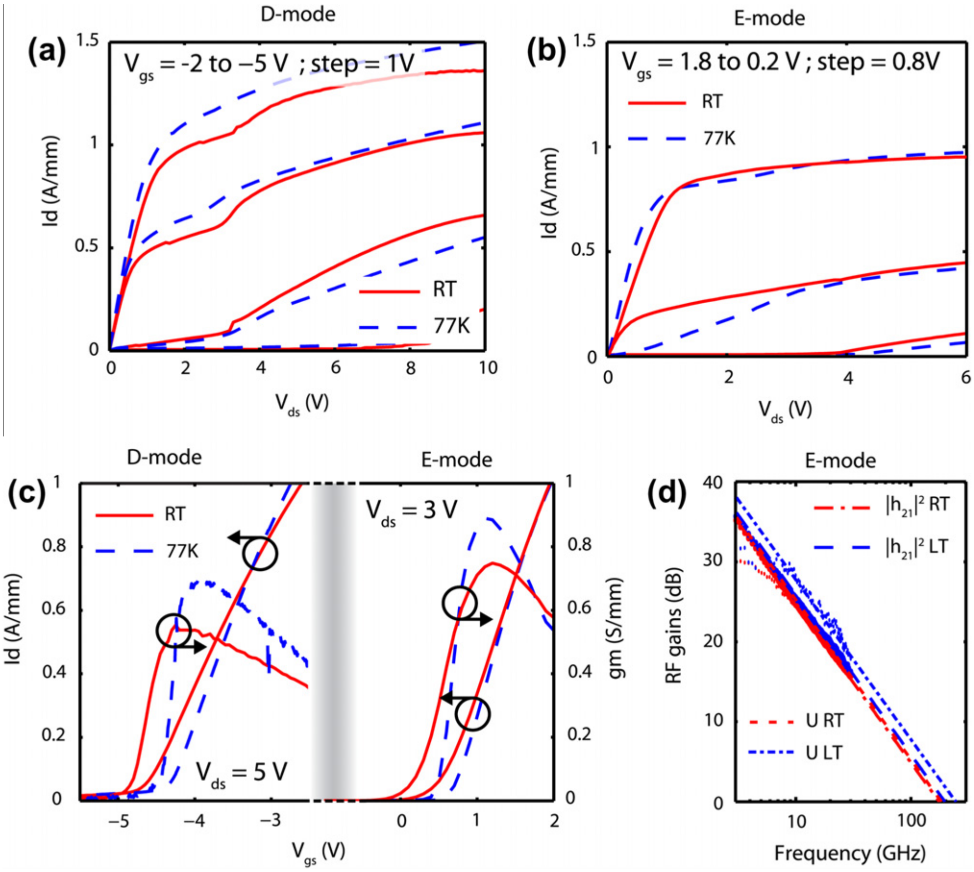

Fig. 2. (a and b) Representative common-source family of *I–Vs*, and (c) transfer characteristics for the 33-nm 2 × 25 μm E-mode (left) and 80-nm 2 × 50 μm D-mode (right) InAlN HEMTs at RT and 77 K. (d) RF-gains for the E-mode device (after deembeding).

Table 1
ECPs, f_t, and f_{max} for the analyzed devices.

	33-nm E-mode RT	33-nm E-mode 77 K	80-nm D-mode RT	80-nm D-mode 77 K	15-nm E-mode (projected RT)
V_{gs}/V_{ds} (V)	1.2/3	1.1/3	−3.9/6	−3.7/4	–
R_s (Ω mm)	0.40	0.31	0.63	0.37	0.15
R_d (Ω mm)	0.46	0.36	0.38	0.36	0.15
C_{gs} (fF/mm)	669	658	508	501	300
C_{gd} (fF/mm)	164	146	67	59	60
g_m (mS/mm)	1086	1142	750	822	1086
g_{ds} (mS/mm)	46	69	96	71	76
f_t/f_{max} (GHz) ECP	171/181	191/239	175/58	210/73	400/430
f_t/f_{max} A.D.[a] (GHz) meas.	172/180	191/240	176/59	214/74	–
f_t/f_{max} B.D.00000[a] (GHz) meas.	128/144	152/220	126/55	152/63	–

[a] A.D. for after deembedding and B.D. for before deembedding.

the electron velocity. In this work, we chose not to separate the "channel charging time" from the intrinsic gate delay since the 2nd de-embedding step accounts for the extrinsic *RC* charging time (τ_{par}). We note, however, that it is typical to observe an "intrinsic channel charging time" in HEMTs with low electron mobility, with a signature linear dependence of $\tau_{T,int}$ on the reciprocal of drain current ($1/I_{ds}$). As shown by Monte Carlo simulations in Ref. [12], this linear dependence is a result of carriers not being injected from the source at the saturation velocity when I_{ds} (i.e. V_{gs}) is varied, which is also consistent with a 2DEG n_s-dependent source injection velocity in GaN [13]. This injection velocity was introduced in Ref. [14], and is defined at the virtual source edge therefore dependent on n_s and mobility in the channel. In InGaAs based HEMTs, a constant $\tau_{T,int}$ versus $1/I_{ds}$ characteristic was observed by Suemitsu et al., indicating electrons were injected into the gate region at the saturation velocity [11]. For low-mobility channels, since electrons more gradually accelerate to the saturation velocity in the region under the gate near the source, the corresponding intrinsic channel charging delay time can be significant in the total delay.

Fig. 4 shows representative plots for the delay analysis when applying the aforementioned two-step deembedding method. The U-shaped curves shown in Fig. 4a are $\tau_{T,int}$ as a function of $V_{ds,int} = V_{ds} - I_d(R_s + R_d)$ for a series of $V_{gs,ext}$ values. Sometimes in the literature, $\tau_{T,int}$ versus $V_{ds,int}$ is plotted using f_T measured at a fixed $V_{gs,ext}$. Here we chose to adjust $V_{gs,ext}$ for each $V_{ds,int}$ for the highest f_T or minimum delay according to the original method described by Moll et al. [15]. The linear extrapolation of the minimum $\tau_{T,int}$ in each U-shaped curve to zero bias is τ_{int}, and τ_d is calculated from the difference between the absolute minimum of $\tau_{T,int}$ (at peak f_T) and τ_{int}. The inset of Fig. 4a shows $\tau_{T,int}$ as a function of $1/I_{ds}$ at V_{ds}, where the absolute minimum of $\tau_{T,int}$ is observed

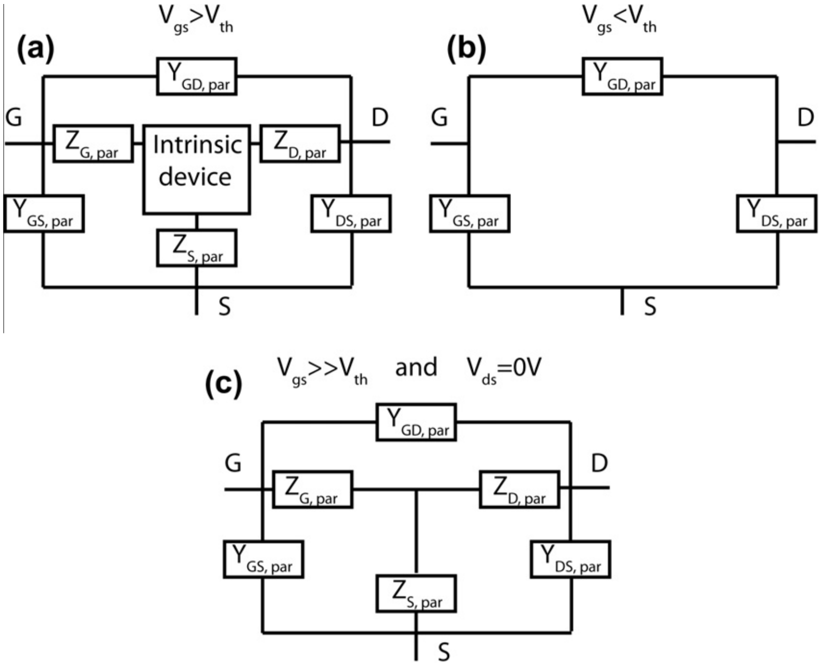

Fig. 3. (a) Parasitic elements in the device after deembeding the effect of the probe pads, the impedances (*Z*'s) represent the devices access parasitic resistances (mainly R_s and R_d) while the admittances (*Y*'s) represent the extrinsic parasitic capacitances (mainly $C_{gs,ext}$ and $C_{gd,ext}$). (b) Equivalent circuit model when $V_{gs} < V_{th}$, channel is depleted below the gate region thus only the extrinsic parasitic capacitances are present. (c) Equivalent circuit model when $V_{gs} \gg V_{th}$ and $V_{ds} = 0$ V; the intrinsic device behaves as short. From the S parameters under the bias conditions depicted in (a–c), we can deembed the effects of these extrinsic parasitic resistances and capacitances thus obtaining the intrinsic device delay.

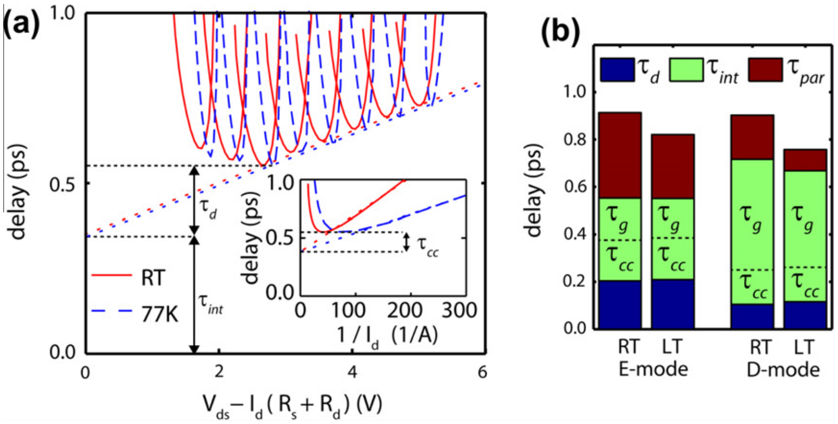

Fig. 4. (a) Delay analysis of the 33-nm E-mode for extraction of the intrinsic delay and drain delay using the two-step deembedding method (Suemitsu method). The inset shows extraction of the "intrinsic channel charging delay". (b) Comparison of delay components of the 33-nm E-mode HEMT with T-gate (left), 80-nm D-mode HEMT with rectangular-gate (right) at RT and 77 K.

[10,15], for extracting the "intrinsic channel charging delay". Shown in Fig. 4b is the comparison between 77 K and RT delay components for both the E- and D-mode HEMTs. It is interesting to note that in the 80-nm D-mode HEMT, in which short channel effects (SCEs) are not very strong ($g_{ds}/g_{m,int}$ ~0.13/0.09 at RT/77 K), both τ_{int} and τ_{par} at 77 K decrease from their RT values. This is expected since the 2DEG mobility increases at 77 K leading to an effective increase of electron velocity under the gate as well as a decrease of $R_s + R_d$ [9]. On the other hand, the improvement in f_t of the E-mode device is nearly all due to reduction of the parasitic delay. Given the E-mode device exhibits smaller SCE ($g_{ds}/g_{m,int}$ ~0.04/0.06 at RT/LT for the E-mode device), the same intrinsic gate delay of 0.35 ps at RT and 77 K suggests that the carrier mobility in the E-mode channel has likely degraded owing to the recess etch damage, which is also consistent with the higher "intrinsic channel charging delay" observed for the E-mode devices (Fig. 4b). The larger drain delay in the E-mode devices is attributed to a wider gate recess in the InAlN barrier than the metal gate length [16].

The parasitic delay (τ_{par}) in the E-mode HEMT accounts for approximately 40% of the total delay at RT (Fig. 4b). This stems from the large $C_{gs,ext}$ as a result of the T-gate and thick dielectric passivation employed in the E-mode HEMT. In contrast, rectangular-gates with thin passivation were used in the D-mode HEMT, leading to much smaller extrinsic capacitive parasitics. It was also observed that the output conductance g_{ds} at 77 K is higher than the RT value in the E-mode device, which merits further investigation. Overall, this study suggests that 400-GHz gate-recessed E-mode GaN HEMTs are achievable; Table I shows projections for a 15-nm E-mode device. This performance can be obtained by employing regrown contacts with lower R_c [9], novel passivation schemes to minimize fringing capacitances [17], and metal gates formed by atomic layer deposition to eliminate the un-gated recessed region.

4. Conclusion

We presented an alternative physical explanation to the “intrinsic channel charge delay” that results from a two-step deembedding time delay analysis method and applied it to a 33-nm gate-recessed E-mode InAlN/AlN/GaN HEMTs. The delay analysis indicates that the speed of the device is dominated by parasitics, which account for more than 40% of the total delay, and that intrinsic delay in this device might have been affected by possible channel damage during the gate recess. Ways to improve device speed were also briefly discussed.

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