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Ultrascaled InAlN/GaN High Electron Mobility Transistors with Cutoff Frequency of 400 GHz

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We report on 30-nm-gate-length InAlN/AlN/GaN/SiC high-electron-mobility transistors (HEMTs) with a record current gain cutoff frequency (f_T) of 400 GHz. Although the high drain-induced barrier lowering (DIBL) value is indicative of significant short-channel effects, more than seven orders of magnitude in the current on/off ratio was observed. The high f_T is a result of minimized parasitic effects and at the expense of a low power gain cutoff frequency (f_{MAX}). The gate length dependence and temperature dependence of f_T were also measured.
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Recently, there has been significant improvement of high-frequency performance in GaN-based high-electron-mobility transistors (HEMTs) using a self-aligned gate structure,[1] a lattice matched $In_{0.17}Al_{0.83}N$ barrier,[2–5] an $In_{0.13}Al_{0.83}Ga_{0.04}N$ quaternary barrier,[6] regrown ohmics,[7] and nitrogen-face HEMTs.[8] In this work, we report on a record current gain cutoff frequency (f_T) of 400 GHz in 30-nm-gate-length metal-face InAlN/AlN/GaN/SiC HEMTs with a scaled source drain distance (L_{SD}) of 270 nm.

The lattice-matched $In_{0.17}Al_{0.83}N$/AlN/GaN HEMT structure was grown by metal–organic chemical vapor deposition on a SiC substrate, consisting of, nominally, a 7.5 nm InAlN barrier, a 1.5 nm AlN spacer, a 200 nm UID GaN channel, and a 1.6 µm Fe-doped GaN buffer. Figure 1 shows the post-fabrication barrier layer thicknesses confirmed by transmission electron microscopy (TEM). The Hall effect measurements at room temperature show a channel charge of 1.92×10^{13} cm^{-2} and a mobility of 1240 cm^2 V^{-1} s^{-1}. Devices with gate lengths between 30 and 150 nm were fabricated using the same process flow detailed in Ref. 3. A rectangular gate was adopted to minimize the parasitic effects associated with the T-gate cap. The 30 nm device has a L_{SD} of 270 nm while the 90 and 150 nm devices have a L_{SD} of 860 nm to avoid short circuits during the direct writing of gate fingers. The ohmic contact resistance is 0.16 ohm-mm. The DC and RF characteristics of the HEMTs were measured at both room temperature and 77 K. On-wafer device RF measurements were taken with an HP 8510C vector network analyzer (VNA) in the frequency range from 250 MHz to 30 GHz. Calibration of the VNA was performed using LRM off-wafer impedance standards at corresponding temperatures. The device S-parameter measurements were de-embedded employing on-wafer open and short test structures.

The room temperature DC characteristics of the HEMT with a 30 nm gate length are shown in Fig. 2. A maximum drain current density I_{dmax} of 1.9 A/mm is obtained at $V_{gs} = 0$ V and $V_{ds} = 5$ V. In comparison with the 30 nm HEMT with a large L_{SD} of 865 nm,[3] which was processed from the same HEMT wafer and regrown contacts, the 30 nm HEMT with a scaled L_{SD} of 270 nm in this work exhibits a higher I_{dmax}. Also notable are the kinks in the common-source I–Vs near $V_{ds} \sim 3$–4 V [Fig. 2(a)]. These kinks might stem from poor electron confinement that is exacerbated by the small L_{SD} since they were not observed in the 30 nm HEMT with a large L_{SD} over the same bias

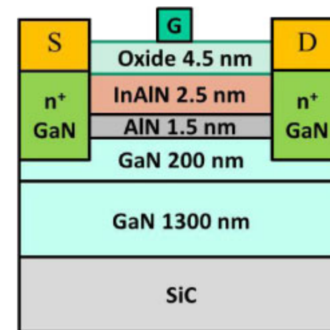

Fig. 1. (Color online) Schematic of the InAlN/AlN/GaN HEMT cross section.

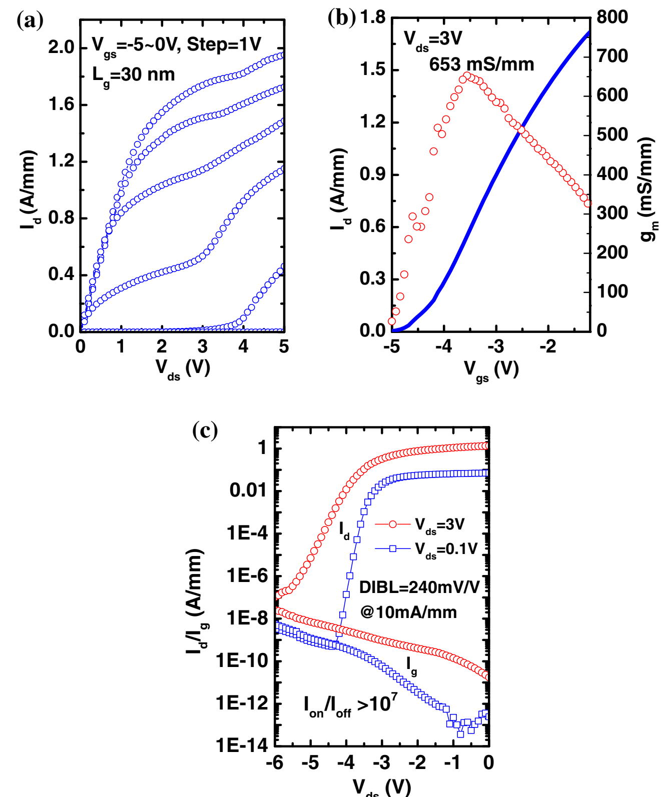

Fig. 2. (Color online) Room temperature DC characteristics of InAlN/AlN/GaN HEMT with a 30 nm gate length and a 270 nm source–drain distance: (a) common source I–V characteristics, and transfer characteristics at $V_{ds} = 3$ and 0.1 V in (b) linear scale and (c) semilog scale.

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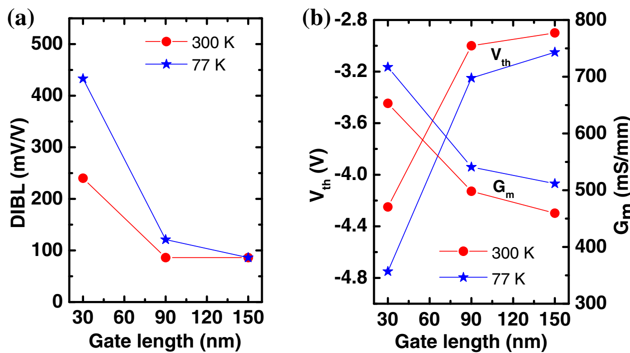


Fig. 3. (Color online) Temperature- and gate-length-dependent (a) DIBL, (b) threshold voltage and transconductance of the HEMTs.

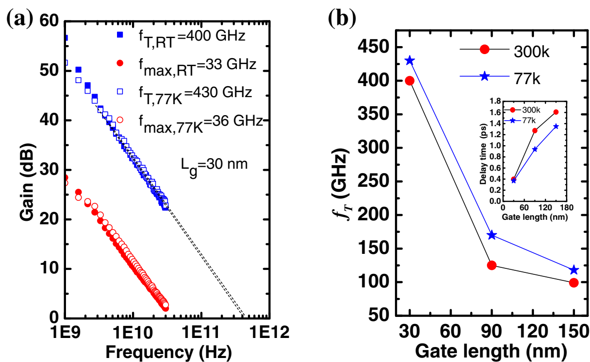
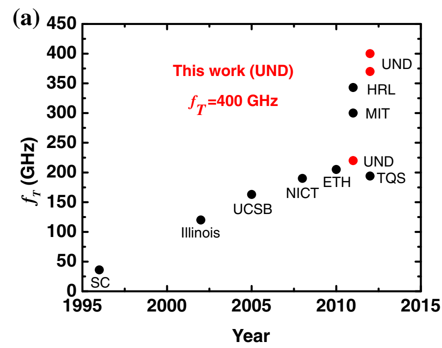


Fig. 4. (Color online) (a) Small-signal RF characteristics of the HEMT with $L_g = 30$ nm. (b) Temperature-dependent RF performance of devices with gate lengths between 30 and 150 nm, and the inset shows total delay time versus gate length.

range, and the HEMT wafer has no back barrier. In the literature, kinks have also been attributed to impact ionization and traps. Hence, further studies are necessary to pinpoint the exact mechanism. The extrinsic g_m of 653 mS/mm [Fig. 2(b)] is moderate since the device has a large barrier thickness of 9 nm. The drain-induced barrier lowering (DIBL) was measured to be 240 mV/V at $I_d = 10$ mA/mm over a bias range V_{ds} of 0.1–3 V (peak f_T bias). Although the high DIBL value is indicative of significant short-channel effects, more than seven orders of magnitude in the current on/off ratio was observed. Figure 3 shows the temperature- and gate-length-dependent DIBL and threshold voltage measured in these InAlN/AlN/GaN HEMTs. An increased DIBL and a negative shift of V_{th} are probably due to an effective V_{ds} increase across the channel at a low temperature.

Figure 4 shows that the peak f_T values increases from 400 GHz under the bias condition of $V_{gs} = -3.6$ V and $V_{ds} = 3$ V at room temperature to 430 GHz under the bias condition of $V_{gs} = -3.9$ V and $V_{ds} = 3$ V at 77 K in the device with a 30 nm gate length, because of the reduced channel resistance. The peak f_T of 90 and 150 nm HEMTs was measured under the bias conditions of $V_{gs} = -2.1$ V and $V_{ds} = 3$ V at room temperature, $V_{gs} = -2.7$ V and $V_{ds} = 4$ V at 77 K. A low f_{max} is observed owing to the high resistance of the small rectangular gate. It is interesting to note that the total delay time reduction at 77 K is much smaller for the 30 nm HEMT than the 90 and 150 nm HEMTs. This can be most likely attributed to the more severe short-channel



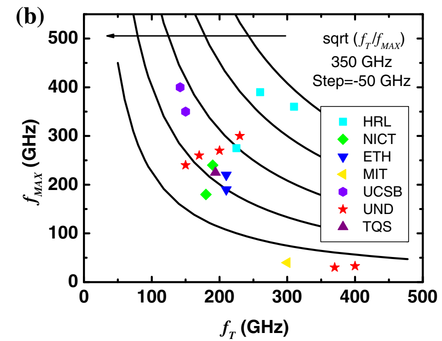


Fig. 5. (Color online) (a) Highly representative f_T values demonstrated over the past two decades, and (b) higher than 200 GHz f_T and/or f_{max} values of D-mode GaN HEMTs reported by various groups.

effects and the influence of the scaled L_{SD} in the 30 nm HEMT, which needs further scrutinization. Figure 5 shows improvements in the f_T and f_{max} of GaN-based HEMTs over the past two decades. Although it appears possible to reach 500-GHz f_T by further reducing gate length, it is imperative to investigate alternative structures that offer a higher mobility/velocity while keeping the best possible electrostatic control in ultrascaled geometry, for example, AlN/GaN/GaN quantum well HEMTs.[9)]

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