Vertical heterojunction of MoS_2 and WSe_2

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The development of experimental methods[1] to create stacked structures of layered 2D materials with atomic-plane precision provides opportunities to study a variety of van der Waals heterojunctions that is difficult to fabricate with traditional growth methods. Here, we report the vertical integration of two 2D TMD materials, MoS_2 and WSe_2, to form van der Waals heterojunction. We show that the electrical properties of the heterojunction are controlled by gate voltage and rectification is observed with forward/reverse current ratio ~ 100.

Vertically stacked MoS_2/WSe_2 heterostructure is fabricated with a dry transfer process similar to the method described in Ref. 2. Fig.1 shows the fabrication process. MoS_2 and WSe_2 flakes of few-layer thickness (<5nm) were first mechanically exfoliated on the transparent transfer mask and Si/SiO_2 (285 nm) substrate separately. Suitable thin flakes were identified by optical microscopy and transferred with our home-built transfer system to form stacked structure on Si/SiO_2. The alignment was controlled with a mechanical manipulator under long working distance objectives. After transfer, the polymer handling layer was removed by acetone. Cross-section TEM image of the heterojunction confirms that MoS_2 is in good contact with WSe_2 (Fig. 2). Metal contacts were patterned on the non-overlapping area by two steps of e-beam lithography and metal deposition: first Ti (5 nm)/Au (50 nm) on MoS_2, then Pd (50 nm) on WSe_2.

Current across the heterojunction was measured under two-probe configuration with back-gate voltage applied on the heavily doped Si substrate. The electrical measurement using the pair of electrodes on the non-overlapping region reveals the doping type of MoS_2 and WSe_2 as a function of the back gate voltage, as well as the nature of the top metal-semiconductor contacts. It is found that both the Ti/Au/ MoS_2 and the Pd/WSe_2 junctions are Schottky like. Fig. 3(a) shows the transfer characteristics of MoS_2 and WSe_2 in non-overlapping region. At Vg=-20V, it is observed that MoS_2 is n-type and WSe_2 is p-type. Assuming MoS_2 in the overlapping region has the same residue charge with the non-overlapping MoS_2, the TCAD simulation (Fig. 4) shows the overlapping MoS_2 has a similar dependence on the back gate voltage since the thin WSe_2 underneath can not completely screen the gate field. It is found that in the overlapping region MoS_2/ WSe_2 form an n-/p-junction at Vg=-20V. Fig. 3(b) shows the I-Vs measured across the stacked MoS_2/ WSe_2 heterojunction under varying back gate voltages. At Vg=-40 and 0V, very low current was observed since one of the TMD layers was fully depleted. At Vg=-20, 20 and 40V, rectifying I-Vs were observed. Though the device behavior is complicated by the Schottky-like metal – TMD contacts, it is very likely that the rectification observed at Vg=-20V stems from the vertical n-MoS_2/p- WSe_2 junction (i.e. the overlapping region). At Vg=20 and 40V, the rectifying behavior is likely a result of the n/n MoS_2/ WSe_2 heterojunction together with the influence of the Schottky-like metal-TMD contacts.

In summary, we have observed rectifying behavior across heterojunction of 2D TMD crystals, which can be explained with simulated band diagrams. This represents the first steps toward achieving stacked p-n junctions using 2D layered materials to realize more advanced devices such as tunnel FETs[3]. This work was supported by the Center for Low Energy Systems Technology (LEAST), a STARnet center.

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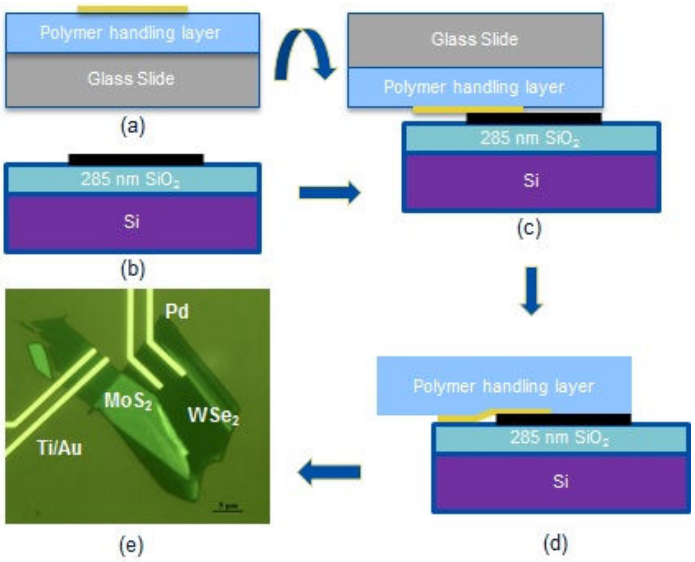

Fig. 1 Fabrication of MoS_2/WSe_2 heterojunction. (a) Exfoliation of MoS_2 on glass slide with polymer handling layer. (b) Exfoliation of WSe_2 on Si/SiO_2 substrate. (c) Alignment under optical microscope. (d) At 100 ^{o}C, polymer handling layer melts and leaves MoS_2 membrane on WSe_2. (e) Image of the device.

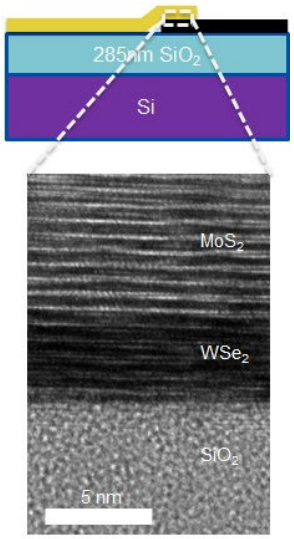

Fig. 2 Cross-section TEM image of MoS_2/WSe_2 heterojunction.

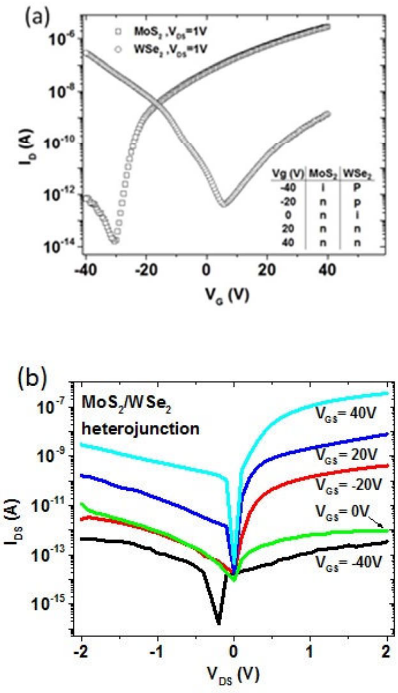

Fig. 3 (a) Transfer characteristics of MoS_2 and WSe_2 in non-overlapping region. The inset lists the type of carriers at different gate voltages. (b) IV characteristics of MoS_2/WSe_2 heterojunction.

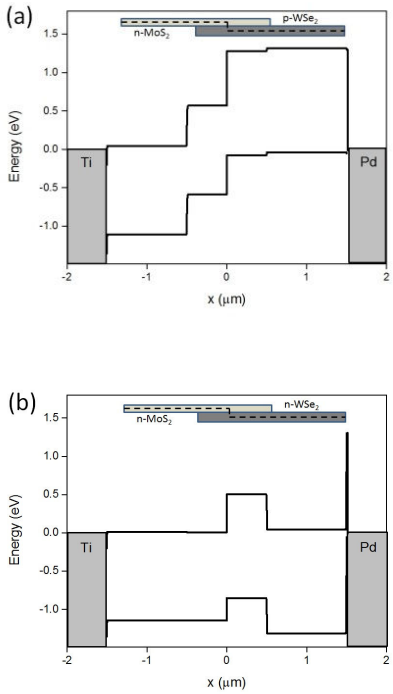

Fig. 4 Simulations of band diagrams: (a) n-type MoS_2 and p-type WSe_2 (b) n-type MoS_2 and n-type WSe_2.