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Challenges and opportunities in the design of Tunnel FETs: materials, device architectures, and defects.

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Abstract

Tunnel FETs are perceived as promising emerging devices to improve the energy efficiency of CMOS integrated circuits. This paper presents results and discussions about some selected topics concerning the working principles and design options of Tunnel FETs, which we believe will play an important role in the development and optimization of these transistors in the near term future.

1 Introduction

The design of most electronic integrated circuits and systems is nowadays power or energy limited, and the performance practically attainable is strongly influenced by the energy efficiency of the signal processing [1]. Consequently, in the last decade VLSI processing at minimum energy has gained an ever growing interest for systems with aggressive requirements on the battery size and lifetime, as well as for energy-autonomous applications. Operation at nearly the minimum energy point, in turn, requires a very aggressive scaling of the supply voltage, V_{DD}, down to only few hundreds mVs [2, 3]. At such extremely low V_{DD} values conventional MOSFETs work in weak-inversion or sub-threshold regime, and the abruptness of the transition between the off and the on state becomes of crucial importance for the ratio of on-current, I_{ON}, to off-current, I_{OFF}, namely for the tradeoff between performance and standby leakage.

In such a context, Tunnel-FETs have been singled out by the International Technology Roadmap for Semiconductors as the most promising emerging transistors that, by reducing the sub-threshold swing, SS, to below 60mV/dec (which is a fundamental limit for MOSFETs at room temperature), may enable a voltage scaling in CMOS based integrated

circuits to below 0.5V [4]. Quite many device architectures, material and technological options have been proposed in the last five to ten years [5, 6], and it is beyond the scope of this paper to provide a comprehensive review of the literature. The purpose of the paper is instead to address a few selected topics, which should help enlighten some fundamental aspects concerning the working principle and the design tradeoffs for Tunnel FETs, and thus provide some hints about future developments in this active research field.

The topics discussed in the paper include: (a) channel material and quantum confinement effects in ultra-thin body or nanowire transistors (in Sec.2); (b) strain engineering and exploitation of staggered of broken band-gap hetero-junctions (Sec.3; (c) impact of interface states and sensitivity to parameters variations (Sec.4); (d) Tunnel FETs based on 2D semiconductors (Sec.5). Some concluding remarks and future outlook are finally reported in Sec.6.

2 Channel materials and geometrical scaling

Tunnel FETs have been experimentally demonstrated by using both silicon and III-V semiconductors as a channel material. Given the maturity of silicon based CMOS technologies, it is probably not surprising that it was with silicon devices that both n-type and p-type transistors were first implemented in the same fabrication flow (albeit with a non optimized design), and that some vehicle circuits consisting of ring oscillators were reported and experimentally analyzed [7]. Given the relatively large energy bandgap of silicon and its indirect bandgap nature, however, the I_{ON} in silicon Tunnel FETs is quite small for V_{DD} below 1V [8, 9], and, in particular, they are small compared to the corresponding currents in MOSFETs. In the context of group IV materials, improvements are expected by the use of strain silicon [10, 7], of SiGe and Ge channel material [11, 10, 12], and of direct bandgap GeSn [13, 14].

III-V semiconductors have a bandgap substantially smaller than silicon and are direct bandgap materials, hence III-V Tunnel FETs have raised legitimate expectations for I_{ON} improvements compared to silicon or group IV material transistors. III-V semiconductors also offer several options for staggered or broken bandgap hetero-junction with a reasonably small lattice mismatch and, in particular, the InAs/$Al_xGa_{1-x}Sb$ system has been identified as potentially interesting for band-to-band-tunneling transistors [15]. Large I_{ON} in hetero-junction Tunnel FETs was confirmed in experiments [16, 17, 18, 19, 20], but with quite unsatisfactory values of sub-threshold swing. Very recent results, however, have reported InGaAs Tunnel FETs with SS values close to 60mV/dec at room temperature [21], which suggests that large SS values in III-V Tunnel FETs are not a fundamental problem, but are instead likely to be linked to larger interface defects compared to silicon devices (see also Sec.4), and may be improved by technology and device design optimization.

In this respect, the modeling support for Tunnel FETs optimization is very important and some of the fabricated device structures have channel lengths in the range of a hundred nanometers or more, typically too large to be simulated with full quantum models. Semi-classical and TCAD models have been successfully employed in the analysis of some to

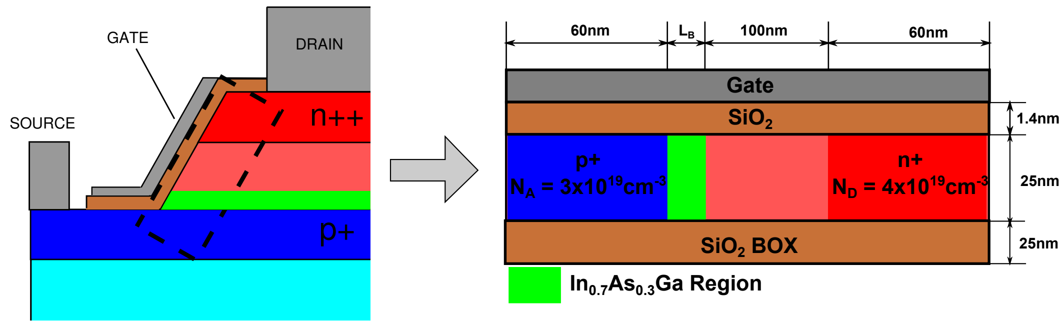


Figure 1: Sketch of the cross section of the MESA $In_{0.53}Ga_{0.47}As$ TFET presented in [16]. A $In_{0.7}Ga_{0.3}As$ region is introduced between the channel and the source. The dashed line rectangle includes the area of the planar hetero-junction TFET sketched in the right plot and used for numerical simulations, where L_B is the length of the $In_{0.7}Ga_{0.3}As$ region. The transport and the wafer plane directions are $\langle 100 \rangle/(001)$.

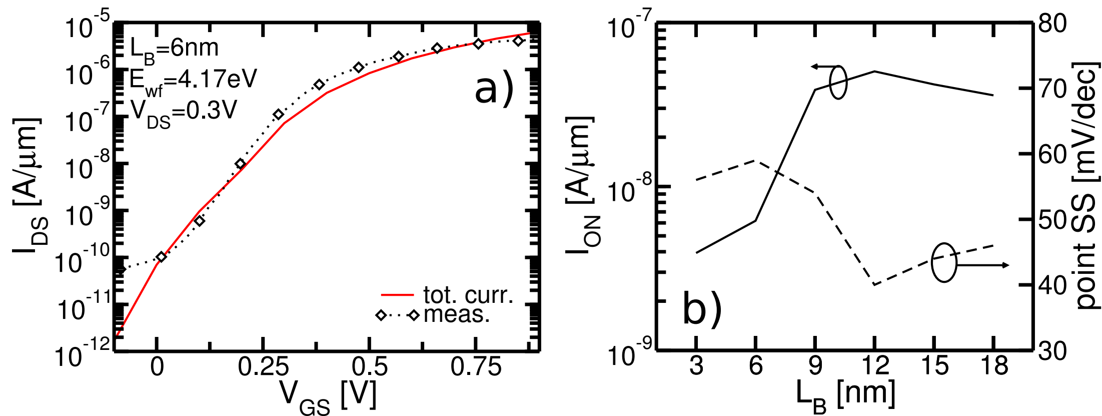


Figure 2: Plot (a) compares the measured trans-characteristics of the $In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ hetero-junction TFET reported in [16] and the simulation results obtained with our multi subband Monte Carlo model. Plot b) reports the simulated I_{ON} and the SS performances versus L_B at $V_{DS} = 0.3V$. The metal gate work-function is tuned to have $I_{DS} = 1pA/\mu m$ at $V_{GS} = 0.0V$. The point SS is computed at $V_{GS} = 0.0V$ and I_{ON} is the I_{DS} at $V_{DS} = 0.3V$.

the best performing, experimentally demonstrated devices. A viable approach used to analyze experiments in [16], for example, is based on a multi subband Monte Carlo transport model [33, 29], modified to include WKB based non-local Band to Band Tunneling (BtBT) models for direct and phonon assisted transitions [34, 35], where heuristic corrections can be introduced to account for the effects on the tunneling rates of quantum confinement [35, 36]. To analyze experiments in [16], a planar SOI structure can be obtained starting from the 3D MESA structure, as shown in Fig.1. The low band gap $In_{0.7}Ga_{0.3}As$ layer between the source and the channel is compressively strained due to the lattice mismatch. The strain splits the degeneracy between the light and heavy hole valence band and changes the band structure [37]. Furthermore the drain and the source regions are heavily doped and

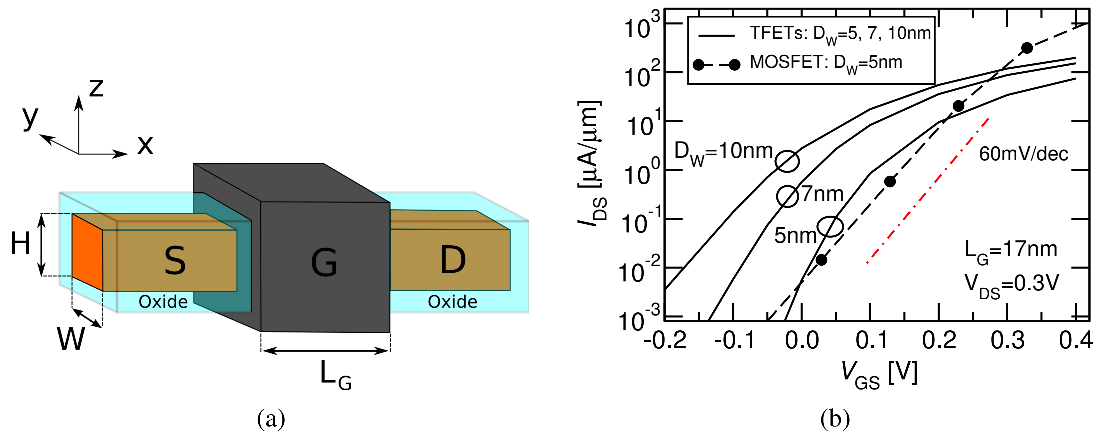


Figure 3: (a) Sketch of the nanowire transistor. We always assume a square section, denote by nanowire diameter D_W=W=H and take the transport direction x to be [100]. (b) I_{DS} versus V_{GS} curves at V_{DS}=0.3V for InAs Tunnel FETs with different diameters D_W and for the InAs MOSFET with D_W=5nm. The gate workfunction is WF=4.66eV for Tunnel FETs and WF= 4.88eV for the MOSFET. For D_W=5nm the I_{OFF} is 5nA/μm for both devices.

band gap narrowing was included in the simulations using the Jain-Roulston model [38].

Fig. 2-a shows that there is a quite good quantitative agreement between the measurements in [16] and the simulation results for the hetero-junction TFET. Simulations can then be used to investigate if the device performance can be improved by changing the length L_B of the low band gap region [39]. Fig.2-b reports the SS and the I_{ON} considering different L_B ranging from $3nm$ to $18nm$ with a step of $3nm$ and we can see that the optimum is found for $L_B = 12nm$.

Aside from the bandgap and hetero-junction properties of group IV or III-V bulk materials, however, it is very important to realize that the design of Tunnel FETs with channel lengths below 20nm requires ultra-thin films or very narrow FinFETs or nanowire transistors, where quantum confinement effects have a profound effect on both the bandgap in nano-structured materials and the band alignment in hetero-junctions.

In this paper all the numerical simulations for nanowire Tunnel FETs and MOSFETs were obtained by considering the device structure sketched in Fig.3(a), where the transport direction x is [100]. The devices were simulated using a self-consistent solution of the 3D Poisson and Schrödinger equations in the NEGF formalism, employing an 8×8 $\mathbf{k}\cdot\mathbf{p}$ Hamiltonian [23], and a coupled-mode space approach [24, 25]. A detailed description of our approach including the treatment of scattering and the inclusion of strain may be found in [25, 26]. The $\mathbf{k}\cdot\mathbf{p}$ model does not account for the Λ and Δ minima of the conduction band (that are instead included in a tight-binding, full-band approach [27]); such an approximation seems reasonable for InAs because the Λ and Δ minima are respectively about 0.72eV and 1.0eV above the Γ minimum in the bulk material [28].

Fig.3(b) shows the I_{DS}-V_{GS} curves for L_G=17nm InAs Tunnel FETs with different D_W=W=H, and for the InAs MOSFET with D_W=5nm; I_{DS} was normalized to D_W. The gate work-function was set to have for the D_W=5nm devices I_{OFF}=5nA/μm (i.e. the

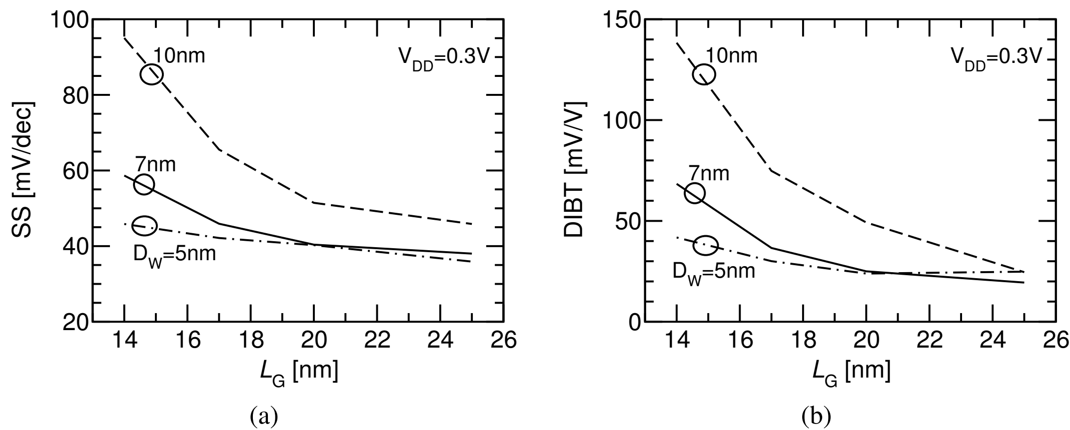


Figure 4: Results for the nanowire transistors of Fig.3. (a) Subthreshold swing SS (obtained as the average value for I_{DS} ranging between 10pA/μm and 10nA/μm), versus L_G and D_W for InAs Tunnel FETs. (b) Drain induced barrier thinning, DIBT, which is defined as the V_T reduction for V_{DS} increasing from 50mV to V_{DD}=0.3V and divided by the V_{DS} variation [22], with V_T defined as the V_{GS} yielding I_{DS}=100nA/μm.

ITRS target for I_{OFF} in low operating power applications [4]), and it can be seen that the I_{DS}-V_{GS} curves for the Tunnel FETs with larger D_W are left shifted because of a smaller quantum confinement.

Most importantly, however, Fig.4 shows that by increasing D_W the SS and the drain DIBT versus L_G substantially degrade for Tunnel FETs; throughout the paper the reported SS values are averaged for I_{DS} ranging between 10pA/μm and 10nA/μm. Clearly D_W=10nm is too large for Tunnel FETs to obtain SS<60mV/dec at L_G=17nm. The introduction of additional design options, such as a gate underlap, does not change significantly the picture compared to Fig.4, so that in the rest of the paper our analysis will focus on nanowire Tunnel FETs with D_W=5nm, with only a few results reported also for D_W=7nm.

The shrinkage in the cross section of the Tunnel FETs enforced by the electrostatic integrity requirements leads to large quantum confinement effects, with a calculated energy bandgap in the DW=5nm InAs device that is about twice as large as in bulk InAs (see also Fig.5(a)). The bandgap enlargement degrades the current in band-to-band-tunneling transistors, and in fact Fig.3(b) shows that the MOSFET has a larger I_{ON} than Tunnel FETs at fixed I_{OFF} even for a supply voltage as low as V_{DD}=0.3V.

3 Strain engineering and hetero-junction transistors

Strain engineering has been dramatically effective in silicon CMOS technologies [29], and the effect of strain can be naturally and implicitly included in a **k**·**p** based transport model by a modification of the band-structure [25]. In our simulations of InAs Tunnel-FETs the strain was included by adding to the **k**·**p** Hamiltonian the strain interaction matrix [23], with the deformation potentials taken from [28].

Fig.5(a) illustrates the energy dispersion for unstrained InAs nanowires, and also for

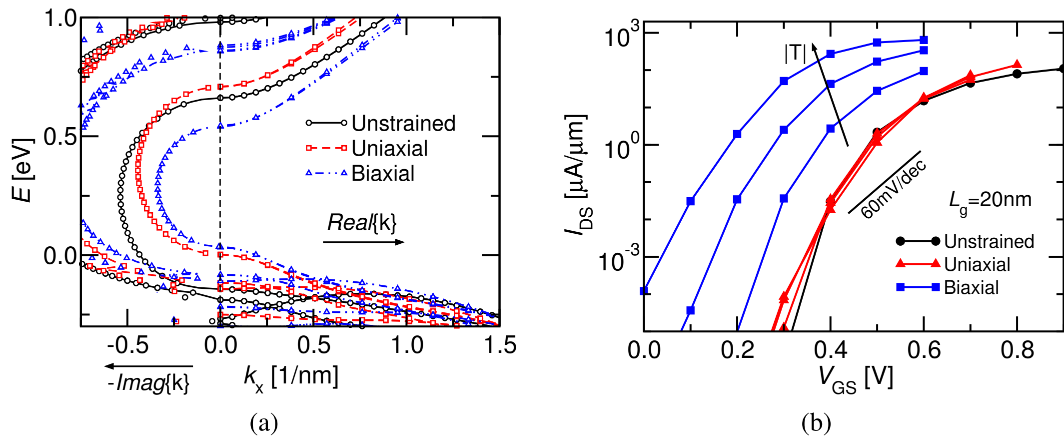


Figure 5: (a) Energy dispersion in the gap for an InAs nanowire (W=H=5nm) and for k_x along the [100] direction. Comparison between unstrained, compressive uniaxial stress (T_{xx}=−2GPa) and tensile biaxial (T_{yy}=T_{zz}=2GPa) stress condition. (b) Corresponding drain current versus gate voltage characteristics for different strain conditions. Compressive uniaxial stress is T_{xx}=−1, −2 and −3GPa and tensile biaxial stress is T_{yy}=T_{zz}=1, 2 and 3GPa.

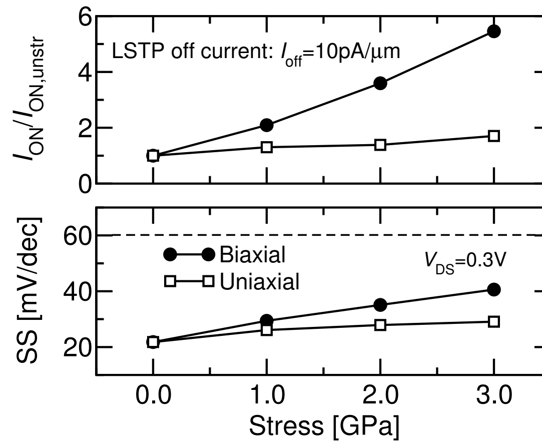


Figure 6: On-current enhancement (top) and SS (bottom) versus the stress magnitude for uniaxial stress (T_{xx}<0) and biaxial stress (T_{yy}=T_{zz}>0) and at fixed I_{OFF}.

a uniaxial and a biaxial strain condition. Both uniaxial compressive and biaxial tensile stress shift up the valence band, but the biaxial stress also lowers the conduction band thus leading the largest reduction of the energy gap and of the imaginary wave-vector in the gap region. Fig.5(b) compares the IV curves of Tunnel FETs for different stress conditions, where it can be seen that the biaxial stress reduces the V_T of the transistors and increases remarkably the I_{DS}, while the uniaxial stress has a smaller impact on the IV curves.

The potentials of stress/strain are further clarified by studying the I_{ON} at fixed I_{OFF}, that is the I_{DS} at V_{DS}=V_{DD} and V_{GS}=($V_{GS,off}$+V_{DD}), where $V_{GS,off}$ is the V_{GS} giving I_{off} [25, 30]. In this respect, the simulated stress induced I_{ON} enhancements at fixed I_{OFF} and the corresponding SS values are illustrated in Fig.6. As it can be seen the biaxial strain enables remarkable I_{ON} improvements, however it brings along also a non negligible SS

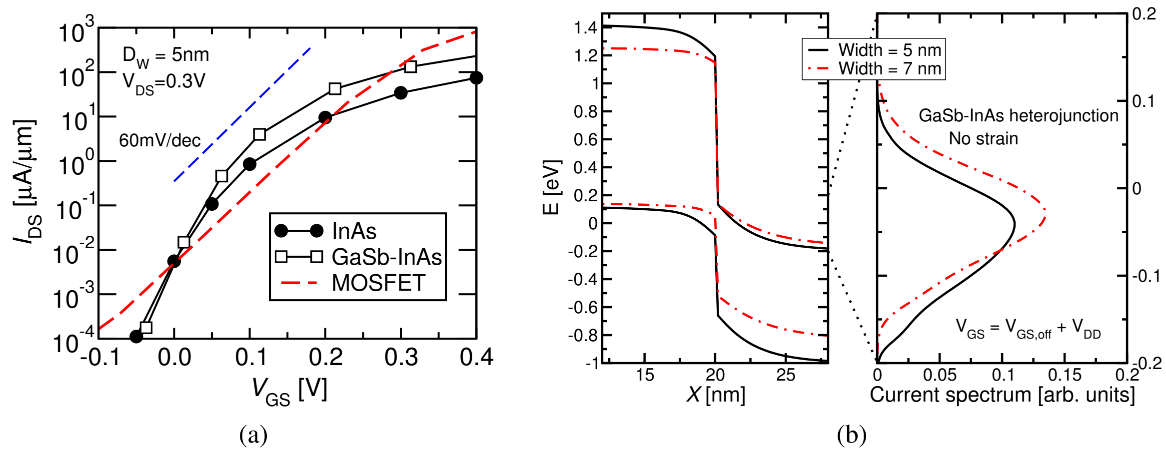


Figure 7: (a) I_{DS} versus V_{GS} curves at V_{DS}=0.3V for an InAs, a hetero-junction GaSb−InAs Tunnel FET and a nanowire MOSFET. L_G=17nm, D_W=5nm and I_{OFF}=5nA/μm). (b) Corresponding subband profile (source Fermi level is taken as zero energy) and current density spectrum for a zoomed energy range between −0.2 and 0.2 eV (where the maximum current density occurs). The bias is V_{GS}=$V_{GS,off}$+V_{DD} with V_{DD}=0.3V

degradation. The analysis of the spectral current density reveals that the I_{ON} improvement mainly stems from the smaller imaginary wave-vector in the energy gap (see Fig.5(a)), in fact the tunneling distance is instead hardly affected by the strain [25].

III-V materials lend themselves to the fabrication of hetero-junctions featuring a large variety of band alignments and, in particular, the conduction band of bulk InAs is about 140 meV below the valence band edge of bulk GaSb, with the two materials having only a minimal lattice mismatch [28]. Such a broken band alignment has been identified as potentially interesting for Tunnel FETs [15].

Fig.7(a) reports the I_{DS}-V_{GS} curves for a homo-junction nanowire InAs Tunnel FET, a hetero-junction GaSb-InAs Tunnel FET and a reference InAs MOSFET. As can be seen the hetero-junction device has an I_{DS} advantage compared to the homo-junction counterpart at fixed I_{OFF}, however the I_{ON} improvement is at best about a factor of two.

The limited advantage of the hetero-junction GaSb-InAs compared to the homo-junction InAs Tunnel FET is partly due to the fact that, despite the properties of GaSb and InAs as bulk materials, the strong quantum confinement effects in the D_W=5nm and D_W=7nm nanowires precludes the implementation of a truly broken bandgap system. This is clearly illustrated by Fig.7(b) reporting the subband profile and the current density spectra of hetero-junctions Tunnel FETs for D_W= 5 and 7nm. Even because of the absence of a broken bandgap profile, the I_{ON} of the GaSb-InAs hetero-junction Tunnel FET is still lower than for the MOSFET for V_{DD} larger than about 0.3V.

Strain and hetero-junction engineering can also be synergically used to improve I_{ON} and, furthermore, it has been recently proposed that the a grading of the AlSb molar fraction in the source region of an $Al_xGa_{1-x}Sb$−InAs hetero-junction Tunnel FETs can be tailored to improve I_{ON} with essentially no sub-threshold swing degradation [31], however these design options admittedly imply an ever increasing complexity of the fabrication pro-

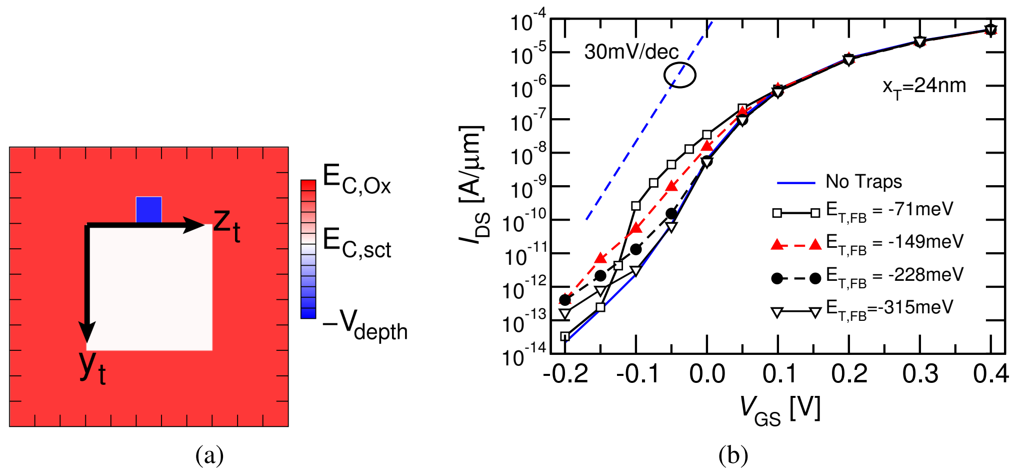


Figure 8: (a) Sketch of the conduction band profile $E_C(\mathbf{r})$ in the section of a nanowire with a trap in the top interface and in the flat-band condition (i.e. for $\phi(\mathbf{r})$=0). $E_C(\mathbf{r})$ is $E_{C,sct}$=0 in the semiconductor, $E_{C,Ox}$ in the oxide and $-V_{\text{depth}}$ in the trap. The coordinates (y_t,z_t) identify the position of the trap. (b) Drain current versus gate voltage characteristics for an InAs Tunnel-FET at V_{DS}=0.4V, with a single trap located 4nm inside the channel at the source end and for different $E_{T,FB}$ values. The (y_t,z_t) position of the trap is the center of one of the nanowire interfaces.

cessing.

4 Defects and variability

While III-V materials are attractive for Tunnel FETs because of the small energy gap and their suitability for hetero-junction engineering, interface traps are a serious concern for III-V transistors [40, 41]. In particular, traps may have a large impact on the IV characteristics of Tunnel-FETs because they can act as stepping stones for the tunneling through the energy gap. In order to investigate this delicate issue, we used a phenomenological description of traps in our NEGF based simulation approach and represented a trap as a cubic potential well $V_t(\mathbf{r}, \mathbf{r}_T)$ superimposed to the conduction band profile, where $V_t(\mathbf{r}, \mathbf{r}_T)$ is $[-V_{\text{depth}}]$ if $(\mathbf{r}-\mathbf{r}_T)\in C_T$ and it is null otherwise, with C_T being the cube representing the trap and $\mathbf{r}_t=(x_T,y_T,z_T)$ being the trap position. The traps were placed essentially at the InAs-oxide interface, as sketched in Fig. 8(a); all simulations were obtained by using a volume of 1 nm^3 for the cube C_T representing the trap. The depth V_{depth} of the quantum well can be used to adjust the trap energy level.

Our approach for the trap modeling accounts for the discrete nature of traps and results in zero-dimensional electrically active states, which can both modify the device electrostatics and play a direct role in the carrier transport. More details about the modeling approach may be found in [42, 43].

Fig. 8(b) shows the I_{DS} versus V_{GS} curves of a Tunnel-FET with a single trap and for different trap energies $E_{T,FB}$, obtained by changing V_{depth}. As can be seen, in a narrow nanowire Tunnel-FET even a single trap can deteriorate substantially both the I_{off} and the

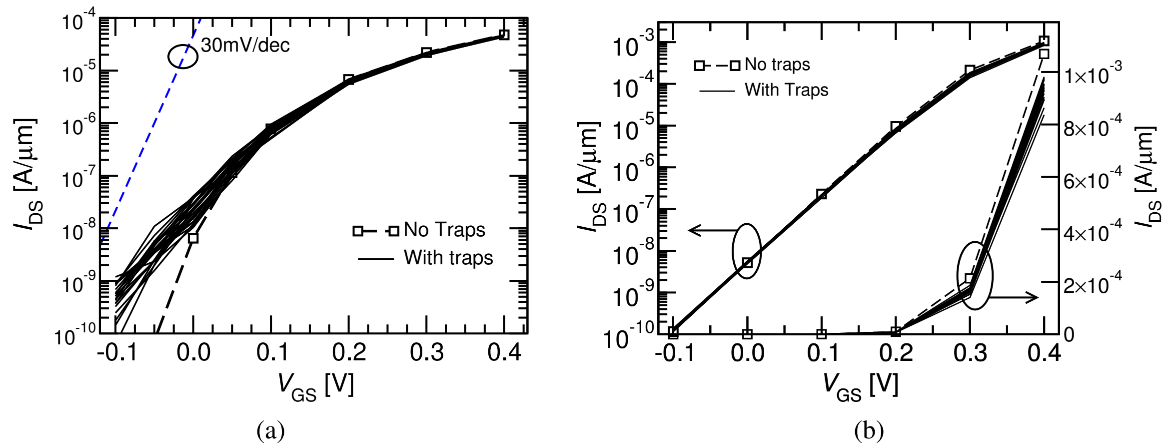


Figure 9: (a) Drain current versus gate voltage characteristics for an InAs Tunnel-FET at V_{DS}=0.4V (open squares) and for about 20 realizations of a spatially random distribution of traps. Trap areal density D_T=2×10^{12}cm^{-2}, E$_{T,FB}\simeq-149$meV; (b) Drain current versus gate voltage characteristics as in (a), but for an InAs MOSFET.

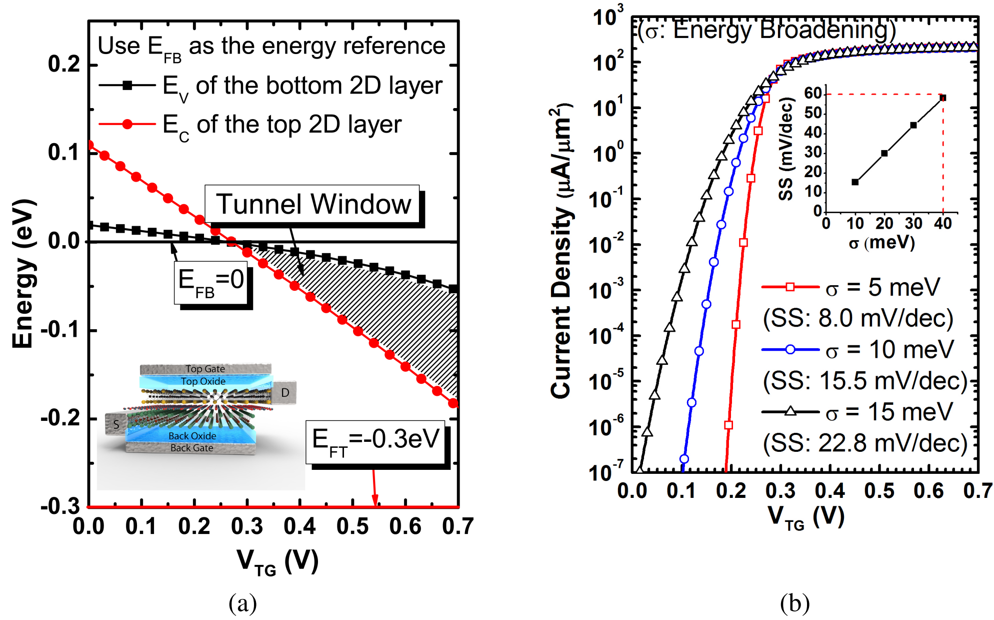
SS of the transistor and, moreover, shallow traps have a larger impact than deep traps in the sub-threshold region.

Physical intuition suggests and numerical simulations confirm that the trap position $\mathbf{r}_t=(x_T,y_T,z_T)$ plays a critical role for its impact on current-voltage characteristics [43], hence the spatially random distribution of traps in the device may be a relevant source of device to device variability. This is exemplified by Fig.9 reporting the I_{DS} versus V_{GS} curves for about twenty different realizations of either a Tunnel FET or a MOSFET having a trap areal density D_T=2×10^{12}cm^{-2}. The results of Figs. 8(b) and 9 suggest that Tunnel FETs are more vulnerable to interface states than MOSFETs because, while in MOSFETs the traps affect the IV curves in DC conditions essentially through an alteration of the electrostatics, in Tunnel FETs the defects act as stepping stones for the band-to-band tunneling process and are thus actively involved in the carrier transport.

Even if the analysis of sensitivity to parameter variations in Tunnel FETs is still at a preliminary stage, the results in Fig.9 confirm the concerns that device variability may be a critical issue in Tunnel FETs [26, 44, 45].

5 Tunnel FETs based on 2D crystals

The bandgap widening in III-V materials produced by quantum confinement in ultra narrow transistors as well as interface defects are serious concerns for Tunnel FET applications. Two-dimensional (2D) semiconductors are arising a great interest for tunneling based transistors [46], also because monolayers of transition metal dichalcogenides (TMDs) MX_2 (M = Mo, W; X = S, Se, Te) offer a large variety of energy bandgaps and band alignments with a layer thickness typically less than 1 nm. Furthermore, the surface of 2D semiconductors is in principle free of dangling bonds, with possible advantages for the performance degra-



(a) (b)

Figure 10: Results for the Thin TFET proposed in [47]. (a) Band alignment versus top gate voltages; (b) current density versus V_{TG} with different values of energy broadening σ. Back gate voltage $V_{BG} = 0$ and drain-source voltage $V_{DS} = 0.3\,V$. Physical parameters are discussed and defined in [47]: tunneling matrix element M_{B0}=$0.01\,eV$; decay constant of wave-function in the interlayer is κ=$3.8\,nm^{-1}$; energy broadening is σ=$10\,meV$ and interlayer thickness is $T_{IL} = 0.6\,nm$ (e.g. 2 atomic layers of BN).

dation produced by interface traps discussed in Sec.4. Moreover TMDs lend themselves to the fabrication of vertical heterostructures, because the weak van der Waals out-of-plane bonding should seamlessly relax substantially the lattice mismatch requirements typical occurring in 3D crystals featuring covalent bonds.

Recently a Two-dimensional Heterojunction Interlayer Tunneling Field Effect Transistor (Thin-TFET) has been proposed and theoretically investigated [47], which implements a density of states switch where the current flows out-of-plane between two monolayers of TMDs. The analysis of this device concept was carried out by using a semi-classical transport model based on the Bardeen's transfer Hamiltonian method [48], in the formulation recently revisited for resonant tunneling in graphene transistors [49, 50]

Fig.10 illustrates numerical simulation results for the Thin-TFET showing the band alignment and the current density versus the top gate voltage V_{TG}. As can be seen the top gate voltage can effectively govern the band alignment in the device and produce the crossing and uncrossing between the conduction band minimum E_{CT} in the top layer and the valence band maximum E_{VB} in the bottom layer that is at the basis of it operation.

In particular, Fig.10(c) reveals that, according to the model employed in [47], the SS is lower limited by the parameter σ describing a finite energy broadening in the 2D layers and that, moreover, the Thin-TFET may be able to provide an SS below the 60mV/dec even for

fairly large broadening energies up to about 40 meV.

6 Conclusions

This paper presented results and developed a discussion mainly based on numerical simulations concerning several aspects of the working principle and the design tradeoffs for Tunnel FETs, which are perceived as promising emerging devices for the highly energy efficient integrated circuits. The topics addressed in the paper cover channel materials and quantum confinement effects, strain and hetero-junction engineering, impact of interface defects and Tunnel FETs based on gapped 2D semiconductors.

Most of the topics touched in the paper are still areas of active research, so that no conclusive assessments about the best options for the design of Tunnel FETs can be made at the time of writing. However some tradeoffs between a good subthreshold swing and a large drive current emphasize fundamental aspects in the working principle of Tunnel FETs, such as the inherent interplay between good electrostatic control and large quantum confinement effects. These aspects are expected to play an important role in the development and optimization of these transistors in the near term future, together with their undesirable sensitivity to interface states and parameter variations.

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