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Exfoliated multilayer $MoTe_2$ field-effect transistors

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The properties of multilayer exfoliated $MoTe_2$ field-effect transistors (FETs) on SiO_2 were investigated for channel thicknesses from 6 to 44 monolayers (MLs). All transistors showed *p*-type conductivity at zero back-gate bias. For channel thicknesses of 8 ML or less, the transistors exhibited ambipolar characteristics. ON/OFF current ratio was greatest, 1×10^5, for the transistor with the thinnest channel, 6 ML. Devices showed a clear photoresponse to wavelengths between 510 and 1080 nm at room temperature. Temperature-dependent current-voltage measurements were performed on a FET with 30 layers of $MoTe_2$. When the channel is turned-on and *p*-type, the temperature dependence is barrier-limited by the Au/Ti/$MoTe_2$ contact with a hole activation energy of 0.13 eV. A long channel transistor model with Schottky barrier contacts is shown to be consistent with the common-source characteristics. © *2014 AIP Publishing LLC*.
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As the scaling of Si-based transistors approaches its limits, attention has been drawn to two-dimensional (2D) materials such as graphene and the transition metal dichalcogenides (TMDs) to provide the ultimate gate electrostatics in field-effect transistors[1] (FETs). Although graphene has remarkably high carrier mobilities at room temperature, more than 15 000 cm^2/V s,[2] it is not well suited to logic applications. Without a band gap, it is difficult to turn the transistor off. TMDs in the form MX_2, where M is a transition metal and X is S, Se, or Te, have a band gap enabling strong ON/OFF current modulation.[3] The X-M-X atoms in each layer are covalently bonded while layer stacks are coupled by van der Waals forces.[4] The weak van der Waals force between the layers makes it easy to exfoliate thin layers from bulk material. The absence of surface dangling bonds, excellent gate electrostatics, dielectric-mediated mobility, and reduced short channel effects are all desirable attributes of TMDs for transistor application.[1] Among TMDs, $MoTe_2$ has a favorable band gap, particularly for tunnel FETs.[5] Theoretical band gaps for bulk and single layer $MoTe_2$ are 0.81 eV (indirect) and 1.13 eV (direct),[6] respectively.

To obtain channel materials, $MoTe_2$ powder (American Elements Co., 99.9% purity, MO-TE-05-P) was exfoliated using 3M Scotch 810 Magic Tape on an $n+$ Si substrate with 285 nm of thermally grown SiO_2. Tape residue after exfoliation was removed by soaking in acetone, followed by an isopropanol rinse, and N_2 blow dry.[7] The exfoliation process yielded flake thicknesses in the range of 3.8–30.4 nm. Flake thicknesses were measured by atomic force microscopy (AFM) using a Bruker Dimension Icon AFM in an argon glove box. For a $MoTe_2$ single-layer thickness of 0.6984 nm,[8] the corresponding layer thicknesses ranged from 6 to 44 monolayers (MLs). The $MoTe_2$ flakes were clearly visible using an optical microscope.

Source/drain contacts were patterned using a Vistec 5200 electron beam pattern generator. The metals were evaporated by electron-beam in the order 5 nm of Ti followed by 100 nm of Au using a lift-off process. An unpatterned back contact using the same metals was applied to the wafer backside. The contacts were annealed at 300 °C for 3 h in forming gas. The transistor cross-section and top-view optical micrograph are shown in Fig. 1.

The photoresponse of an 8 ML channel $MoTe_2$ FET was measured using a Fianium SC 450–2 laser generating a broadband continuum excitation with the device biased in the subthreshold region. Linear variable bandpass filters were used to select the excitation wavelength with a full

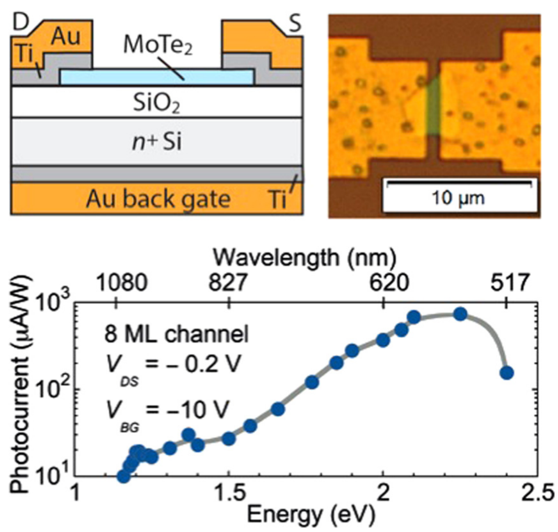

FIG. 1. Schematic cross section of a $MoTe_2$ FET along with an optical top-view micrograph of the source-drain contacts where the $MoTe_2$ channel flake is visible. The lower plot shows the spectroscopic photoresponse of an 8 ML transistor biased in the subthreshold region.

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width at half maximum of approximately 5 nm. The excitation beam was modulated by a mechanical chopper at 20 Hz; a Stanford Research Systems 830 lock-in amplifier was used to detect the photocurrent at the chopping frequency. At every wavelength, the spectral power of the source was measured at the sample position. Normalization of the lock-in signal by the measured spectral power yielded the photocurrent spectra of Fig. 1. A single lower excitation measurement at 0.82 eV showed no photoresponse. The next higher excitation energy was 1.14 eV, where a photoresponse was observed. Presumable this corresponds to a band-to-band absorption and the band edge is between 0.82 and 1.14 eV. The peak at 1.4 eV is consistent with a Fabry-Perot resonance in the SiO_2.

Raman measurements were performed in the backscattering configuration using a WITec Alpha 300 system at room temperature (100× objective, 1800 grooves/mm grating, 488 nm laser, 64 kW/cm^2, 180 s/point, average of 3). Figure 2(a) shows the two bulk $MoTe_2$ peaks corresponding to the out-of-plane A_{1g} mode at 175 cm^{-1} and the in-plane E^1_{2g} vibration at 236 cm^{-1}, seen previously in Refs. 9 and 10. Peaks at 347, 405, and 495 cm^{-1} are also seen in the measurements as has also been observed by Pradhan.[10]

Figure 2(b) plots the drain current per unit width vs. back-gate voltage for 7 $MoTe_2$ FETs with different flake thicknesses. The gate leakage current in all of the measured transistors was negligible at a few picoamperes. With zero back gate bias, the transistors are *p*-type. With less than 10 $MoTe_2$ layers, the transistors showed ambipolar channel conduction where negative gate bias caused hole accumulation and positive gate bias caused electron accumulation. Devices with more than 10 layers of $MoTe_2$ showed *p*-channel conduction. The maximum ON/OFF current ratio was 1×10^5, corresponding to the $MoTe_2$ FET with a 6 ML channel thickness. This channel conduction is opposite to what we observed previously[11] using the same exfoliated materials and source/drain contacts on Al_2O_3 on $p+$ Si.

In addition to Refs. 10 and 11, there is another recent $MoTe_2$ FET report by Lin *et al.*[12] Pradhan has observed an ON/OFF current ratio greater than 10^6 on few layer $MoTe_2$ FETs grown by chemical vapor deposition using iodine. These materials were then exfoliated onto SiO_2, but in contrast they do not observe ambipolar conduction. Field effect mobility of 20 cm^2/V s was reported by Pradhan, compared to 6 cm^2/V s in our work.

As shown in Fig. 2(b), the ON/OFF current ratio increases with reduction in the layer thickness as may be expected due to the reduction of back-gate control over the entire channel thickness. For the same reason, the subthreshold swing generally increases with layer thickness, but not without exception, see for example the FET labeled 44 ML. This apparently anomalous characteristic could result if a void exists dividing the layers into two groups. The layers closest to the back gate then exhibit a steeper subthreshold swing while the layers further from the gate contribute a gate independent parallel leakage. The highest channel current densities obtained varied from 0.24 to 4.4 μA/μm at $V_{DS} = -1$ V and $V_{BG} = -80$ V. As will be shown, the channel currents on $MoTe_2$ are limited by Schottky source/drain contacts; this may be expected to improve with proper choice of contacts work function as has been shown on MoS_2[13] and WSe_2.[14]

In this study, a FET with 30 layers of $MoTe_2$ was used to extract the activation barrier for transport. The temperature dependence of the FET transfer characteristics was measured in the temperature range from 100 to 300 K (Fig. 3(a)). With the transistor biased on with negative back gate voltages, the drain Schottky junction is forward biased and the current is limited by the Schottky barrier at the

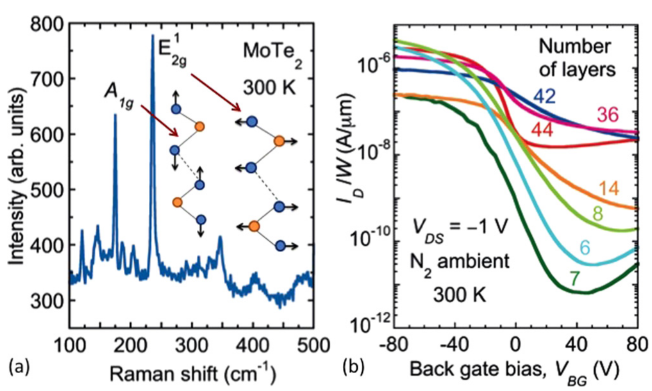

FIG. 2. (a) Raman spectrum of bulk (powder) $MoTe_2$. The out-of-plane A_{1g} and in-plane E^1_{2g} vibrations are identified in the inset. (b) Measured drain current per unit width vs. back gate voltage for 7 transistors at $V_{DS} = -1$ V. The $MoTe_2$ channel thicknesses were measured for each transistor by atomic force microscopy.

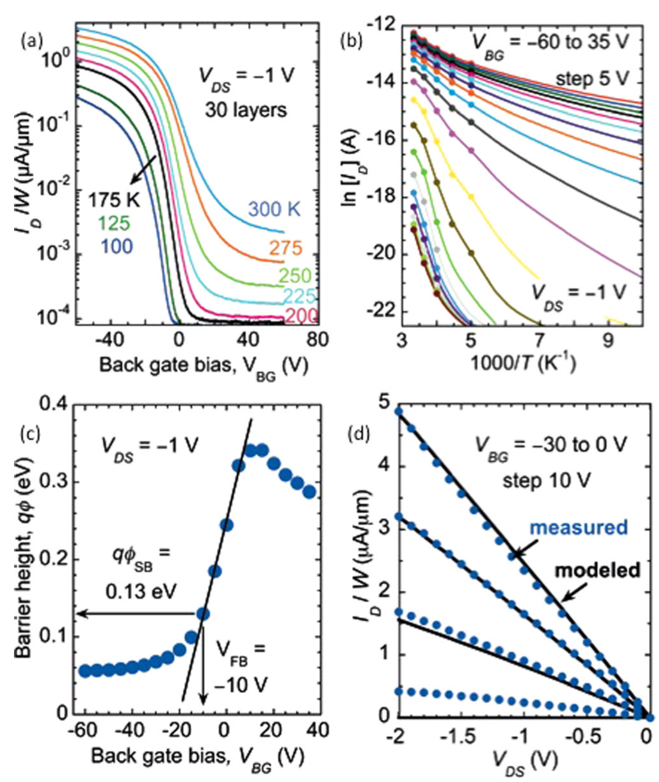

FIG. 3. (a) Temperature dependence of a $MoTe_2$ FET transfer characteristics for a device with $W = 1.4$ μm, $L = 1$ μm and 30 layers. (b) Arrhenius plots obtained from the data of Fig. 3(a) for $-60 < V_{BG} < 35$ V. (c) Apparent barrier height for a 5 nm Ti/100 nm Au contact on $MoTe_2$ plotted versus back gate voltage indicating a Schottky barrier height of 0.13 eV. (d) Measured common source characteristics vs. analytic model for the same transistor.

source junction. A semilog plot of the current vs. inverse temperature can then be used to extract the barrier height, Fig. 3(b), assuming an Arrhenius activation barrier, $I_O \exp[-q\phi_B/kT]$. The solid circles on the curves in Fig. 3(b) were used to compute the activation barrier. As outlined by Das,[13] a plot of the apparent activation barrier vs. back gate bias, see Fig. 3(c), exhibits a linear decrease as the transistor hole barrier is lowered. The point where the barrier decrease deviates from the linear region marks an apparent Schottky barrier height and the flat band voltage as indicated in Fig. 3(c). The hole barrier in this multilayer structure is found to be 0.13 eV and flat band voltage is −10 V. This is consistent with the Ti/$MoTe_2$ barrier measurements by Lin[12] in hole accumulation, but in contrast to the 5 meV barrier height reported by Pradhan.[10] Pradhan applies a T^2 correction to the measured current, which lowers the measured barrier height, but this does not likely explain the difference. We have found that modeling of the transistor current voltage characteristics with Schottky contacts that a barrier height of 0.12 eV is suitable to explain the measured current.[15] Returning to Fig. 3(c) for positive gate biases larger than 15 V, our measured barrier height saturates and then decreases. The decrease is consistent with the onset of electron tunneling at the drain Schottky barrier. It should be noted that interpretation of the temperature dependence of Schottky barriers on multilayer structures is complicated by the unknown current distribution in the individual layers, which can change as a function of back gate voltage[16] and temperature. In fact, we believe that there is a strong impact of layer thickness on the apparent Schottky barrier that is extracted. It is likely that device characteristics for thinner flakes will result in a different barrier height since in particular the minimum off current in $MoTe_2$ FETs is a strong function of the layer thickness as apparent from Figure 2(b).

An analytic model was developed to understand the effects of the Schottky barrier contacts on the FET common source characteristics. The band diagram and model description are included in the supplementary material.[15] As can be seen from Fig. 3(d), a good fit to the experimental data is obtained. The unknowns in the model are the mobility, $\mu_P = 6.4\,\mathrm{cm^2/V\ s}$, the Ti/$MoTe_2$ Schottky barrier, $\phi_{SB} = 0.12\,\mathrm{eV}$, channel acceptor doping density, $N_A = 1 \times 10^{17}\,\mathrm{cm^{-3}}$, and the gate flat-band voltage, $V_{GFB} = 0.5\,\mathrm{V}$. The mobility and Schottky barrier are in good agreement with the measurements and the channel density and flat-band voltage are reasonable.

In conclusion, we report the fabrication and characterization of multilayer exfoliated $MoTe_2$ FETs on SiO_2. Device characteristics for different $MoTe_2$ channel thicknesses (ranging from 6 to 44) were examined. The fabricated devices generally showed *p*-type channel conduction at zero back gate bias and ambipolar channel conduction for flake thicknesses less than 10 layers. At room temperature, the maximum ON/OFF current ratio obtained was 1×10^5 for a FET with 6 layers. The channel current densities for different layer thicknesses varied from 0.24 μA/μm to 4.4 μA/μm at $V_{DS} = -1\,\mathrm{V}$ and $V_{BG} = -80\,\mathrm{V}$. A hole Schottky barrier height for Ti/30 L $MoTe_2$ was measured to be 0.13 eV. This barrier height is in good agreement with the value of 0.12 eV obtained from fitting a Schottky barrier FET model to the measured common source characteristics.

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