Characteristics of $In_{0.17}Al_{0.83}N/AlN/GaN$ MOSHEMTs with steeper than 60 mV/decade sub-threshold slopes in the deep sub-threshold region

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Realization of steep sub-threshold slope (SS) transistors requires exploiting carrier transport mechanisms such as tunneling [1], and also alternative gate barrier materials (i.e. ferroelectric materials) with internal voltage gain [2]. Theoretical studies on piezoelectric barriers indicate that it is possible to achieve internal voltage amplification and steep SS in GaN MOSHEMTs by utilizing electrostriction in conjunction with piezoelectricity in AlN and InAlN [3] [4]. Less than 60 mV/decade SS was experimentally observed in GaN MOSHEMTs with InAlN barriers, in which the steep transition was tentatively correlated with the inhomogeneous distribution of polarization in the barrier [5]. However, steep SS were only observed at drain current (I_d) near nA/mm regimes, which leads to difficulties in interpretation of experiment data. Understanding of the mechanism of the steep SS in these devices is still unclear and needs more characterization and modeling. In this work we demonstrate InAlN/AlN/GaN MOSHEMTs with less than 60 mV/decade SS in deep sub-threshold regions (1E-8 A/mm and below) at room temperature (RT). Drain voltage and temperature dependent characteristics are provided with analysis for advancing our understanding of this phenomenon.

InAlN/AlN/GaN MOSHEMTs with ALD Al_2O_3 (device structure shown in Fig. 1) gate dielectrics and alloyed ohmic contacts were fabricated on SiC substrates. The devices have 5 nm InAlN barrier, 1 nm AlN interlayer and a GaN channel on 1.8 μm Fe doped GaN buffer grown by metal organic chemical vapor deposition (MOCVD). Gate openings in the ALD SiN_x passivation define 2 μm gate lengths, where 10 nm ALD Al_2O_3 gate dielectric and Ni/Au gate metallization are placed. Some devices are recessed in the gate area by CF_4 plasma treatment in a reactive ion etching (RIE) system to achieve close to E-mode operation. The InAlN barrier thickness after recess etching is estimated to be 2.5 nm based on the etch rate of CF_4 plasma on InAlN. Details of device fabrication are described in [6].

At room temperature, representative I_d-V_{ds} characteristics of InAlN/AlN/GaN MOSHEMTs with 5 nm InAlN barrier are shown in Fig. 2 (a). Dual-directional I_d-V_{gs} sweeping at V_{ds}=3 V on the same device shows SS of 46 mV/decade during V_{gs} sweeping from negative bias to 0 V and 81 mV/decade when V_{gs} is swept back, with a small hysteresis of about 60 mV. C-V characteristics of MOS gate diodes with 5 nm InAlN and 2.5 nm InAlN (with CF_4 plasma treatment) are shown in Fig. 3 (c). To avoid introducing large uncertainties and arbitrary numbers into the determination of threshold voltages, V_{th} is defined by the steepest slopes of the two C-V curves, respectively. The two diodes exhibit the same capacitances at -0.2 V<Vg<0.2 V, which is an indication of the existence of "negative" capacitance in the InAlN or AlN barriers of the diode with 5 nm InAlN. In Fig. 3(d), capacitances are calculated using the electrostriction model [3] [4], where a similar trend can be seen. In Fig. 4 (a), I_d-V_{gs} characteristics (5 nm InAlN) with V_{gs} sweeping from off-state to on-state and V_{ds} from 0.1 V to 9 V biases are shown, from which the SS dependence on the drain current is calculated in Fig. 4 (b). At small V_{ds}=0.1V, the minimum local SS is 57 mV/decade. With increasing V_{ds}, the minimum local SS decreases, and reaches 46 mV/decade at V_{ds}=3 V and 5 V. This phenomenon may be linked with the non-uniform distribution of electric field under the gate, especially near the drain side edge of the gate, where the electric field is largely dominated by the drain bias. When V_{ds} is increased further, the local SS increases partly due to the higher minimum drain leakage. When V_{gs} is swept from on-state to off state, the transfer characteristics are plotted in Fig. 5 (a), and the SS is calculated in Fig. 5 (b). For all biases of V_{ds}, the minimum SS values are >75 mV/decade in this sweep condition. The electrostriction model qualitatively agrees with this trend, since a forward sweep and a large electric field may bias part of the barrier in the regions of "negative" capacitance [4]. However, since I_d is very small ~nA/mm, a dynamic charging model [5] can also explain this effect, in which a higher drain bias leads to a faster charging rate. From temperature dependent dual-directional I_d-V_{gs} characteristics of the MOSHEMT with 5 nm InAlN thickness, SS and body factor m ($SS = m \cdot \ln(10) \cdot kT/q$) are calculated and plotted in Fig. 6. For V_{ds}=3 V with V_{gs} up sweeping, the body factor m=0.6, indicating voltage amplification from the gate voltage to the GaN surface potential and "negative" capacitance in the barrier. The possibility of steep SS in conventional FETs with active barriers can potentially lead to high performance (high current) FETs if the mechanisms underlying the steep behavior are understood, and the hysteresis removed. This work is supported by the SRC LEAST center.

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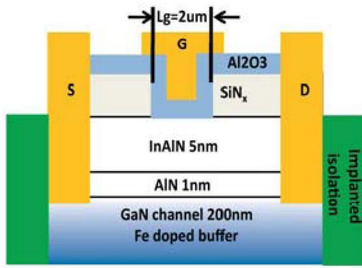

Figure 1: InAlN/AlN/GaN MOSHEMT structure with 5 nm InAlN barrier.

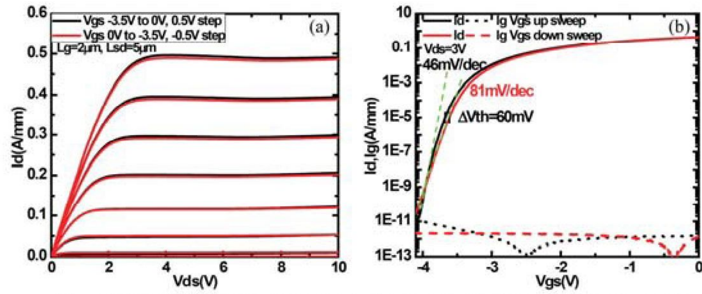

Figure 2: (a) Id-Vds characteristics of a InAlN (5 nm)/AlN/GaN MOSHEMT with Vgs stepping up and stepping down (RT); (b) Id-Vgs characteristics of the same device with Vgs sweeping up and sweeping down and calculated hysteresis and SS (RT).

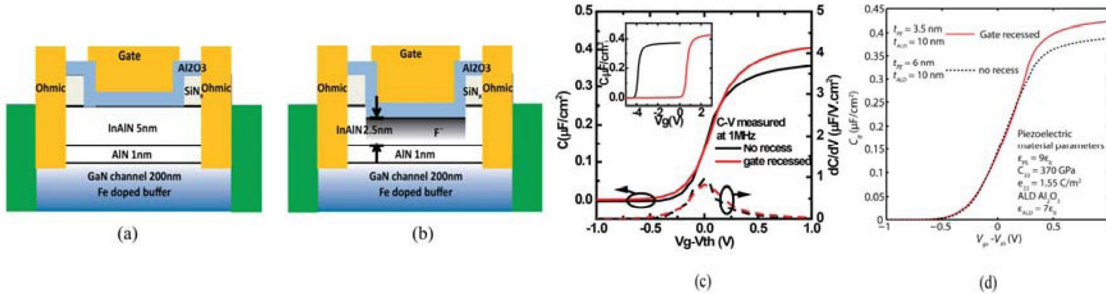

Figure 3: InAlN/AlN/GaN MOSHEMT (a) without (5 nm InAlN) and (b) with (2.5 nm InAlN)gate recess and (c) comparison of C-V characteristics near Vth at RT. (d) Theoretical calculation of C-V characteristics of these two structures by considering electrostriction effect using the model described in [3] and [4].

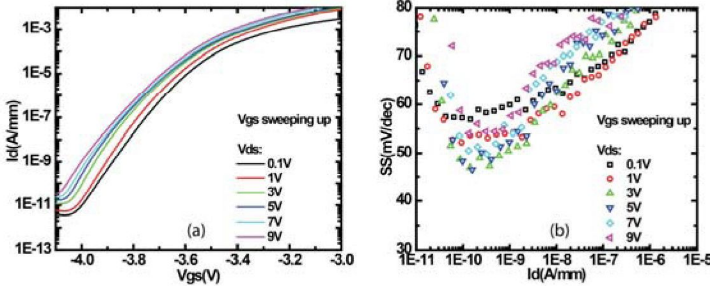

Figure 4: (a) Id-Vgs characteristics of a InAlN (5 nm)/AlN/GaN MOSHEMT at various Vds with Vgs sweeping up (RT); (b) SS calculated as functions of Id when Vgs is sweeping up.

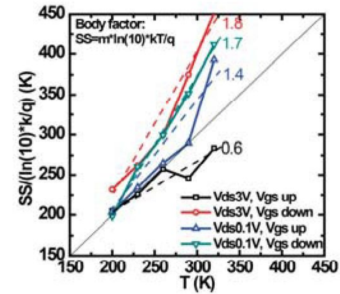

Figure 6: SS dependence on temperature measured on the InAlN (5 nm)/AlN/GaN MOSHEMT at Vds=0.1V and 3V with Vgs sweeping up and down. Body factors are calculated according to linear fitting of SS/(ln(10)*k/q)~T.

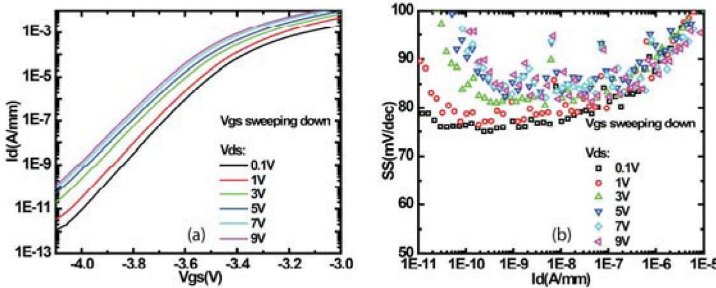

Figure 5: (a) Id-Vgs characteristics of a InAlN (5 nm)/AlN/GaN MOSHEMT (same device as in Fig. 4) at various Vds with Vgs sweeping down (RT); (b) SS calculated as functions of Id when Vgs is sweeping down.