Electronic transport properties of top-gated epitaxial-graphene nanoribbon field-effect transistors on SiC wafers

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Top-gated epitaxial-graphene nanoribbon (GNR) field-effect transistors on SiC wafers were fabricated and characterized at room temperature. The devices exhibited extremely high current densities (~10 000 mA/mm) due to the combined advantages of the one-dimensionality of GNRs and the SiC substrate. These advantages included good heat dissipation as well as the high optical phonon energy of the GNRs and SiC substrate. An analytical model explains the measured family of I_D–V_{DS} curves with a pronounced 'kink' at a high electric field. The effective carrier mobility as a function of the channel length was extracted from both the I_D–V_{DS} modeling and the maximum transconductance from the I_D–V_{GS} curve. The effective mobility decreased for small channel lengths (<1 μm), exhibiting ballistic or quasiballistic transport properties. © *2014 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4861379]

I. INTRODUCTION

Graphene nanoribbons (GNRs) are being investigated as a possible channel material for transistors as well as for interconnects for future electron devices. This is because graphene allows exceptional electrostatic control due to its native two-dimensional (2D) confinement, and it also has a high current carrying capacity with excellent thermal conductivity.[1–3] In many reports, graphene or GNRs sit on SiO_2 substrates, whose phonon energy (~57 meV)[4] is significantly below the longitudinal zone boundary phonon energy (~160 meV) of intrinsic graphene.[5] Therefore, the saturation velocity of carriers in graphene field-effect transistors (FETs) has been found to be limited by the remote phonon scattering caused by the SiO_2 substrate, and not by the intrinsic properties of graphene, indicating the importance of substrate choice for graphene devices.[6] In order to exploit the inherent advantage of graphene, substrates with higher phonon energies such as SiC (~100 meV)[7] are attractive. In this paper, we report the measurement of very high current densities (~10 mA/μm), differential conductance (~1.3 mS/μm), and estimated transconductance (~1 mS/μm @ $V_{DS} = 10$ V) in epitaxial-graphene nanoribbon FETs (EGNR-FETs) on SiC. Compared to GNRs on SiO_2 substrates (~2 mA/μm)[8] and 2D graphene on SiC substrates (~2 mA/μm),[9] GNRs on SiC substrates show a far higher current carrying capacity because the substrates show efficient heat dissipation and higher optical phonon energy. The combined effect of GNRs and the SiC substrate allows the EGNR-FETs to achieve the highest current density measured in any semiconductor structures to date, including 2D graphene. We model the high-field device characteristics and extract the carrier mobility in the GNRs as a function of the channel length. The numbers indicate ballistic or quasiballistic transport properties as the channel length of the device is scaled down below 1 μm.

II. EXPERIMENTAL PROCEDURES

Epitaxial graphene (EG) was formed by thermal decomposition of semi-insulating, nominally on-axis Si-face 6H-SiC substrate coupons with square side lengths of 10 mm using a commercial Aixtron VP508 SiC growth reactor at 1620 °C for a duration of 120 min in an Ar ambient at a constant pressure of 100 mbar. Using a continuous process, samples were etched in hydrogen at temperatures 1520 °C for 50 min to attain a scratch-free SiC surface with uniform steps and terraces before graphene synthesis.[10] Pressure and temperature stabilization when transitioning from hydrogen etching to graphene synthesis in an Ar ambient took between 3 and 5 min. After growth, the samples were cooled in Ar to 800 °C in order to suppress unwanted Si sublimation and limit contaminates that may adhere to the surface. This recipe yields a uniform epitaxial graphene layer that is reproducible from run-to-run.[10]

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The EG was then patterned into 20 nm-wide nanoribbons using electron-beam lithography (EBL). Finally, EGNR-FETs with a 70 meV energy gap were fabricated.[11] Figure 1(a) shows the schematic top and cross-sectional views of the device structure. Source/drain electrodes were defined using EBL. The Cr/Au (5/100 nm) was then deposited using an electron-beam evaporation, and a lift-off process was carried out. Atomic layer deposition Al_2O_3 of 20 nm was deposited on the EGNRs using a 0.5 nm-thick oxidized evaporated Al nucleation layer. A scanning electron microscope (SEM) image of an EGNR in the channel is shown in Fig. 1(b) with an inset depicting the Raman map of the graphene on the SiC. The measured capacitance of the gate stack was $\sim 0.3\ \mu F \cdot cm^{-2}$ with a 100 x 100 μm^2 area.

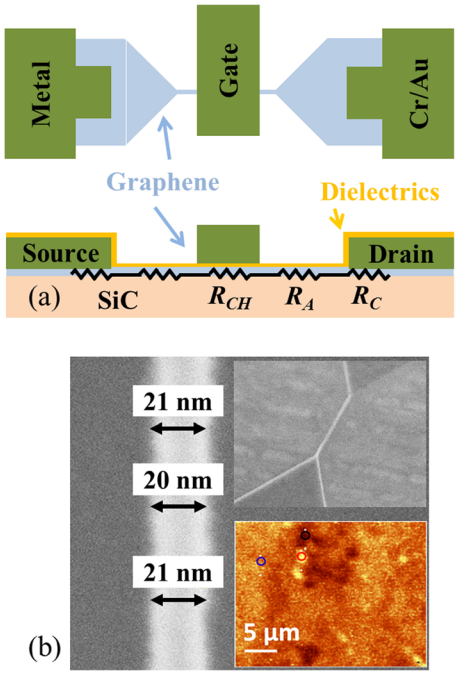

FIG. 1. (Color online) (a) Schematic device structure of the top-gated EGNR-FETs with parasitic resistances ($R_S = R_A + R_C$) aside from the intrinsic resistance of GNR (R_{CH}). (b) SEM image of a 20 nm-wide GNR covered by an HSQ mask with the top right insert showing a bird's eye view of the representative device structure before deposition of the gate dielectric and gate metal. The bottom insert shows a Raman map of I_{2D}/I_G image indicating the uniformity of the epigraphene on the SiC.

III. RESULTS AND DISCUSSION

Figure 2(a) shows the measured I_D versus V_{GS} of the 20 nm-wide EGNR-FETs. The results indicate that the EGNR-FETs shown-type behavior. A family of I_D–V_{DS} curves at various V_{GS} was correlated with the modeling (discussed below) in Fig. 2(b). The observed maximum current density ($\sim$10 000 mA/mm) of the EGNR-FETs, as shown in Fig. 2(b), is the highest current density ever reported from either graphene-based FETs (Refs. 1, 12, and 13) or III-nitride high-electron mobility transistors (HEMTs).[14] The current density was defined as current per unit GNR width (I_D/W). The current-carrying capacity of 2D graphene FETs has been reported to be higher than traditional FETs and comparable to III-Nitride HEMTs.[13] The 1D transport of GNRs enables EGNR-FETs to show the highest current density by preventing lateral momentum in the graphene and enabling the materials to benefit from the spreading of the 3D heat.[1] The efficient heat dissipation of the EGNR and SiC substrate also contribute to the enhanced current density. SiC has a very high thermal conductivity compared to SiO_2 [SiC $\sim 350\ Wm^{-1}K^{-1}$,[15] $SiO_2 \sim 1.3\ Wm^{-1}K^{-1}$,[16] and suspended graphene $>4000\ Wm^{-1}K^{-1}$ (Ref. 17)] and this reduces localized heating, which can generate resistive defects.

The measured I_D–V_{DS} curves were compared with a traditional long channel transistor model,[18] where $C_{OX} = 0.29\ \mu Fcm^{-2}$, $\mu = 950\ cm^2.V^{-1}.s^{-2}$, and $V_T = -12$ V. The C_{OX}, μ, and V_T are best fits, and those values are comparable to the measured one. The measured I_D only matched well with the model in the linear region. However, the pronounced "kink" at the large negative gate bias $V_{GS} = -4$ V with the higher V_{DS} was not captured. This revealed that the behavior of the EGNR-FETs was predictable using the long channel model in the linear region, but due to the narrow band gap of the GNR, the saturation region equation was not valid.

In order to model the pronounced "kink" accurately, the analytical expression shown in Eq. (1)[19] was used, where $n_0 = 9 \times 10^{12}\ cm^{-2}$, $\mu = 950\ cm^2 \cdot V^{-1} \cdot s^{-2}$, $\nu_{SAT} = 10^8\ cm \cdot s^{-1}$, $C_{OX} = 0.3\ \mu F \cdot cm^{-2}$, $V_{DP} = -8.5$ V, and $R_S = 1000\ \Omega$

$$I_D = \frac{e\mu(W/L)\int_{I_D R_S}^{V_{DS}-I_D R_S} \sqrt{n_O^2 + [C_{OX}(V_{GS} - V_{DP} - V(x))/e]^2}\, dV(x)}{1 + \mu(V_{DS} - 2I_D R_S)/L\nu_{SAT}}. \quad (1)$$

The analytical model captures the measured I_D in all V_{DS} regions, as shown in Fig. 2(b). Figure 2(c) shows the differential conductance as a function of V_{DS} at two different V_{GS} values: $V_{GS} = 6$ V and $V_{GS} = -4$ V. On the one hand, at $V_{GS} = 6$ V (region I), the Fermi level is far above the charge neutrality point so that the Fermi level in the channel remains above the neutral point for the drain voltages used, and thus, electrons are the major carrier over the entire V_{DS} region. The decrease in the differential conductance is due to scattering as the electric field increases. On the other hand,

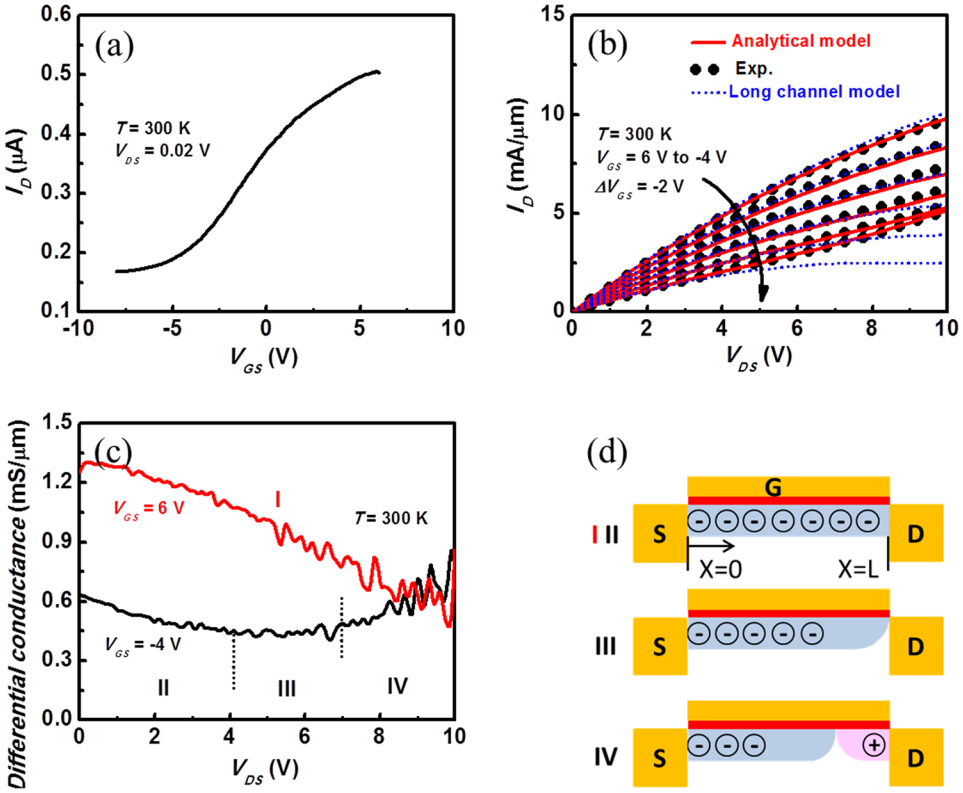

FIG. 2. (Color online) Transport properties of top-gated 20 nm-wide EGNR-FET. (a) I_D–V_{GS} characteristics at $V_{DS} = 0.02$ V. (b) Analytical model (line, discussed in text), long channel mode (dashed line), and measured I_D–V_{DS} characteristics (dotted line) with V_{GS} varied from 6 V to −4 V. (c) Differential conductance as a function of drain-to-source voltage (V_{DS}) at $V_{GS} = 6$ V and −4 V. (d) Schematic drawing of the carrier concentration in the channel regions at $v_{GS} = 6$ V (I) and −4 V (II, III, and IV), respectively.

at $V_{GS} = -4$ V, the Fermi level is just above the charge neutrality point, and the differential conductance shows three distinct behavior regimes (II, III, and IV) as illustrated in Fig. 2(d). At a low electric field ($V_{DS} \leq 4$ V, region II), the channel near the drain is influenced to a lesser degree by the drain voltage, and the electrons are still the major carriers. However, at a high electric field ($V_{DS} \geq 7$ V, region IV), the channel near the drain is significantly influenced by the drain voltage, and holes become the major carrier type in the channel near the drain since the Fermi level moves below the charge neutrality point. The differential conductance then increases as the electric field increases due to the increase in the number of hole carrier density. Region III is thus the transition region.

Using the analytical modeling applied in Fig. 2(b), the channel length dependence of mobility was then explored. Figure 3(a) shows a comparison of the modeled I_D with constant mobility and the measured I_D as a function of the channel length. In the case of long channel devices ($L = 3$ μm and 5 μm), the model matches well with the experimental results. However, the discrepancy between the model and experiment increases as the channel length decreases. This indicates that the effective mobility parameter of a short channel model should be smaller than that of a long channel model in order to match the modeling with experimental results ($L < 1$ μm). Figure 3(b) shows the I_D–V_{DS} plot at $V_{GS} = 0$ V at various channel lengths. In order to match the measured I_D with the modeled I_D, the effective mobility is varied as a single fitting parameter while other parameters are fixed to be the same as the values used in Fig. 2(b).

The effective low-field mobility was also extracted from the maximum transconductance (g_m) of the I_D–V_{GS} curve (not shown) as a function of the channel length, as shown in Fig. 3(c). Figure 3(d) shows the effective mobility as a function of channel length, where the effective mobility were extracted both from the I_D–V_{DS} fitting, as shown in Fig. 3(b), and the maximum g_m of the I_D–V_{GS}, as shown in Fig. 3(c). The effective mobility trend from these different methods clearly shows that mobility degrades significantly as the channel length is scaled down below 1 μm. This indicates that the channel length becomes comparable to the mean free path and an onset of quasiballistic transport properties, where the mobility is expected to be degraded. A ballistic mean free path can be extracted from[20]

$$\mu_{\text{Effective}} = \mu_0 \times L/(\lambda + L), \tag{2}$$

where μ_0 = the mobility of a long channel device (700 $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-2}$) from Fig. 3(d), λ = mean free path, and L = channel length. From this relation, the extracted mean free path (λ) is between 100 and 800 nm for EGNR-FETs, comparable to 300 ± 100 nm for 2D graphene FETs.[20] It should be noted that parasitic capacitance, scattering, and the internal junction of the metal/graphene with a scaling

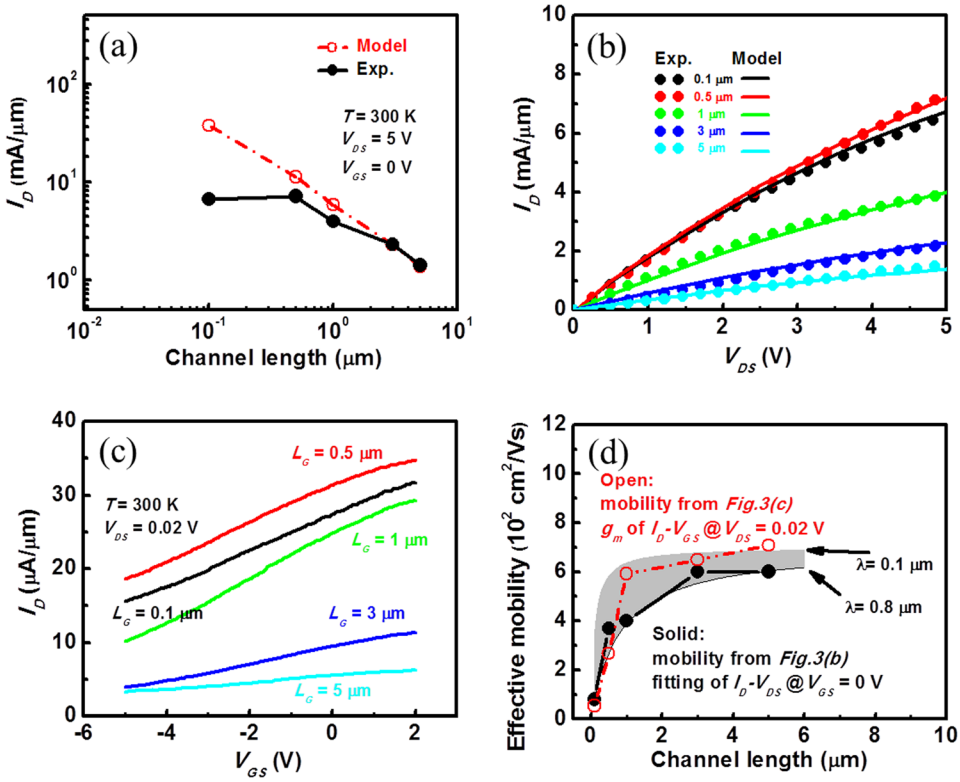

FIG. 3. (Color online) (a) Comparison of the analytical modeled I_D with constant mobility and measured I_D at $V_{DS} = 5$ V and $V_{GS} = 0$ V. (b) Comparison of the analytical model (line) and measured I_D–V_{DS} characteristics (dashed line) as a function of channel length at $V_{GS} = 0$ V. Only the mobility in the model was released to match the measured results as a function of channel length. (c) I_D–V_{GS} characteristics at $V_{DS} = 0.02$ V depending on various channel lengths (0.1, 0.5, 1, 3, and 5 μm). (d) Effective mobility obtained from fitting the I_D–V_{DS} parameter as a function of channel length, as shown in (b), and maximum g_m of I_D–V_{GS}, as shown in (c). The mean free path is discussed in the text.

down of the GNR channel length were neither discussed nor considered in the modeling. These factors lead to some uncertainty to the mean free path in the GNRs.

IV. CONCLUSIONS

Top-gated EGNR-FETs were fabricated and characterized at room temperature. These devices exhibited very high current densities ($\sim$10 mA/μm) and conductance ($\sim$1.3 mS/μm) due to the combined advantages of the GNRs and SiC substrate—namely, the excellent heat dissipation and high optical phonon energies. The transistor characteristics were explained using an analytical model, and the extracted effective mobility showed comparable behavior to 2D graphene. The effective mobility degraded as the channel length decreased below 1 μm, where the quasiballistic transport begins to contribute.

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