Energy-Efficient Clocking Based on Resonant Switching for Low-Power Computation

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***Abstract*—A mechanism for the reduction of dynamic energy dissipation based on energy recovery resonant switching in a computing circuit is described. The resonant circuit with controlled switches conserves energy by recovering 90% of energy that would be otherwise lost during logic state transitions. The new approach of incorporating an energy recovery storage capacitor in the resonant circuit helps to initialize the logic operation and moves the energy back and forth to the load capacitance. This energy-conserving approach preserves thermodynamic entropy, ideally preventing heat generation in the system. This proposed method is used for generating an energy-efficient "flat-topped" (quasi-trapezoidal) waveform, which is required to perform the low power digital logic computation, especially for clocking in the system applications.**

***Index Terms*—Clocking, energy dissipation, energy recovery resonant switching, entropy, energy-efficient waveform, low-power computation, low-voltage/low-power (steep subthreshold slope) transistor switch.**

I. Introduction

SCALING of semiconductor transistors (MOSFETs, HEMTs, etc.) improves the device performance. These improvements have driven integrated circuit (IC) performance gains for over 40 years. However, static and dynamic energy dissipation have become the main limiting factors for further device scaling in complementary metal-oxide-semiconductor (CMOS) circuits [1]–[4]. This dissipation and the associated heat generation can exceed the limits of practical cooling and impede the scaling of the device speed and packing density in ICs [2], [6]. To maintain scaling for terascale integration with CMOS logic, it is necessary to dramatically reduce heat generation by reducing energy dissipation in a computing system [2], [5]. Reusing or conserving the stored energy (used to represent the information) during logic transitions can reduce the heat generation in a computing system. This low power technique requires carefully controlled waveforms to obtain low dissipation.

The field-effect transistors (FETs) in CMOS logic are used as switches by controlling the height of a potential energy barrier between the source and the conductive channel with the applied gate voltage [4], [7]. Conventional CMOS logic operation dissipates energy to heat during each logic transition in the system even in a system with ideal switches (zero $I^2R_{\rm on}$ loss and zero off current) [7]. The fundamental limit on dissipation is expressed in the Landauer's principle concerning irreversible logic [8]. According to Landauer, there is a minimum energy dissipation of $k_BT\log(2)$ (k_B is Boltzmann's constant and T is the temperature of the system) to heat in the system when information in a physical system is erased in a conventional irreversible logic operation, but no minimum limit of energy is dissipated to heat when information is not destroyed, as in a reversible logic computation [8]–[12].

Clock signals are essential to perform logic operation in ICs and any microprocessor based digital systems. The clock signal provides a time base to various parts of the system so that logic operations are performed in the correct order. In ultra-scaled technology with large device densities, the clock power becomes a major contributor to dynamic power dissipation during logic computation. Thus, it is important for energy-efficient designs to reduce the power dissipation caused by clocking of the system. However, the resonant clocking [13]–[18] based on energy-recovery switching is a promising approach for reducing dynamic power dissipation without reducing the FET operating voltage.

In this paper, we present an energy conserving resonant circuit with the externally controlled FET switches that generates an energy-efficient "flat-topped" output waveform. In particular, we introduce a novel approach to incorporate an energy recovery capacitor in the resonant circuit with the controlled switching for electrical energy storage and initializing the logic operation. Here, the energy recovery storage capacitor acts as a virtual voltage source, and helps to move energy back and forth to the load capacitance, without requiring an additional power supply. This energy conserving resonant circuit can be utilized to perform digital logic computation in a thermodynamically reversible fashion to recycle the energy from cycle to cycle. The flat-topped (quasi-trapezoidal) output waveform generated by the energy recovery resonant switching (ERRS) [19] in a circuit can be used as an "adiabatic clocking" [20]–[22], [24], [25] and especially as a "Bennet clocking" [26] in reversible logic computation [10], [11], [25].

The methodology we propose here, an effective way of generating an energy-efficient waveform with very low energy loss, can also be used for drive circuitry in a number of applications such as a high-voltage emissive display driver, a liquid crystal display (LCD) driver, and more. Here, an LCD or any other display device (i.e., a plasma display) acts as a load capacitance, from which the energy is recycled during display operation [27]–[29].

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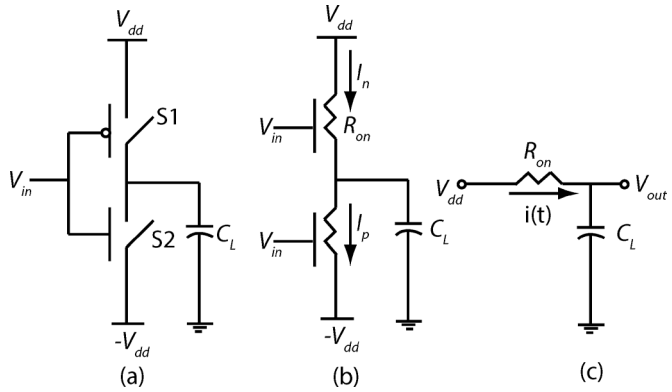

Fig. 1. (a) Conventional CMOS logic inverter. (b) Resistive models of switching transistors (pull-up & pull-down) in CMOS logic inverter. (c) An RC equivalent circuit model of inverter during logic operation for one-half cycle of input control signal.

This paper is organized as follows. Section II describes the concept and an implementation of the energy-efficient clocking waveform based on energy recovery resonant switching. In Section II-A and II-B, we discuss the energy dissipation in conventional CMOS logic and the mechanisms for the reduction of energy dissipation in field-effect devices and circuits. In Section II-C, we propose a resonant energy conserving logic with controlled switching and present a detailed analysis for the generation of quasi-trapezoidal clocking waveforms. In Section II-D, we derive the relations for energy dissipation and recovery efficiency based on practical aspects of the resonant circuit. In Section II-E, we present the design of energy recovery system based on the proposed method. In Section III, results and discussions are provided. Finally, the conclusion of this work is addressed in Section IV.

II. Ideas and Implementation

A. Conventional CMOS Logic

We first discuss a conventional CMOS inverter shown in Fig. 1(a). When the input voltage is low (logic '0'), the output voltage becomes V_{dd} (logic '1'.) by charging the load capacitor C_L through the PMOS transistor S1. Similarly, for high input voltage with logic '1', the output node is discharged to $-V_{dd}$ level (logic '0'.) through the NMOS transistor S2. To calculate the energy dissipation, we use a simplified RC model of the logic circuit, shown in Fig. 1(b) and (c). For an *abrupt* transition, analysis of this circuit gives the charging current, $i(t) = (V_{dd}/R_{\rm on})\exp(-t/R_{\rm on}C_L)$. The dynamic energy stored in the load capacitor C_L during the charging phase is

$$E_{\rm dynamic} = \frac{V_{dd}^2}{R_{\rm on}}\int_0^\infty \exp\left(-\frac{2t}{R_{\rm on}C_L}\right)dt = \frac{1}{2}C_L V_{dd}^2. \quad (1)$$

An equal amount of energy is dissipated as heat in the PMOS transistor. During the discharge phase, the stored energy is dissipated in the NMOS transistor switch as heat. In CMOS logic, energy is dissipated during a logic state transition, but, ignoring leakage current, no energy is required to hold the state for logic '1' or logic '0' [7].

B. Reduction of Energy Dissipation in Devices and Circuits

The energy dissipation in the logic circuit occurs when charging and discharging the load capacitor associated with the FET device. In particular, this dissipation is associated with the current flowing through an equivalent series resistance in the circuit. Therefore, the dynamic energy dissipation in a conventional CMOS circuit through an equivalent series resistance is equal to $C_L V_{dd}^2$ per period for an operating voltage V_{dd}. Excessive heat resulting from large energy dissipation might impede the circuit performance. However, there are primarily dynamic and static power dissipation associated with the logic circuit. Dynamic power dissipation associated with switching of logic states in a circuit can quadratically be reduced by lowering the operating voltage V_{dd} of the switching transistor. In a conventional transistor, a constraint for voltage scaling comes from a link to static dissipation caused by the subthreshold slope limit of 60 mV/dec at room temperature due to thermally distributed charge carriers emitted over the potential barrier from the source contact to the conductive channel [3], [4]. Static power dissipation is also considered to be a constraint for voltage scaling. It is associated with the power dissipation, when there is no computation performed in the system (transistors are turned off) [30]. Indeed, it is due to leakage current mechanisms [31] in the device/circuit, and draws extra power from the power supply voltage V_{dd}. Further reductions of power dissipation will require a change in the physics of the device operation that enable further reductions in the operating voltage V_{dd}. A novel switching device with sub-60 mV/dec enables more abrupt turn-on with the gate voltage, which allows further voltage scaling, and hence the operating voltage V_{dd} could be reduced [3], [4].

Since C_L is difficult to scale, additional reduction of dynamic energy dissipation requires conserving the energy during the switching of transistors. Conserving the stored energy effectively reduces the energy loss. This can be achieved by employing an energy recovery resonant switching (ERRS) in a conventional circuit. In this resonant mechanism, the signal energy stored on the load capacitor can be recycled through an oscillation of energy between electric and magnetic form instead of being dissipated as heat across the device resistance. The charging and discharging a capacitor for digital logic computation with reduced power loss can be accomplished using an adiabatic switching principle [20]–[23]. In adiabatic switching, the supply voltage V_{dd} is cycled by ramping up to a maximum, and then ramping down to a minimum, and the output load capacitor is charged during the ramp-up period and then discharged during the ramp-down period of the voltage. The energy dissipation for a supply voltage ramped from 0 V to V_{dd} over a time interval t_r, as shown in Fig. 2, is then $E_{\rm diss} = (1/2)C_L V_{dd}^2 \cdot (R_{\rm on}C_L/t_r)$ [4]; the energy dissipation can be arbitrarily small if $t_r \gg R_{\rm on}C_L$. Although this computation requires lower clock rates, it can greatly reduce dynamic energy dissipation. However, an adiabatic logic requires the alternating

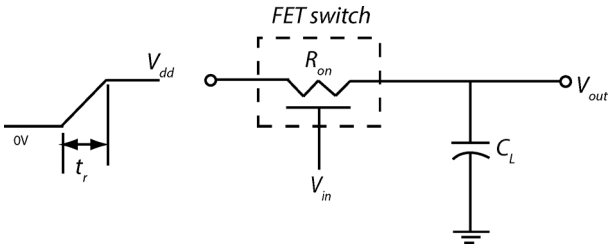

Fig. 2. Equivalent circuit model for adiabatic logic incorporating a FET switch with ramp operating voltage supply.

operating voltage waveform, which can efficiently be achieved by our proposed method, presented in the following.

C. Resonant Energy Conserving Logic

The dynamic energy dissipation in a computing circuit, that associated with processing information, can be reduced to zero in reversible computation, but the energy used to encode information in the circuit must be recovered and reused. This can be accomplished by incorporating a series resonant circuit to provide energy to, and recover energy from, the logic circuit in a gradual and controlled manner. The energy recovery resonant switching utilizes a sinusoidal waveform generated by the standard oscillator with an externally controlled switch to generate an energy-efficient flat-topped clocking waveform. Here, the oscillator is realized by the series LC resonator, or the high-Q MEMs/NEMs resonator [32].

The implementation for generating an energy-efficient clocking waveform based on the LC resonating circuit with controlled switching is described in detail here. Fig. 3(a) depicts the schematic of the proposed energy-conserving circuit that generates an output pulse with a sinusoidal ramps at the rising and falling edges. The resonant circuit incorporates a high-Q inductor $L_{\rm ER}$ connected in series with capacitors C_L and $C_{\rm ER}$, along with switching transistors. Here, the equivalent series resistance $R_{\rm on}$ consists of $R_{ds,{\rm on}}$, the ON resistance in the FET switch, when operating in the linear regime, and inductor series resistance $R_{\rm series}$ in the resonant circuit, i.e., $R_{\rm on} = R_{ds,{\rm on}} + R_{\rm series}$. The equivalent circuit of series RLC resonator with $R_{\rm on}$ and $L_{\rm ER}$ connected in series with capacitors C_L and $C_{\rm ER}$ is shown in Fig. 3(b). Energy is taken from $C_{\rm ER}$ and delivered to the load capacitor C_L during the charging phase and is returned in the discharge phase, as shown in Fig. 3(a). Resonating energy between the integrated inductor and the load capacitor effectively conserves the dynamic energy in switching of load capacitance. The operation of the proposed circuit for clocking is based on the input control signals and inductor current waveforms shown in the timing diagram of Fig. 4.

The novelty of this method is associated with two design approaches. One introduces the controlled switching operation using transistors in the resonant circuit. The other employs a virtual voltage source, which is created by adding an energy-recovery storage capacitor $C_{\rm ER}$ in the circuit. This capacitor $C_{\rm ER}$ is precharged to a voltage of $V_{dd}/2$ to begin. The stored energy in this capacitor is used to initialize the logic operation. The restoring voltage $(V_{dd}/2)$ in the storage capacitor $(C_{\rm ER})$ is

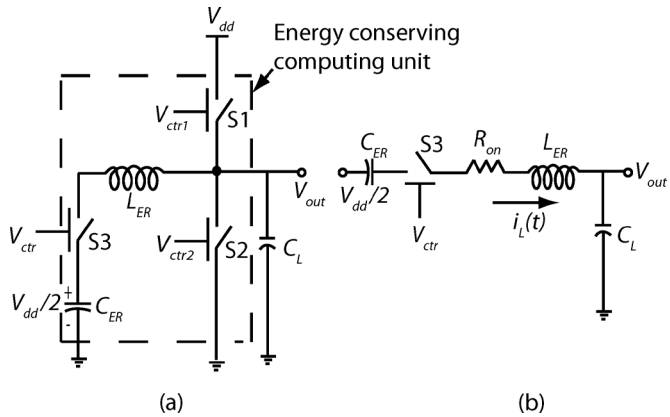

Fig. 3. (a) The proposed energy conserving resonant circuit used for generating the flat-topped (trapezoidal) clocking waveform with a very low energy loss (ideally zero energy dissipation). An energy recovery capacitor, $C_{\rm ER}$, is incorporated for electrical energy storage and initializing the logic operation. (b) An equivalent series resonant RLC circuit model for energy conserving clocking circuit.

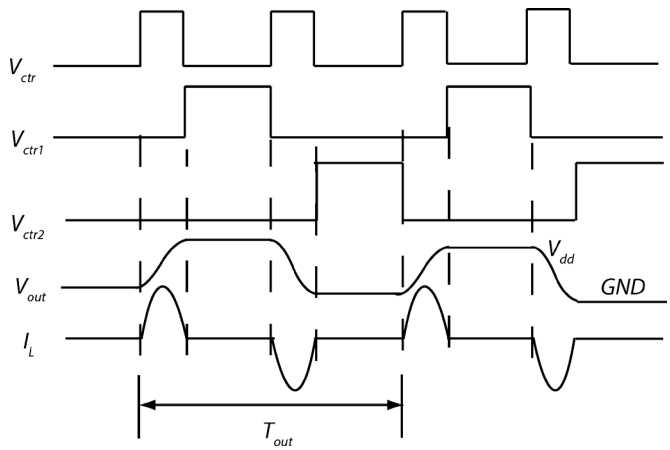

Fig. 4. The timing diagram for generating the flat-topped clocking pulses by the energy recovery logic circuit. Here, the timing diagram is crucial for controlling the switching operation in the energy recovery resonant circuit. The periods of clocked waveform can be determined by the designed values of inductance and capacitances in a circuit.

assumed to be stable during charging and discharging of C_L, requiring the designed value of $C_{\rm ER}$ to be larger than that of C_L. Here, the energy recovery capacitor $C_{\rm ER}$ is used as a reservoir, as energy moves back and forth to load capacitor C_L, without requiring an additional power supply. This approach aids the reversible energy transfer between the load capacitor and the non-dissipative inductor during logic state transitions. An externally controlled switch S3 controls the energy transfer during each state transition. The other two controlled switches S1 and S2 are responsible for holding the output at logic '1' or '0'. In the charging phase, the switch S3 is turned on by applying control signal $V_{\rm ctr}$ to the gate of transistor switch S3 according to the timing diagram as shown in Fig. 4. Current flows into the load capacitor C_L and an electromotive force (EMF) is generated in a series inductor, $L_{\rm ER}$. When the output voltage $V_{\rm out}$ reaches the same potential $(V_{dd}/2)$ as the storage capacitor $C_{\rm ER}$, the EMF of $L_{\rm ER}$ begins to collapse and the current is forced to flow in the same direction through the inductor $L_{\rm ER}$, forcing the $V_{\rm out}$ to approach V_{dd}.

The output voltage $V_{\rm out}$ reaches V_{dd} at the point when the current I_L in the series inductor becomes zero. At this time, the switch S3 is turned off, and the switch S1 is turned on. This holds the output voltage at V_{dd} for finite time, giving the flat-top of the output pulse. A small amount of energy will be drawn from V_{dd} through switch S1 to bring the output to the full logic '1', and replenish any energy dissipated in the resonant circuit. In the discharge phase, the charge is returned to the energy-recovery biasing capacitor $C_{\rm ER}$ by current flowing out of C_L through $L_{\rm ER}$ by turning on the switch S3, and by turning off the other switches S1 and S2. $L_{\rm ER}$, $C_{\rm ER}$, and C_L again form a series resonant circuit for energy transfer from C_L to the inductor $L_{\rm ER}$ by current flowing out of C_L through $L_{\rm ER}$. This causes a build-up of EMF in $L_{\rm ER}$ in the direction opposite to the charging phase, returning charge to the capacitor $C_{\rm ER}$. When $V_{\rm out}$ decreases to $V_{dd}/2$, the EMF of $L_{\rm ER}$ collapses and forces the current in same direction through the $L_{\rm ER}$, forcing $V_{\rm out}$ to reach ground at logic '0'. At this point, the current I_L becomes zero and the switch S3 is turned off, and the switch S2 is turned on to hold the output voltage to ground (i.e., logic '0'). Through this resonant energy transfer mechanism, most of the energy is recovered, and the charge is restored to the biasing capacitor $C_{\rm ER}$, and stable $V_{dd}/2$ stored voltage in $C_{\rm ER}$ is maintained during the circuit operation since the designed value of $C_{\rm ER}$ is 8× larger than C_L. In this way, the resonant driver with externally controlled switches generates a sequence of output voltage pulse with finite flat-tops.

D. Derivation of Energy Dissipation and Recovery Efficiency

The proposed method for conserving the stored energy during digital switching of states is based on an energy recovery mechanism using a series resonant circuit with controlled switching. The switching action of transistor switch S3 controls the flow of current through the circuit, thus gradually storing energy in the inductor. Here, the inductor behaves as an "electrical flywheel" assisting the transfer of energy between $C_{\rm ER}$ and C_L. For a practical circuit model, the resistance $R_{\rm on}$ associated with the transistor switch and the series inductor is included along with inductance $L_{\rm ER}$, and capacitances $C_{\rm ER}$ and C_L in the circuit. The resistance in the circuit introduces the damping in the oscillating waveforms, and results in some energy dissipation. To calculate energy dissipation, the output voltage $(V_{\rm out}(t))$ and the transient current $(i_L(t))$ flowing through the circuit can be computed based on the series RLC analysis of the circuit shown in Fig. 3(b). From Kirchhoff's Voltage Law (KVL), we find the relation for voltage as

$$\frac{1}{C_{\rm ER}}\int i_L(t)dt + R_{\rm on}i_L(t) + L_{\rm ER}\left(\frac{di_L(t)}{dt}\right) + \frac{1}{C_L}\int i_L(t)dt = \frac{V_{dd}}{2} \quad (2)$$

which leads to a second-order differential equation for current $i_L(t)$, and can be expressed as

$$\frac{d^2i_L(t)}{dt^2} + \left(\frac{R_{\rm on}}{L_{\rm ER}}\right)\frac{di_L(t)}{dt} + \left(\frac{C_L + C_{\rm ER}}{C_L C_{\rm ER}}\right)\frac{i_L(t)}{L_{\rm ER}} = 0. \quad (3)$$

By using initial conditions for current and output voltage of $i_L(0) = 0$ and $V_{\rm out}(0) = V_{dd}/2$ at $t = 0$, the solution for the transient current $i_L(t)$ in (3) can be written as [33]

$$i_L(t) = \frac{V_{dd}}{2}C_L\left(\frac{\omega_0^2}{\omega_d}\right)e^{-\alpha t}\sin(\omega_d t) \quad (4)$$

where $\alpha = R_{\rm on}/2L_{\rm ER}$ is the attenuation frequency, $\omega_d = \sqrt{\omega_0^2 - \alpha^2}$ is the angular frequency of oscillation, and $\omega_0 = 1/\sqrt{L_{\rm ER}C_{\rm tot}}$ is a resonant frequency from the total capacitance, $C_{\rm tot} = C_L C_{\rm ER}/(C_L + C_{\rm ER})$. Finally, the output voltage $V_{\rm out}(t) = (1/C_L)\int i_L(t)dt$ is calculated by [33]

$$V_{\rm out}(t) = \frac{V_{dd}}{2}e^{-\alpha t}\cdot\left[\cos(\omega_d t) + \frac{\alpha}{\omega_d}\cdot\sin(\omega_d t)\right]. \quad (5)$$

Without the switches S1 and S2, the output voltage oscillates with a frequency ω_d for the under damped condition $(\alpha < \omega_0)$ met by an appropriate choice of the lumped parameters of $L_{\rm ER}$, C_L, and $C_{\rm ER}$ in the computing circuit. The output waveform of the series resonant circuit combines with S1 and S2 to generate a flat-topped (quasi-trapezoidal) energy-efficient final output pulse at each rising and falling edge. The resistive losses associated with the circuit are accounted for in the energy dissipation using $i_L^2 R_{\rm on}$ loss in the FET switches. Using (4), the energy dissipation per complete cycle of oscillation can be expressed as $2\int_0^{\pi/\omega_d}[i_L^2(t)R_{\rm on}]dt$ [33] which evaluates to

$$E_{\rm diss} = \frac{1}{4}C_L V_{dd}^2\cdot\left(1 + \frac{C_L}{C_{\rm ER}}\right)\cdot\left(1 - e^{-(2\pi\alpha/\omega_d)}\right). \quad (6)$$

A figure of merit for a computing circuit can be defined as the energy recovery efficiency $\eta_{\rm rec} = [E_{\rm stored} - E_{\rm diss}]/E_{\rm stored} \times 100\,\%$. For conventional CMOS with no energy recovery mechanism, the stored energy in the load capacitor C_L during charging phase is completely lost as heat in the switching transistor during discharging phase, resulting in $E_{\rm stored} = E_{\rm diss}$ and recovery efficiency of $\eta_{\rm rec} = 0\%$. Using resonant switching, a lossless high-Q circuit asymptotically recovers all the energy leading to $E_{\rm diss} = 0$ and $\eta_{\rm rec} = 100\%$. Practically, there are resistive losses (i.e., $i_L^2 R_{\rm on}$) and switching losses in the switches, leading to dissipation in the circuit. Using (6), the energy recovery efficiency $\eta_{\rm rec}$, taking into account the resistive losses and switching losses, can be calculated by

$$\eta_{\rm rec} = \left[1 - C_g V_g^2 - \frac{1}{4}\cdot\left(1 + \frac{C_L}{C_{\rm ER}}\right)\cdot\left(1 - e^{-\frac{2\pi\alpha}{\omega_d}}\right)\right]\times 100\%. \quad (7)$$

The second term in (7) is due to the switching energy loss in driving the gates of the controlled switches (here, S3, S1 & S2). This term $C_g V_g^2$ contributes a negligible amount, ∼69 aJ for $C_g = 6.9 \times 10^{-17}$ F at $V_g = 1$ V using the 22-nm node [35], with the FET switch at an aspect ratio $W/L_g = 5/1$ at $L_g = 20$ nm, $W = 5 \times 20$ nm, and $T_{\rm ox} = 1$ nm. By substituting

the values of α and ω_d in (7), the energy recovery efficiency $\eta_{\rm rec}$ can be written as

$$\eta_{\rm rec} = \left[1 - C_g V_g^2 - \frac{1}{4}\cdot\left(1+\frac{C_L}{C_{\rm ER}}\right) \times \left(1 - e^{-\frac{2\pi R_{\rm on}\sqrt{C_{\rm tot}}}{\sqrt{4L_{\rm ER} - R_{\rm on}^2 C_{\rm tot}}}}\right)\right] \times 100\%. \quad (8)$$

The energy recovery efficiency depends on the lumped components in a computing circuit. To achieve high recovery efficiency, the resistive losses should be minimized by incorporating switches with very low ON resistance and a high-Q lossless inductor. The ideality of an inductor is measured by a quality factor Q, which represents the ratio of energy stored in the form of magnetic field to the energy dissipated in an inductor per cycle [37]. In a series RLC resonant circuit, the quality factor Q can be written as $Q = \omega_0 L_{\rm ER}/R_{\rm on}$. The oscillation frequency ω_d in a circuit is given by $\omega_d = \omega_0\sqrt{1-1/4Q^2}$. By substituting ω_d in terms of Q in (7), the energy recovery efficiency can also be expressed as

$$\eta_{\rm rec} = \left[1 - C_g V_g^2 - \frac{1}{4}\cdot\left(1+\frac{C_L}{C_{\rm ER}}\right) \times \left(1 - e^{-\frac{\pi}{Q\sqrt{1-1/4Q^2}}}\right)\right] \times 100\%. \quad (9)$$

The energy recovery efficiency is considered to be higher for a higher value of Q of the resonant circuit. The value of Q is limited by energy loss due to parasitics in the inductor. In order to obtain a high Q value of inductor, the values of parasitics (resistance and capacitance) in the inductor have to be lowered.

E. Design of Energy Recovery System

The energy recovery circuit is designed for a technology with fixed resistance associated with a transistor switch and load capacitance. The inductance $L_{\rm ER}$ can be adjusted to form a series resonant circuit at a required frequency of operation with minimum energy loss. In the circuit of Fig. 3, the only component that dissipates energy is the transistor switch. The calculated energy dissipation in (6) included the non-zero ON resistance of the MOS switch. The resistance of an N-channel MOSFET, $R_{\rm on} = V_{ds}/I_d$, operating in the linear region (i.e., $V_{ds} \ll V_{gs} - V_t$ for quasi-static switching) is given by [33], [34]

$$R_{\rm on} = \frac{L_g^2}{\mu_n c_0 (V_{gs} - V_t)} \quad (10)$$

where L_g is the channel length of the MOS transistor, μ_n is the effective carrier mobility in the channel, $c_0 = W L_g c_{\rm ox}$ is the gate capacitance, W is the channel width of the transistor, and $c_{\rm ox}$ is the oxide capacitance. For a typical 22-nm node [35], the gate overdrive voltage $(V_{gs} - V_t) \sim 1$ V, $\mu_n = 500$ cm^2/V.s, $L_g = 20$ nm, $W = 5 \times 20$ nm, and $c_0 = (5 * 20 \times 10^{-9} * 20 \times 10^{-9} * 3.9 * 8.85 \times 10^{-12})/(1.0 \times 10^{-9}) = 6.9 \times 10^{-17}$ F with $T_{\rm ox} = 1.0$ nm gate oxide thickness, and the ON resistance calculated by (10) gives $R_{\rm on} = 115.9\ \Omega$. From the analysis of output voltage and current waveforms of the resonant circuit in (5) and (4) for under-damped or critically damped condition, ω_d increases as $L_{\rm ER}$ decreases, up to a maximum, $\omega_{d\,\max} = 1/R_{\rm on}C_{\rm tot}$, and then decreases, thus requiring the value of minimum inductance, $L_{\rm ER,min} = R_{\rm on}^2 C_{\rm tot}/2$. To design the energy recovery resonant clocking circuit, the chosen value of inductor $L_{\rm ER}$ should be larger than $R_{\rm on}^2 C_{\rm tot}/2$ ($L_{\rm ER} \geq R_{\rm on}^2 C_{\rm tot}/2$) in order to obtain underdamped oscillation and a good energy recovery efficiency. From the circuit analysis, the energy dissipation due to charging and discharging of C_L through two transistor switches in a conventional logic is equal to $C_L V_{dd}^2$. By incorporating a resonant energy conserving mechanism, the restored energy in the energy-recovery capacitor $C_{\rm ER}$ with $V_{dd}/2$ precharged voltage is equal to $(1/8)C_{\rm ER}V_{dd}^2$. From these two relations, the value of $C_{\rm ER}$ should at least be 8× larger than C_L ($C_{\rm ER} \geq 8C_L$) in order to maintain stable $V_{dd}/2$ stored voltage in the $C_{\rm ER}$ during switching operation. The $C_{\rm ER}$ with this predicted designed value in a clocking circuit is crucial for electrical energy storage and initialization of the circuit operation.

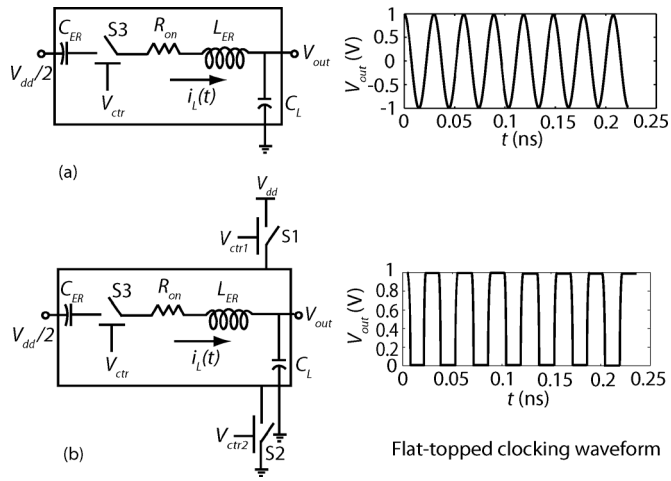

Fig. 5. (a) The calculated sinusoidal waveform generated by a standard LC resonator with an externally controlled FET switch, S3, using the schematic of Fig. 3(b). (b) Derived flat-topped (quasi-trapezoidal) output clocking waveform from sinusoidal waveform by modifying the circuit with two externally controlled FET switches, S1 & S2, using the schematic of Fig. 3(a). The underdamped sinusoidal oscillated waveform is generated by a resonant circuit with $V_{dd} = 2$ V, $R_{\rm on} = 5\ \Omega$, $L_{\rm ER} = 25$ nH, $C_L = 1$ fF, and $C_{\rm ER} = 8$ fF.

III. Results and Discussions

The proposed method based on energy recovery resonant switching in a circuit results in a sequence of energy-efficient flat-topped clocking pulses. Fig. 5 illustrates the derived flat-topped (quasi-trapezoidal) clocking waveforms from the sinusoidal waveforms. Fig. 5(a) shows the underdamped sinusoidal oscillated waveforms generated by the standard LC resonant circuit using the schematic of Fig. 3(b), and plotted with time. Here, the sinusoidal waveform is calculated by (5) at underdamped condition using the designed values, $V_{dd} = 2$ V, $R_{\rm on} = 5\ \Omega$, $L_{\rm ER} = 25$ nH, $C_L = 1$ fF, and $C_{\rm ER} = 8$ fF in

the resonant circuit. Fig. 5(b) illustrates the derived clocking waveforms from sinusoidal waveforms by modifying the resonant circuit with addition of two externally controlled switches, S1 & S2, over the underdamped sinusoidal waveforms using the schematic of Fig. 3(a). The switch S1 is used to clamp the output node to the logic level '1' (providing flat-tops at logic '1'), and to replenish any energy dissipated in the resistance of the circuit during switching. The switch S2 is also used to clamp the output node to the logic level '0' (ground ~ 0 V, flat-tops at logic '0'). In designing the clocking circuit, the amplitude of the clocking waveform can be adjusted by the operating voltage V_{dd}, and the time period can also be optimized by choosing the proper values of inductance and capacitance in the resonant circuit.

Figs. 6 and 7 plot the energy dissipation as a function of inductance, $L_{\rm ER}$, for different values of series resistances $R_{\rm on}$, at load capacitances $C_L = 1\times10^{-15}$ F and 1×10^{-12} F, and energy recovery capacitances $C_{\rm ER} = 8C_L$, with conventional abrupt switching and energy recovery resonant switching, respectively. The dissipation is smaller for resonant switching over the conventional abrupt switching. At resonance, the inductive reactance is used to cancel the capacitive reactance, and energy is only dissipated in an equivalent series resistance in the circuit. Thus, the energy recovery resonant switching reduces the energy dissipation and improves the phase stability (reducing skew and jitter in clock period) of the output clocking waveform. At load capacitance $C_L = 1$ pF, the dissipation is higher than that for the lower load capacitance $C_L = 1$ fF (see Figs. 6 and 7). Therefore, to achieve lower energy dissipation, a higher value of inductance is required for resonance at the higher clock load capacitance in the circuit. Note that the reduction of energy dissipation in this energy recovery resonant switching method approaches the fundamental limit for irreversible switching, at $R_{\rm on} = 0.45\ \Omega$ in Fig. 6 ($\sim 10^{-20}$ J, which is one order of magnitude greater than the $k_BT\ln(2) \sim 10^{-21}$ J at $T = 300$ K per bit operation [2], [5]). It is also worthwhile to point out that there is no lower limit on energy dissipation to heat if information is not destroyed during logic computation [12]. This preservation of information can be achieved by reversible computation with the adiabatic logic [10], [25].

Using (8), and assuming the values of $C_L = 1\times10^{-15}$ F, 1×10^{-12} F, $C_{\rm ER} = 8C_L$, and $R_{\rm on} = 0.45\ \Omega$, 20 Ω, 50 Ω, 100 Ω, the energy recovery efficiency $\eta_{\rm rec}$ is calculated and plotted as a function of the inductance $L_{\rm ER}$. The results are shown in Figs. 8 and 9. Note that the energy recovery efficiency is higher (close to 100%) for lower value of series resistance $R_{\rm on} = 0.45\ \Omega$, while the efficiency is reduced with increasing $R_{\rm on}$ (because of large resistive losses). The clocking circuit recovers more than 90% of the energy at $C_L = 1$ fF for different values of $R_{\rm on} = 0.45\ \Omega$, 20 Ω, 50 Ω and 100 Ω (see Fig. 8). It is shown that the recovery efficiency is reduced (75%) at higher load capacitance $C_L = 1$ pF, as compared to lower $C_L = 1$ fF with the designed value of inductance $L_{\rm ER} = 1$–10 nH (see Fig. 9). To obtain a high energy recovery efficiency ($> 80\%$), higher value of inductance is needed to resonate the large load capacitance C_L in the resonant circuit. The operating conditions for a clocking circuit with recovery efficiency ($> 80\%$) can be optimized at $L_{\rm ER} = 1$–10 nH with fixed load capacitance C_L

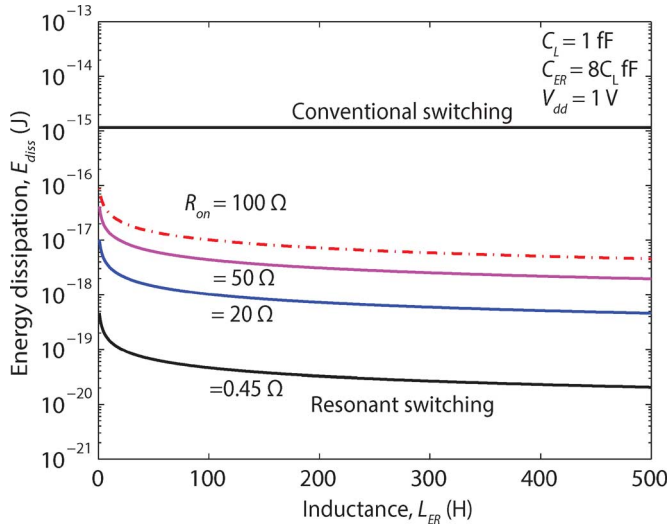

Fig. 6. Calculated energy dissipation as a function of inductance for various values of series ON resistances $R_{\rm on}$, load and energy-recovery capacitances, $C_L = 1\times10^{-15}$ F and $C_{\rm ER} = 8C_L$, assumed in the clocking circuit. Energy dissipation is lower for resonant switching with energy recovery mechanism over the conventional abrupt switching. For resonant switching, energy dissipation is even smaller for smaller values of $R_{\rm on}$.

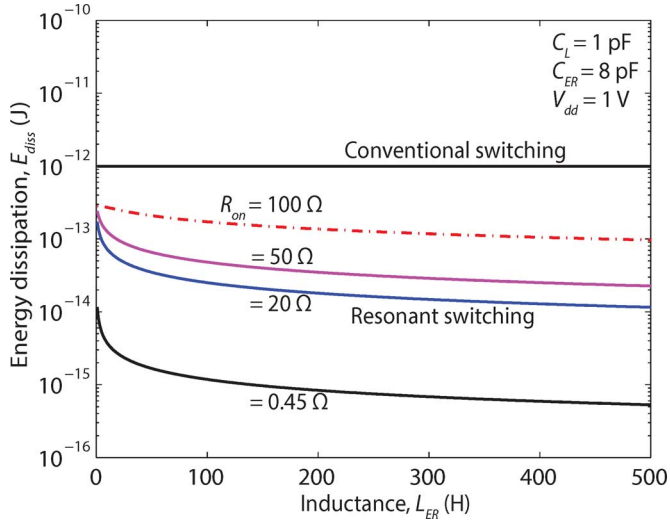

Fig. 7. Calculated energy dissipation as a function of inductance for various values of series ON resistances $R_{\rm on}$, load and energy-recovery capacitances, $C_L = 1\times10^{-12}$ F and $C_{\rm ER} = 8C_L$, assumed in the circuit. Energy dissipation is higher for higher load capacitance C_L in both switching.

to generate an energy-efficient GHz clock pulse for a specific technology.

Fig. 10 shows the plot of energy recovery efficiency as a function of inductance for different values of $C_{\rm ER}$ at $R_{\rm on} = 10\ \Omega$ and $C_L = 1$ pF. The recovery efficiency remains constant for the values of energy recovery capacitor $C_{\rm ER} = 8$, 20, 30, and 50 pF (our predicted designed value $C_{\rm ER} \geq 8C_L$), with little reduction even at a value of $C_{\rm ER} = 4$ pF. For $C_{\rm ER} = 0.1$ pF (i.e., $C_{\rm ER} < C_L$), the recovery efficiency is reduced as compared to the higher values of $C_{\rm ER}$. From the analysis and calculated results in Fig. 10, the designed value of energy recovery capacitor $C_{\rm ER}$ can be optimized to $C_{\rm ER} \geq 8C_L$ in order to maintain the

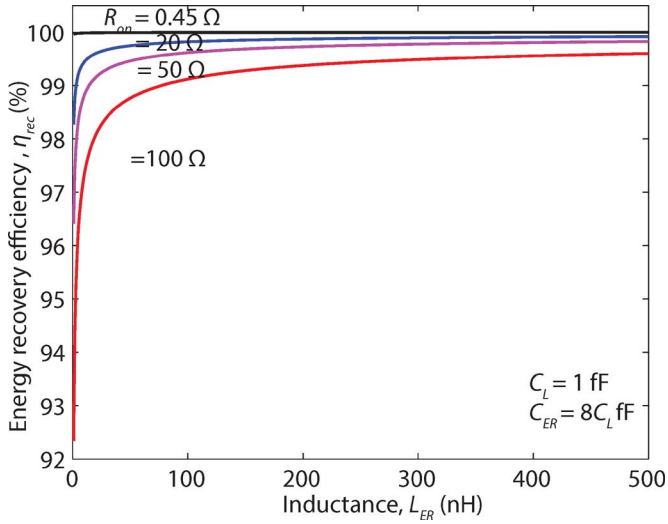

Fig. 8. Calculated energy recovery efficiency as a function of inductance for different values of series ON resistances $R_{\rm on}$, load and energy-recovery capacitances, $C_L = 1 \times 10^{-15}$ F and $C_{\rm ER} = 8C_L$, in the clocking circuit. Recovery efficiency is higher for smaller values of $R_{\rm on}$. The circuit recovers more than 90% of the energy.

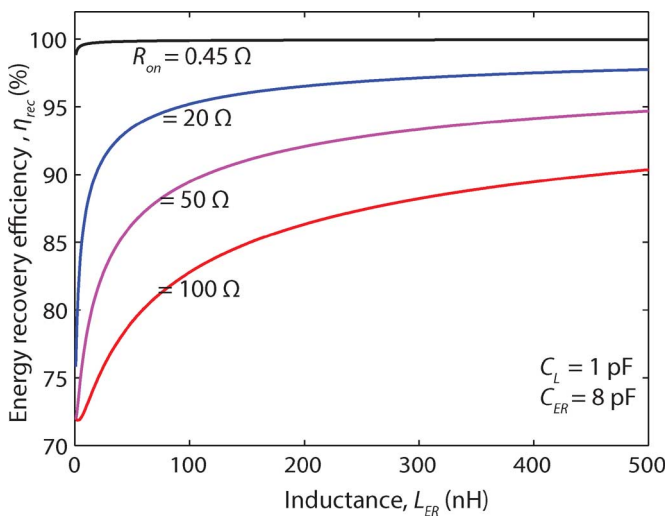

Fig. 9. Energy recovery efficiency as a function of inductance for different values of series ON resistances $R_{\rm on}$, load and energy-recovery capacitances, $C_L = 1 \times 10^{-12}$ F and $C_{\rm ER} = 8C_L$, in the clocking circuit. The circuit recovers less energy (71% of the energy) at $C_L = 1$ pF as compared to the lower value of load capacitance $C_L = 1$ fF with lower value of inductance.

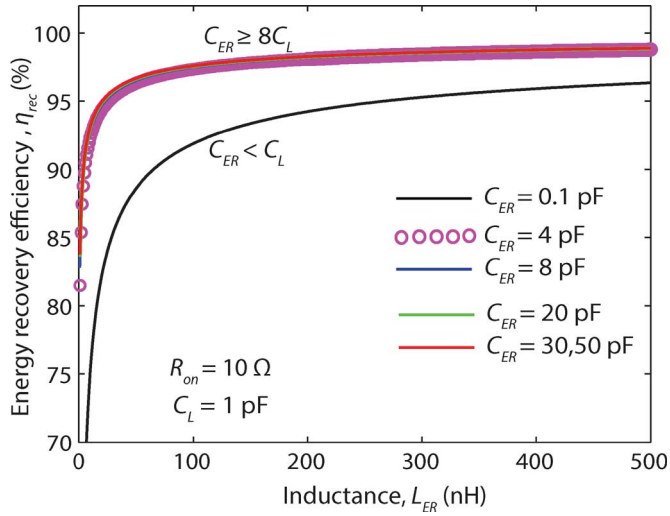

Fig. 10. Energy recovery efficiency as a function of inductance for different values of energy-recovery capacitances $C_{\rm ER} = 0.1$, 4, 8, 20, 30, and 50 pF at $R_{\rm on} = 10\ \Omega$ and $C_L = 1$ pF in the clocking circuit. Recovery efficiency remains constant for $C_{\rm ER} = 8$, 20, 30, and 50 pF (i.e., $C_{\rm ER} \geq 8C_L$)), and is lower for $C_{\rm ER} = 0.1$ pF (i.e., $C_{\rm ER} < C_L$).

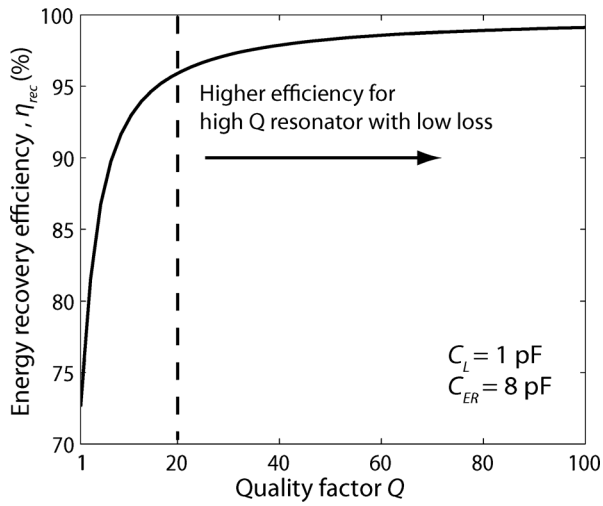

Fig. 11. Energy recovery efficiency as a function of quality factor Q varied from 1 to 100 at $C_L = 1$ pF and $C_{\rm ER} = 8$ pF in the circuit. Recovery efficiency is larger at higher values of Q in the resonant clocking circuit.

high recovery efficiency and stable $V_{dd}/2$ voltage during circuit operation.

Fig. 11 depicts the plot of energy recover efficiency as a function of the quality factor Q varied from 1 to 100 at $C_L = 1$ pF and $C_{\rm ER} = 8$ pF in the clocking circuit. Here, Q accounts for the losses due to parasitics in the inductor in the resonant circuit. The energy recovery efficiency is larger ($> 95\%$) at higher values of Q (> 20) due to low losses in the resonant circuit.

The inductor in a resonant circuit can physically be realized by the distributed spiral thick metal layers on-chip [16], [36]–[39]. Using the value of on-chip spiral inductor of $L_{\rm ER} \sim 7.4$ nH (with $Q \sim 6.76$, total parasitic resistance $R_p \sim 15$ kΩ, and capacitance $C_p \sim 1.3$ pF) at 1-GHz frequency [36], 71% of the energy can be recovered based on our energy recovery circuit and its analysis. A high-Q (low parasitic loss) inductor is required for operating the energy recovery circuit with high recovery efficiency. An off-chip discrete inductor with high Q can also be used to generate resonant clocking pulse. Due to limitations of high quality factor for on-chip inductors, a MEMS/NEMS (very high-Q) resonator can be used for generating an energy-efficient clocking waveform.

IV. Conclusion

An efficient energy-recovery mechanism (reduced heat generation) based on a resonant circuit with controlled switching during logic transitions has been presented. This method has been used to conserve the stored energy during switching of logic states, thus aiding computation in a thermodynamically reversible fashion with asymptotically zero energy loss. The proposed resonant circuit with the FET switches generates an en-

ergy-efficient flat-topped output waveform, which is needed to enable low energy, reversible computation. We have also derived the energy recovery efficiency and shown that more than 90% of the energy can be recovered by this externally controlled resonant switching in the circuit. To obtain low dissipation and high energy recovery efficiency, the high-precision FET switches with the lower operating voltage V_{dd} and lower ON channel resistance in the circuit are required to perform the logic operations. To initialize the resonant switching operation, an energy-recovery capacitor $C_{\rm ER}$ with the proposed designed value ($C_{\rm ER} \geq 8C_L$) and $V_{dd}/2$ stored voltage has been incorporated in the circuit. An LC resonator with a high-Q inductor has been used to generate the energy-efficient waveform. This energy-efficient waveform with a sequence of the periodic pulses generated by this proposed energy recovery resonant switching has played important applications in clocking for low-power digital logic computations. In addition to clocking application, this energy-efficient switching approach can also be applied to high-voltage drive circuitry used in consumer electronics, such as field emission displays, liquid crystal displays (LCD) backlighting driving, and the interfacing of a circuit to the external world. In these system applications, the display devices (such as an LCD, plasma displays, etc.) have been used as a load capacitor; energy is moved to and from these devices through storage/recovery switching mechanisms instead of dissipating as heat during display operation. The methodology we have proposed here is generally applicable to any low-power computing systems.

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