Electron transport in 2D crystal semiconductors and their device applications

Debdeep Jena[1], Mingda Li[1], Nan Ma[1], Wan Sik Hwang[2], David Esseni[3], Alan Seabaugh[1], and Huili Grace Xing[1]
[1]Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN USA
[2]Department of Materials Engineering, Korean Aerospace University, Gyeonggi-do, Korea
[3]Department of Electrical Engineering, University of Udine, Udine, Italy
Email: djena@nd.edu

***Abstract* —In this work, we investigate the transport properties of 2D crystal semiconductors from two angles. For drift transport in traditional FETs, scattering mechanisms that limit the electron mobility are identified, and means to improve them vastly over currently reported values are presented. For low-power electronics, tunneling transport currents within monolayer p-n junctions, and interlayer tunneling currents between adjacent 2D semiconductor layers is discussed for TFETs.**

I. Introduction

The physics of electron transport in 2D crystal semiconductors such as graphene and transition metal dichalcogenides (MoS_2, …) will be the basis for their integration into electronic devices, and yet is poorly understood. Here, the mobility is studied to gauge the potential of 2D semiconductors for extending scaling, owing to their excellent electrostatics and atomically thin nature with well-defined band-edge profiles. These attractive scaling properties also can potentially allow interband tunnelling FETs [1, 2] as a potential strategy for beyond-CMOS devices.

II. Scattering and mobility limits

The reported electron and hole mobilities in thin TMD crystals [3] are in the range of 100 cm^2/Vs, which compares unfavourably with graphene, Si and other III-V semiconductors [Fig 1]. However, by careful modelling of the scattering mechanisms, we uncover that charged impurity scattering is responsible for these low numbers [4]. Significant improvement can be achieved by the reduction of impurities but that alone would not be enough. Being atomically thin semiconductors, charge carriers couple effectively to optical phonon scattering modes in the surrounding dielectrics because of the spatial proximity. For high electron mobilities, the dielectrics must be made of light atoms that forbid low-energy phonon modes.

III. Tunneling Transport

For low-power electronics, current flow by interband tunnelling transport can potentially enable steep switching below the 60 mV/decade thermal limit. Figure 3 shows the in-plane interband tunnelling currents in p-n junctions formed in various atomically thin 2D semiconductors [5]. High currents can be achieved in electrostatically well-designed devices that deliver the requisite large electric fields at the junction by exploiting the very small electrostatic screening lengths stemming from the atomically thin semiconductor body thickness. The ultrathin body also allows for scaling to thicknesses that are difficult in traditional semiconductors because the energy bandgaps increase due to quantum confinement, reducing tunnelling current. The variation in the thickness in a top-down approach also compromises the integrity of the band-edge profiles in traditional semiconductors. To illustrate the feasibility of in-plane tunnelling FETs, we show in Fig 4 an example of a lithographically defined graphene nanoribbon (GNR) device that exhibits NDR at room temperature [6], and Fig 5 shows calculated currents and steep slopes for an interlayer tunnelling FET, in which current flows from one 2D crystal semiconductor into another, showing attractive low-power device potential [7]. This work is supported in part by the NSF, AFOSR, and STARnet, a Semiconductor Research Corporation program supported by MARCO and DARPA.

References

[1] A. Seabaugh, Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic", *Proc. of the IEEE*, v.98, p.2095, 2010.
[2] D. Jena, "Tunneling Transistors Based on Graphene and 2D Crystals", *Proc. of the IEEE*, v.101, p.1585, 2013.
[3] S, Kim et al., "High-mobility, low-power thin-film transistors based on multilayer MoS_2 crystals," *Nature Communications*, v.3, p.1011, 2012.
[4] N. Ma, D. Jena, "Charge Scattering and Mobility in Atomically Thin Semiconductors", *Phys. Rev. X*, v.4, p.011043, 2014.
[5] N. Ma, D. Jena, "Interband tunneling in 2D crystal semiconductors," *Appl. Phys. Lett.*, v.102, p.132102, 2013.
[6] W. S. Hwang et al., in preparation.
[7] M. Li et al., "Single particle transport in 2D heterojunction interlayer TFET (THIN-TFET)", *J. Appl. Phys.* v.115, p.074508, 2014.

978-1-4799-5677-7/14/$31.00 ©2014 IEEE

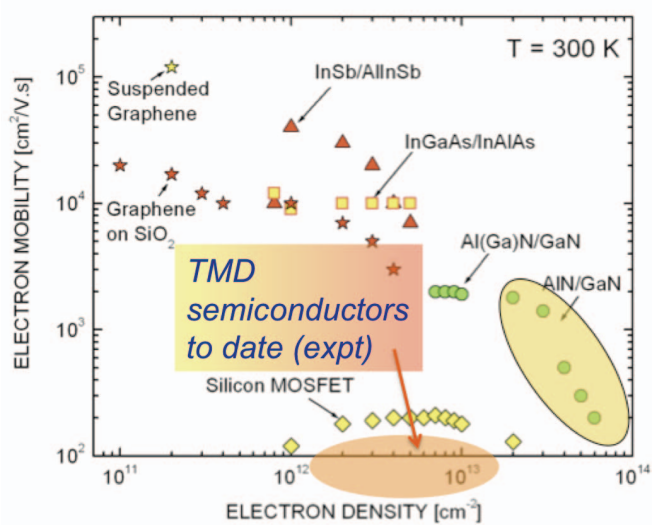

Fig 1: Carrier mobilities in TMD semiconductors in comparison to traditional semiconductors and graphene. Carrier mobilities in zero-gap graphene are reasonably high, but experiments till date are in the 100 cm^2/Vs range for the gapped TMD semiconductors [3,4].

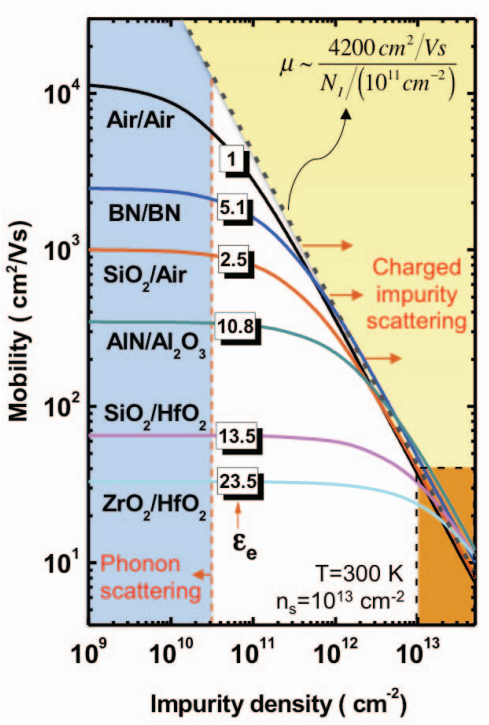

Fig 2: Carrier mobilities in monolayer MoS_2 as a case study, showing the very strong effect of charged impurity scattering. In sufficiently pure layers, remote-phonon scattering must be tamed to obtained high mobilities at room temperature. The choice of correct dielectrics is crucial [4].

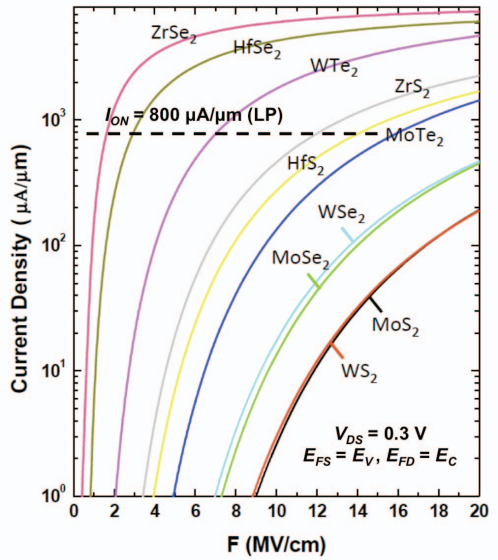

Fig 3: In-plane interband tunneling currents in monolayer TMD crystal p-n junctions. The currents at high fields are appreciably high for TFETs [2, 5].

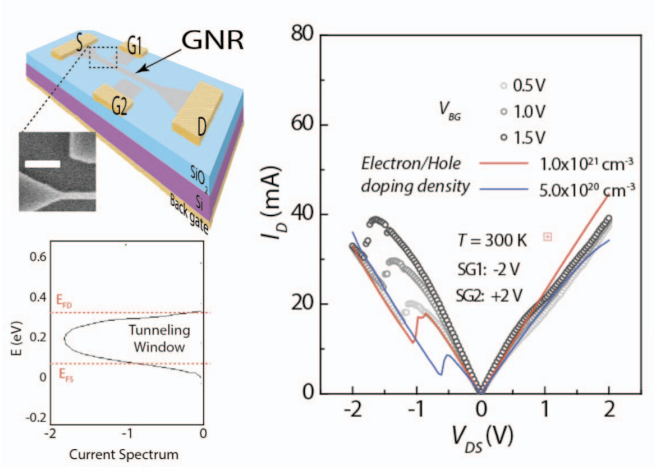

Fig 4: Experimental GNRTFET with NDR at 300K[6].

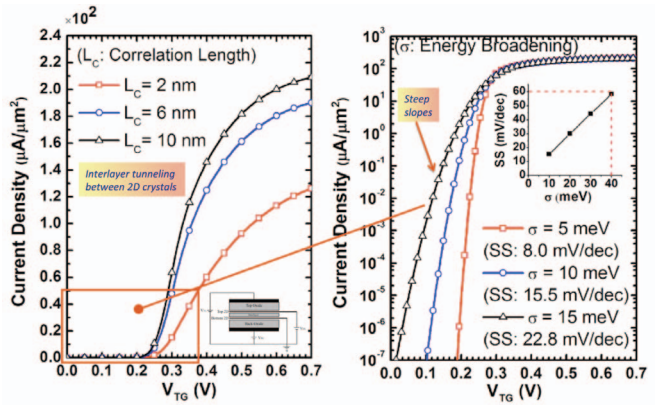

Fig 5: Calculated steep-slopes in thin-TFETs using interlayer tunneling between TMD semiconductor layers [7].