AlGaN/GaN MIS-HEMT on Silicon with Steep Sub-threshold Swing < 60 mV/dec over 6 orders of drain current swing and relation to traps

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***Abstract* — AlGaN/GaN MIS-HEMT on silicon with steep sub-threshold swing (SS) < 60mV/dec over 6 orders of drain current swing over a wide range of drain biases from 0.1 to 10V at room temperature are demonstrated. A low SS of 33 mV/dec has been observed at a drain bias of 10V when V_{gs} is sweept 'up', from low to high values. The origin for such steep SS has been ascribed to the dynamic de-trapping and charge injection into the 2DEG channel from interface states at the dielectric/GaN cap interface, as validated by V_{gs} stress measurements.**

I. Introduction

Steep subthreshold swing (SS) transistors have received wide attention and significant demand in low power consumption applications, such as portable consumer electronics. Traditional CMOS scaling is limited by the unscalbility of the power supply voltage due to SS>60mV/decade at room temperature (RT). Novel device concepts such as tunneling [1] and alternative gate barrier materials (i.e. ferroelectric materials) [2] have been proposed to break the SS limit. GaN based high electron mobility transistors (HEMTs) ideally are suitable for high speed and high power applications due to its high saturation velocity and high breakdown field [3]. However, less than 60 mV/dec SS was recently experimentally observed at GaN MIS-HEMT with InAlN barriers [4-6]. The low SS was only observed within a small drain current range (i.e. < 3 orders). In this work, we report that the steep SS<60 mV/dec persists over 6 orders of drain current in AlGaN/GaN MIS-HEMT on silicon at room temperature. The observation points to the possibility for future logic switches on silicon platform, with the proper engineering and control of such dynamic de-trapping and charging process.

II. Experiments

The AlGaN/AlN/GaN HEMT device layer structure consists of a 1 nm GaN cap, 20 nm $Al_{0.26}Ga_{0.74}N$ barrier, 1 nm AlN spacer and a GaN channel on 1.3 μm semi-insulating GaN buffer grown by metal organic chemical vapor deposition (MOCVD) on silicon substrate. The device processing started from a Ti-based alloyed ohmic contact, followed by mesa isolation. The 2DEG concentration and electron mobility was $6.23\text{x}10^{12}$ cm^{-2} and 1760 cm^2/Vs, respectively, by Hall measurement after mesa isolation. A $SiN_x/Al_2O_3/SiN_x$ (5/5/2nm) gate dielectric stack was deposited by plasma-assisted atomic layer deposition (ALD), after which a 3μm Ni/Au gate metallization was placed.

III. Results and Discussion

The representative common source and transfer characteristics of AlGaN MISHEMTs are shown in Fig.1. The device can achieve a $I_{d,max}$ ~ 360 mA/mm at V_{gs} = 2 V and V_{ds} = 10 V. Dual-direction V_{gs} sweeps at V_{ds} = 6 V shows SS of 55 mV/dec during the V_{gs} up-sweeps from negative to +2 V at a sweep rate of 38 mV/s. In the reverse (down)-sweep, a SS of 73 mV/dec is obtained and results in a small hysteresis of ~10 mV. I_d-V_{gs} characteristics with gate turn-on (up-sweep) and turn-off (down-sweep) at variable drain bias V_{ds} from 0.1 to 10 V a sweep rate of 16 mV/s are shown in Fig.2 (a) and (c), from which the SS dependence on the drain current is calculated in Fig. 2(b) and (d), respectively. During the turn-on process, SS< 60 mV/dec over almost 6 order of drain current swing has been observed and the minimum local SS decreases with increasing drain voltage, e.g. a minimum local SS reduces from 50 to 33 mV/decade when V_{ds} increases from 0.1 to 10 V. During the gate turn-off process, the minimum SS values are >65 mV/decade regardless of the drain bias. Besides, hysteresis in the threshold voltage V_T is observed where a more negative value is obtained during the down-sweep than that in the up-sweep. A dynamic trapping and de-trapping of acceptor-like states [4] at the dielectric/GaN cap interface shown in Fig.3 can explain such observations, where the de-trapped electrons aid the turn-on/off process, leading to a low/high SS during the sweeping up/down process. To further validate the model, an initial stress to de-trap the acceptor-like states is applied with different initial V_{gs} and holding time. A more negative initial $V_{gs,initial}$ and a longer holding time at $V_{gs,initial}$ result in a more negative V_{th} and a higher SS (Fig.3(c)) since more

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electrons have been de-trapped from trap states in the gate stack between the metal gate and the GaN channel before starting to sweep V_{gs} (i.e. the turn-on process), thus less apparent charge gain in the channel.

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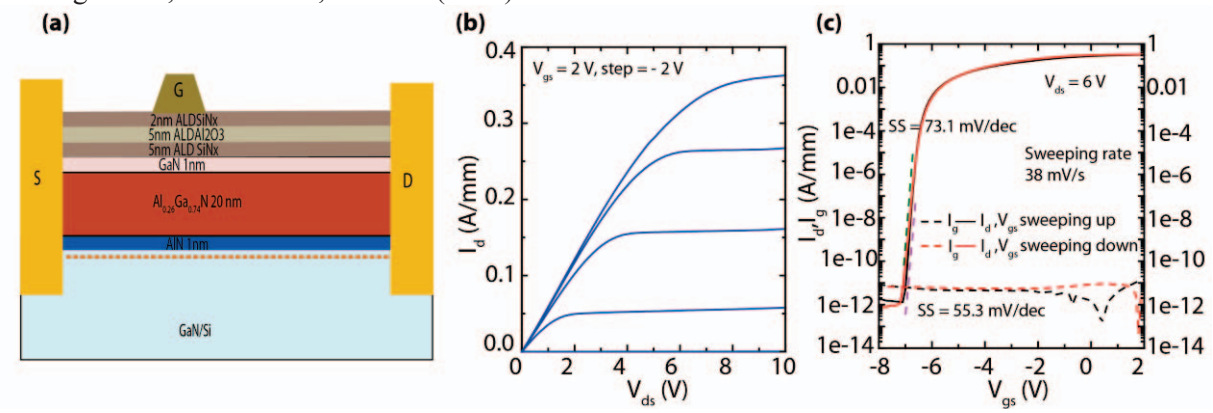

Fig.1 (a) Schematic of AlGaN/GaN MIS-HEMT on Si substrate with $SiN_x/Al_2O_3/SiN_x$(5/5/2 nm) gate dielectrics , (b) common source and (c) dual direction sweeping transfer characteristics of AlGaN/GaN MIS-HEMT showing a SS ~55/73 mV/dec at sweeping up/down conditions

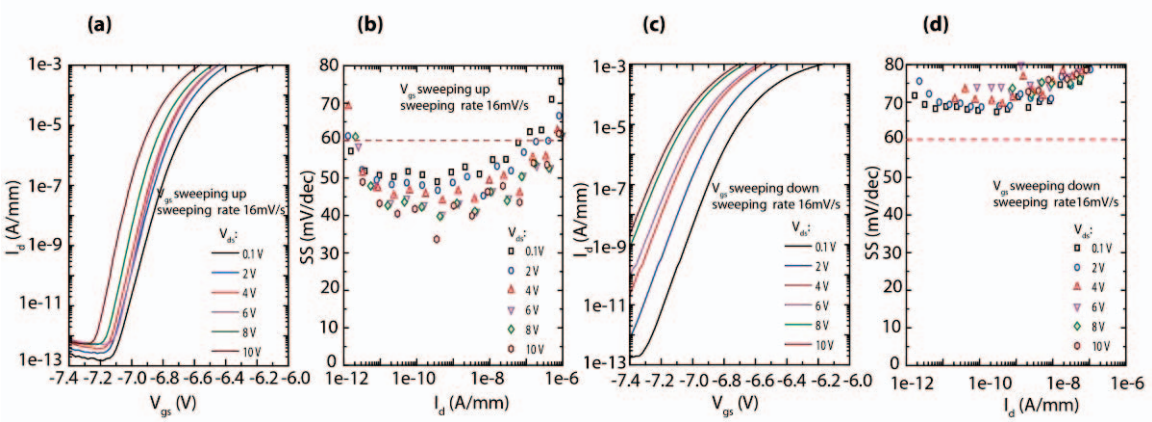

Fig.2 I_d-V_{gs} characteristics of AlGaN/GaN MIS-HEMT at various V_{ds} (RT): (a) V_{gs} sweeping up; (b) SS calculated at the sweeping up conditions, SS< 60mV/dec observed within 6 order of drain current at a wide range of drain bias;(c) V_{gs} sweeping down and (d) SS calculated at the sweeping down conditions, SS > 60 mV is obtained for all the drain bias

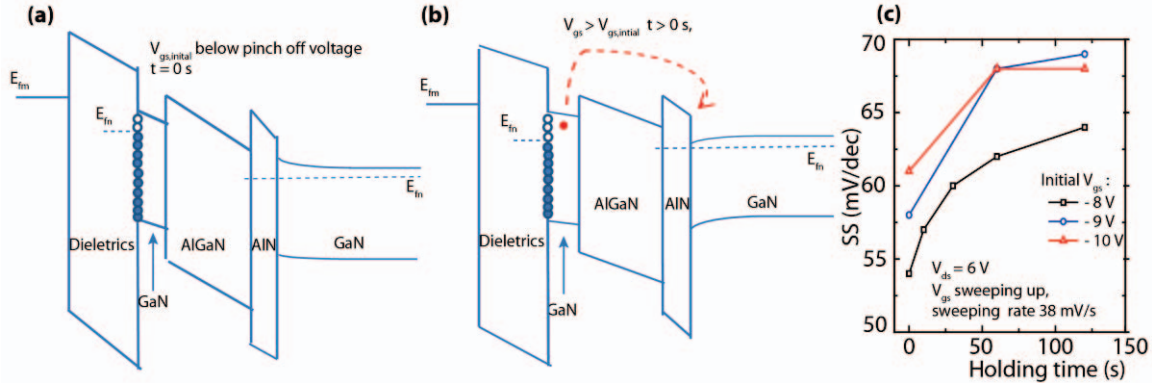

Fig.3 Schematic of AlGaN/GaN MIS-HEMT band diagram: (a) at t = 0 s, $V_{gs} << V_{th}$, the interfacial states are filled with charges; (b) at t > 0 s, V_{gs} sweeps up , charges from the interfacial states inject into the channel thus leading to a total channel charge higher than the gate-field effect alone, Interface states at the dielectric and GaN interface are used to illustrate the de-trapping process, however, the trap states can be present anywhere in the gate stack between the metal gate and the GaN channel and (c) SS as a function of the initial V_{gs} and the holding time at the sweeping up conditions