Optimum Bandgap and Supply Voltage in Tunnel FETs

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Abstract—A physics-based analytic model of the ON- and OFF-currents in a homojunction tunnel field-effect transistor (TFET) is used to understand the relationship between bandgap, gate length, ON-current, OFF-current, ON/OFF current ratio, and supply voltage to meet minimum energy requirements. The model, which applies to direct-bandgap semiconductors, is validated against numerical simulations to show that it captures the trends of more comprehensive simulations. The analytic model is then used to compare alternative channel materials for TFETs. Gate-all-around InAs nanowire and graphene nanoribbon TFETs are used as design examples at gate lengths of 10 and 15 nm and for an ON/OFF current specification of 10^5. The results suggest that TFETs based on 2-D materials can be more energy efficient than semiconductor nanowire TFETs and conventional metal–oxide–semiconductor field-effect transistors for low-power logic.

Index Terms—Analytic model, graphene nanoribbon (GNR), nanowire (NW), tunnel field-effect transistor (TFET).

I. INTRODUCTION

THE sub-60-mV/decade subthreshold swing of the tunnel field-effect transistor (TFET) allows reduction in supply voltage and power dissipation [1]–[3]. Projections based on III–V TFET atomistic simulations and experimentally calibrated models indicate that the TFET is a realistic candidate to complimentary metal–oxide–semiconductor at low supply voltages [4], [5].

In the development of TFETs, the quest for higher drive currents has led to the exploration of lower bandgap channels, for example, InGaAs [6]–[8] and InAs [9]–[11]. Vandenberghe *et al.* [12] showed, using a model based on the Wentzel-Kramers–Brillouin (WKB) approximation that there is an optimum bandgap and doping to maximize the ON current

at a particular supply voltage and without consideration of the OFF current. Khayer and Lake [13] provided an analytic approach for understanding the effect of channel material on both the ON and OFF currents in the TFET. In their assessment, the OFF-state leakage is considered to be independent of the gate length and given by interband tunneling from channel to drain at a supply voltage of 1 V. Subsequent analysis by Luisier *et al.* [14] and Sylvia *et al.* [15] for 5-nm gate length transistors showed that direct source-to-drain tunneling dominates the OFF-state leakage and thus limits the ON/OFF current ratio.

Recently, Kam *et al.* [3] employed an analytic approach to evaluate the transfer characteristic of steep transistors to achieve a minimum energy-delay performance. Their analysis expanded the tradeoff space for optimizing TFETs to include subthreshold swing, ON-current, ON/OFF current ratio, activity factor, and logic depth, and showed that these must be balanced for steep devices to operate with lower energy and shorter delay than the metal–oxide–semiconductor field-effect transistor (MOSFET). The input for the analytic approach of Kam was the transfer characteristic of the steep transistor. Still lacking until now is a general approach that allows the tradeoffs to be explored between bandgap, gate length, ON-current, OFF-current, ON/OFF current ratio, and supply voltage to meet minimum energy requirements. While this can be done numerically and should be for a particular material system and device geometry, this is time consuming and does not yield physical insights across materials systems.

II. ANALYTIC MODEL AND VALIDATION

To be shown is a simple analytic model of the ON and OFF currents for a homojunction direct-bandgap TFET that captures the essential physics of the TFET. This analysis applies to short channel transistors where direct source-to-drain tunneling dominates the OFF-state leakage and extends the results of [16] to 10 nm gate lengths and into 2-D materials [17], [18]. Our model captures the essential relationships among bandgap, gate length, and supply voltage in TFETs with excellent electrostatics such as in gate-all-around nanowire geometries [19] or in 2-D channel materials [18], [30]. The source/drain degeneracy is fixed for simplicity, but its optimization can be found in [12]. Trap-assisted tunneling, which has been observed experimentally [6], is neglected in the model, but could be added when this limitation in TFETs is better understood.

The schematic band diagrams for a generic *n*-channel homojunction *p-i-n* TFET in the ON and OFF states are shown
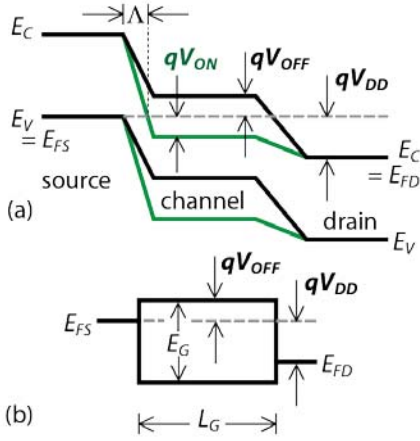
Fig. 1. (a) Schematic band diagram of an n-channel TFET in the ON (green) and OFF state (black). (b) Simplified band diagram in the OFF-state, assuming a source-to-channel junction width of Λ, which is much less than the gate length, L_G. The conduction band, valence band, and energy bandgap are given by their usual symbols, E_C, E_V, and E_G.

in Fig. 1, where the Fermi level is aligned with the valence band maximum in the source, E_{FS}, and the conduction band minimum in the drain, E_{FD}. In the ON state, the conduction band edge in the channel is pulled below the Fermi level in the source (dashed line) by a positive gate bias. This enables electrons to tunnel through a narrow energy barrier of width Λ, at the source–channel junction. The energy window for source-to-channel tunneling in the ON state is qV_{ON}, where q is the electron charge and V_{ON} is the turn-on voltage. The energy qV_{OFF} defines the energy barrier between the source Fermi level and the channel conduction band in the OFF state.

In the OFF state, the leakage is dominated by direct tunneling from source to drain with an energy window given by qV_{DD} [Fig. 1(b)]. The total potential change in the channel in going from the ON to the OFF state depends on the gate-source voltage, V_{GS}, which ranges as high as the supply voltage, V_{DD}. A gate control parameter α, 0.8–0.9 after Khayer and Lake [13], is used to set a proportionality between the gate-source voltage and V_{ON} while the coupling between the gate-source voltage and V_{OFF} is taken to be unity, assuming negligible injected charge in the channel in the OFF-state: $V_{ON}/\alpha + V_{OFF} = V_{DD}$.

For short channel TFETs, both ON- and OFF-state currents are interband tunneling currents and are calculated by considering 1-D ballistic transport for nanowires and nanoribbons [2] and an abrupt Fermi function

$$I = \frac{q}{\pi \hbar} \int T(E) dE \tag{1}$$

where $\hbar$ is the reduced Plank constant, and $T(E)$ is the 1-D tunneling transmission coefficient. Here the spin degeneracy is 2 and the valley degeneracy is 1. The lowest conduction subband and the highest valence subband are assumed to connect via a single dominant imaginary band in the bandgap for tunneling, which has been shown to be true in direct semiconductors from full-band atomistic simulations [21]. So the transmission coefficient can be calculated using
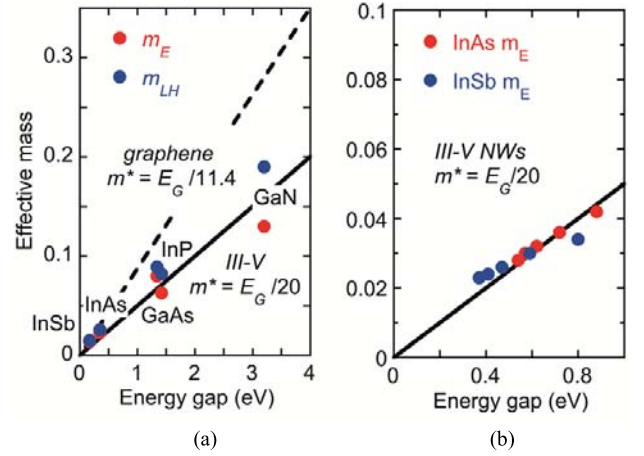

Fig. 2. (a) Electron effective mass (red dots) and light-hole effective mass (blue dots) versus energy bandgap for zinc-blende III–V semiconductors [23]. The electron effective mass, $m*$, is given by the electron effective mass, m_E which is approximately equal to the light-hole effective mass, m_{LH}. (b) Electron effective mass versus bandgap for nanowires of InAs (red dots) and InSb (blue dots) with diameters in the range from 4 to 12 nm from Khayer and Lake [25].

Kane's two-band model [22]

$$T(E) = \exp\left(-2\int k\,dx\right)$$

$$= \exp\left(-\frac{2\sqrt{2m_E}}{\hbar}\int\sqrt{E(1 - E/E_G)}\,dx\right) \tag{2}$$

where κ is the magnitude of the imaginary wave vector and m_E is the electron effective mass. In Kane's two-band model, the electron effective mass in the lowest conduction band is assumed to be equal to the light-hole effective mass in the highest valence band, which is reasonable for bulk zinc-blende III–V materials [23] with direct bandgaps [21]. It also applies for carbon-based materials that have a symmetric band structures.

The relationship between effective mass and bandgap is roughly linear for III–V semiconductors, as shown in Fig. 2(a) and as anticipated from two-band $k \cdot p$ theory [24]. For III–V semiconductors, the relationship is approximately $m_E = E_G/20$ where E_G is given in eV. For nanowires (NWs), the energy bandgap increases with smaller NW diameter owing to quantum confinement. The calculated bandgaps and electron effective masses for InAs and InSb NWs are shown in Fig. 2(b) from Khayer and Lake [25], which uses a 3-D discretized eight-band $k \cdot p$ model. This model accounts for band non-parabolicity in the conduction band. The linear relation $m_E = E_G/20$ is also still a good approximation for NWs as shown in Fig. 2(b). For graphene nanoribbons, the relationship between effective mass and bandgap is given by $m_E = E_G/11.4$ [26].

Using (2), the ON-state tunneling transmission coefficient, T_{ON}, is calculated for electrons tunneling through a triangular energy barrier [27]

$$T_{ON} = \exp\left(-\frac{\pi\sqrt{2m_E}E_G^{3/2}}{4q\hbar\xi}\right) \tag{3}$$
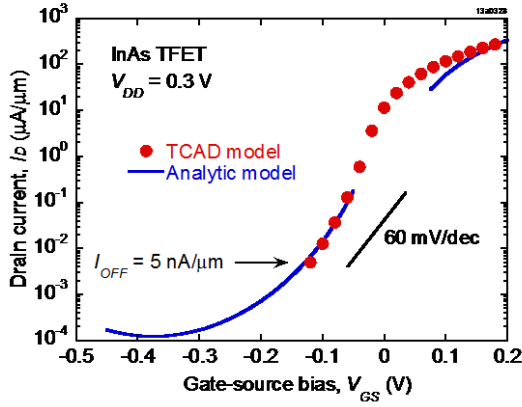
Fig. 3. Calculated transfer characteristics of an InAs GAA NW TFET (solid blue line) at a supply voltage of 0.3 V with $L_G = 15$ nm, $t_{OX} = 0.6$ nm, $\epsilon_{OX} = 3.9\epsilon_O$, $E_G = 1.05$ eV, and the nanowire diameter $d_S = 3.5$ nm. The calculated results for the InAs GAA NW TFET from this paper is in fair agreement with TCAD simulation results (red dots) at $I_{OFF} = 5$ nA/μm.
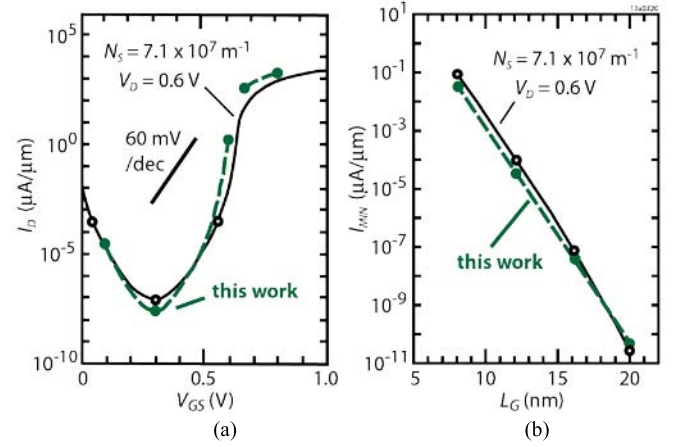

Fig. 4. (a) Calculated transfer characteristics of a GNR TFET (dashed line) at a supply voltage of 0.6 V. The ribbon width $w = 1.2$ nm, $E_G = 1.22$ eV, $L_G = 16$ nm, $t_{OX} = 1$ nm, $\varepsilon_{OX} = 3.9\varepsilon_0$. The calculated results for the GNR TFET in this paper is in fair agreement with NEGF [18] simulation results (solid line) where the source/drain doping is $7.1 \times 107/m$. (b) Comparison of the minimum leakage current versus gate length from NEGF (solid line) [18] with the analytic model (dashed line) illustrating that it also captures the gate length dependence.

with an average electric field in the tunneling direction given by $\xi = E_G/(q\Lambda)$. Here Λ is related to the electrostatic length of the junction, λ, determined from a solution of Poisson's equation [28]. The electrostatic potential in the source–channel junction can be approximated as $\phi(x) \approx (E_G/q + V_{ON})\exp(-x/\lambda)$, $V_{ON} > 0$ (see Fig. 1). It follows that at $x = 0$, $\phi(0) = E_G/q + V_{ON}$ and at $x = \Lambda$, $\phi(\Lambda) = (E_G/q + V_{ON})\exp(-\Lambda/\lambda)$ which equals V_{ON}, then

$$\Lambda = \lambda \ln\left(\frac{E_G + qV_{ON}}{qV_{ON}}\right). \tag{4}$$

The ON-state current is then written by substituting the energy-independent ON-state tunneling transmission coefficient T_{ON} into (1) and completing the integration over the tunneling window

$$I_{ON} = \frac{q^2}{\pi\hbar} T_{ON} V_{ON}. \tag{5}$$

In the OFF-state, the tunneling transmission coefficient T_{OFF} is assumed to be approximated by electrons tunneling through a rectangular energy barrier with a length equal to the gate length. The flat channel profile [18], [19] is a good estimate for an Electrostatically well-designed TFET where the electrostatic scaling length is small relative to the gate length [29], [30]

$$T_{OFF}(E) = \exp\left(-\frac{2\sqrt{2m_E L_G}}{\hbar}\sqrt{E(1 - E/E_G)}\right). \tag{6}$$

The OFF-state current is given by

$$I_{OFF} = \frac{q}{\pi\hbar} \int_0^{qV_{DD}} T_{OFF}(E + qV_{OFF})dE. \tag{7}$$

To test this analytic model, the transfer characteristics of an InAs gate-all-around, 3.5 nm diameter, NW TFET are calculated and compared with Synopsys TCAD simulations [31] (see Fig. 3). In the TCAD model, drift-diffusion with Fermi statistics was used. Quantum confinement was accounted for by adjusting the bandgap and density-of-states effective masses obtained from tight-binding-simulated band structure. Tunneling was calculated using the Dynamic NonlocalPath tunneling model, where the tunneling effective mass was derived by fitting the imaginary band structure from tight binding. Even though the tunneling model in TCAD is based on the WKB approximation, the results were compared with NEGF quantum simulation and good agreement was achieved. Agreement was also shown in [28] with double-gate TFET simulations on 7 nm thin InGaAs channels.

In Fig. 3, the comparison of our analytic model with TCAD simulations is made at a gate length of 15 nm, at a supply voltage of 0.3 V and for the same OFF current density, 5 nA/μm. The analytic model is in good approximation to the numerical simulations in the bias ranges of interest. It is not exact, but provides a reasonable estimate for understanding tradeoffs and trends. Use of the model to explore tradeoffs at NW diameters below 3.5 nm should be proceeded by comparison and validation against reliable experimental results or simulations which comprehend quantization.

The transfer characteristics of a graphene nanoribbon TFET are also calculated analytically and compared with the NEGF method used by Chin *et al.* [18] [see Fig. 4(a)]. For this comparison, the gate length is 16 nm, the supply voltage is 0.6 V, and the ribbon width is 1.2 nm. A source and drain doping concentration of $7.1 \times 10^7/m$ is chosen to align the Fermi level with the valence and conduction edges, respectively, to minimize source depletion and to be consistent with the model energy band diagrams shown in Fig. 1. The analytic model captures the ambipolar transport in the TFET and provides a good representation of the ON- and OFF-state currents. The minimum currents predicted by the analytic model also capture the gate length dependence as shown in
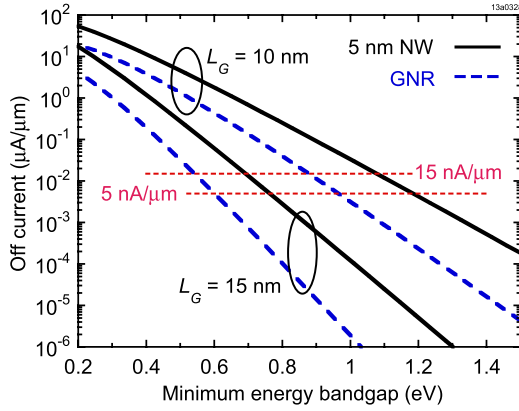
Fig. 5. OFF-state current versus the minimum energy bandgap, E_G, that is needed for NW TFETs (solid line) and GNR TFETs (dashed line) with gate lengths of 15 and 10 nm. At a gate length, L_G, of 15 nm, for an OFF-state current of 5 nA/μm, the bandgap of the NW has to be at least 0.77 eV and the bandgap of the GNR has to be at least 0.6 eV. As the gate length is scaled to 10 nm, the minimum bandgaps of the NW and GNR rise to 1.19 and 0.93 eV, respectively, to meet this $I_{OFF} = 5$ nA/μm requirement.

Fig. 4(b) and are in agreement with the NEGF simulations of Chin *et al.* [18].

III. OPTIMIZATION OF BANDGAP AND SUPPLY VOLTAGE

With an analytic model which captures the essential physics and trends, it becomes possible to explore the tradeoffs between bandgap and supply voltage. Following the circuit-level energy-performance analysis of Kam *et al.* [3], the target ON/OFF current ratio is chosen to be 10^5, the optimized ratio for TFETs. At this fixed optimized ON/OFF current ratio, the lower optimized supply voltage and lower effective subthreshold swing is an indicator of a more energy-efficient device. The electrostatic length, λ, is fixed to be 1.5 and 1.0 nm for the NW and GNR TFETs, respectively. All the currents are normalized to twice the NW diameter or twice the ribbon width.

The procedure for the optimization of bandgap and supply voltage proceeds in two steps. First, the minimum bandgap is determined to meet the OFF current requirement. This is determined from (7) which shows that the OFF current depends on both V_{OFF} and V_{DD}; however, the minimum V_{DD} can be inferred from the band diagram shown in Fig. 1(b) by noting first that the relationship between the OFF-state voltage and supply voltage is $V_{OFF} = (E_G/q - V_{DD})/2$, or $V_{DD} = E_G/q - 2V_{OFF}$. Next, note, from the earlier definition of V_{ON}, $V_{ON}/\alpha + V_{OFF} = V_{DD}$, and the fact that V_{ON} is always positive, that V_{OFF} must always be less than V_{DD}. Therefore, the minimum bandgap condition occurs when $V_{OFF} = V_{DD} = E_G/(3q)$ and this then defines the minimum OFF current in (7).

The minimum OFF current versus bandgap is shown in Fig. 5 for a 5 nm diameter NW TFET and the GNR TFETs for two different gate lengths, 10 and 15 nm. Two OFF current density requirements are considered, 5 and 15 nA/μm (with ON current of 1500 μA/μm) corresponding to low-power (LP) and high-performance (HP) transistors, respectively. For this example, the minimum energy gap has to be at least 0.77 eV
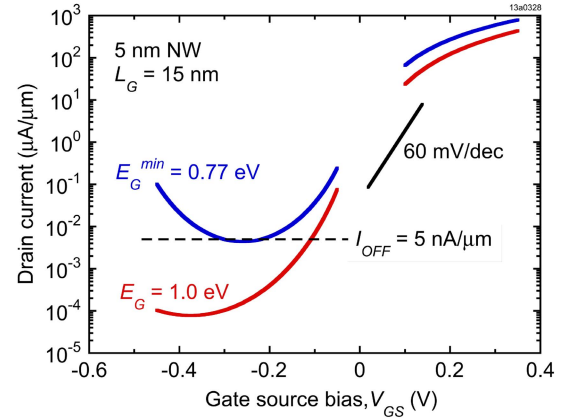

Fig. 6. Transfer characteristics of a 5 nm diameter InAs NW TFET with the minimum EG (dotted line) and a larger EG (solid line) for the required $I_{OFF} = 5$ nA/mm. It is shown that the TFET achieves a steeper subthreshold slope by increasing the bandgap from the minimum E_G and reducing V_{OFF}.

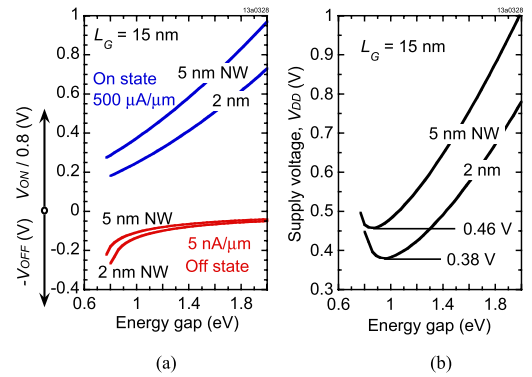(a)   (b)

Fig. 7. Tradeoff space for TFETs: (a) For a given ON-OFF current ratio and gate length, constant current density plots show the relation between V_{ON}, V_{OFF}, and E_G for the InAs NW TFET (diameter of 2 and 5 nm). (b) Supply voltage versus bandgap showing an optimum bandgap to minimize the supply voltage.

to achieve an OFF current of 5 nA/μm for the 5 nm NW TFET with a gate length of 15 nm.

The transfer characteristic of the 5 nm diameter InAs TFET is shown as the blue line in Fig. 6, confirming that the minimum OFF current of 5 nA/μm is obtained at $V_{OFF} = E_G/q/3$. It is also shown that this TFET can be switched at a steeper subthreshold slope with a larger energy bandgap and a smaller V_{OFF} (red line) by increasing the bandgap. However, it comes at the expense of lower ON current.

The design space can be compactly summarized as shown in Fig. 7(a) and (b). In Fig. 7(a), constant current plots are made to show how V_{ON} and V_{OFF} from (5) and (7) depend on bandgap for an ON/OFF ratio of 10^5. Since $V_{ON}/\alpha + V_{OFF} = V_{DD}$ and $\alpha = 0.8$, the supply voltage can be readily calculated for any band gap. V_{DD} is plotted versus bandgap in Fig. 7(b) where it is clear that there is an optimum bandgap of the channel material for a particular gate length and ON/OFF current requirement.

Similar plots can be made for the GNR TFET and these are shown in Fig. 8 where in addition to showing two gate
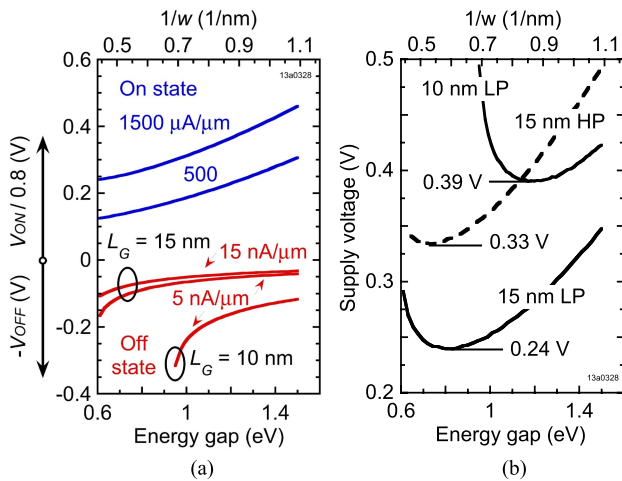
Fig. 8. (a) Similar plot as in Fig. 7(a) but with GNR TFETs. (b) For low-power application, $I_{\rm OFF} = 5$ nA/μm and the $I_{\rm ON}/I_{\rm OFF}$ ratio of 105, the minimum $V_{\rm DD}$ is 0.24 and 0.39 V for $L_G = 15$ and 10 nm, respectively. For high-performance application at $L_G = 15$ nm, $I_{\rm ON} = 1500$ μA/μm, and the $I_{\rm ON}/I_{\rm OFF}$ ratio of 105, the minimum $V_{\rm DD}$ is 0.33 V.

lengths the comparison is made for the two different OFF current requirements. Comparing Figs. 7(b) and 8(b), it is seen that the GNR TFETs have lower optimized supply voltage than the NW TFETs, which is due to the larger effective mass of graphene nanoribbons and the smaller scaling length for 2-D transistors [3]. In Fig. 8(b), it is shown that the optimized supply voltage increases with shorter gate length because bandgap must increase to meet the OFF-current requirement. Similarly, HP devices can meet the ON/OFF ratio specification with smaller bandgaps and the optimum supply voltage can take on a lower value for the LP technology.
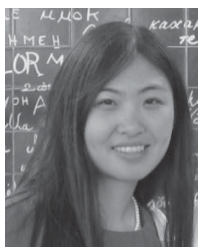
IV. CONCLUSION

A physics-based analytic model of advanced TFETs was formulated, compared with more sophisticated models, and then used to show how bandgap, supply voltage, and gate-length tradeoff to meet a given ON/OFF ratio. Both InAs NW and GNR TFET geometries were used to illustrate the model.

REFERENCES

[1] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[2] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, Nov. 2011.

[3] H. Kam, T.-J. K. Liu, and E. Alon, "Design requirements for steeply switching logic devices," *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 326–334, Feb. 2012.

[4] U. E. Avci, R. Rios, K. Kuhn, and I. A. Young, "Comparison of performance, switching energy and process variations for the TFET and MOSFET in logic," in *Proc. Symp. VLSI Technol.*, Jun. 2011, pp. 124–125.

[5] U. E. Avci, S. Hasan, D. E. Nikonov, R. Rios, and I. A. Young, "Understanding the feasibility of scaled III–V TFET for logic by bridging atomistic simulations and experimental results," in *Proc. Symp. VLSI Technol.*, Jun. 2012, pp. 183–184.
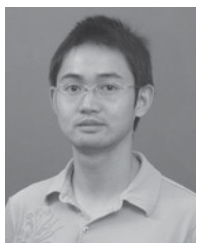
[6] S. Mookerjea *et al.*, "Experimental demonstration of 100nm channel length In0.53Ga0.47As-based vertical inter-band tunnel field effect transistors (TFETs) for ultra low-power logic and SRAM applications," in *Proc. Int. Electron Devices Meeting (IEDM)*, Dec. 2009, pp. 1–4.

[7] H. Zhao, Y. Chen, Y. Wang, F. Zhou, F. Xue, and J. Lee, "InGaAs tunneling field-effect-transistors with atomic-layer-deposited gate oxides," *IEEE Trans. Electron Device*, vol. 58, no. 9, pp. 2990–2995, Sep. 2011.

[8] G. Dewey *et al.*, "Fabrication, characterization, and physics of III–V heterojunction tunneling field effect transistors (H-TFET) for steep sub-threshold swing," in *Proc. Int. Electron Devices Meeting (IEDM)*, Dec. 2011, pp. 33.6.1–33.6.4.

[9] K. E. Moselund, H. Schmid, C. Bessire, M. T. Bjork, H. Ghoneim, and H. Riel, "InAs–Si nanowire heterojunction tunnel FETs," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1453–1455, Oct. 2012.

[10] G. Zhou *et al.*, "Novel gate-recessed vertical InAs/GaSb TFETs with record high ION of 180 μA/μm at VDS = 0.5 V," in *Proc. Int. Electron Devices Meeting (IEDM)*, Dec. 2012, pp. 32.6.1–32.6.4.

[11] A. W. Dey *et al.*, "High-current GaSb/InAs(Sb) nanowire tunnel field-effect transistors," *IEEE Electron Devices Lett.*, vol. 34, no. 2, pp. 211–213, Feb. 2013.

[12] W. G. Vandenberghe *et al.*, "A model determining optimal doping concentration and material's band gap of tunnel field-effect transistors," *Appl. Phys. Lett.*, vol. 100, no. 19, p. 193509, May 2012.

[13] M. A. Khayer and R. K. Lake, "Drive currents and leakage currents in InSb and InAs nanowire and carbon nanotube band-to-band tunneling FETs," *IEEE Electron Devices Lett.*, vol. 30, no. 12, pp. 1257–1259, Dec. 2009.

[14] M. Luisier, M. Lundstrom, D. A. Antoniadis, and J. Bokor, "Ultimate device scaling: Intrinsic performance comparisons of carbon-based, InGaAs, and Si field-effect transistors for 5 nm gate length," in *Proc. Int. Electron Devices Meeting (IEDM)*, Dec. 2011, pp. 11.2.1–11.2.4.

[15] S. S. Sylvia, H.-H. Park, M. A. Khayer, K. Alam, G. Klimeck, and R. K. Lake, "Material selection for minimizing direct tunneling in nanowire transistors," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2064–2069, Aug. 2012.

[16] Q. Zhang, Y. Lu, C. A. Curt, D. Jena, and A. Seabaugh, "Analytic determination of the optimum bandgap for a tunnel FET," in *Proc. Device Res. Conf.*, 2012, pp. 1–2.

[17] Q. Zhang, T. Fang, H. Xing, A. Seabaugh, and D. Jena, "Graphene nanoribbon tunnel transistors," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1344–1346, Dec. 2008.

[18] S.-K. Chin, D. Seah, K.-T. Lam, G. S. Samudra, and G. Liang, "Device physics and characteristics of graphene nanoribbon tunneling FETs," *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 3144–3152, Nov. 2010.

[19] M. Luisier and G. Klimeck, "Atomistic full-band design study of InAs band-to-band tunneling field-effect transistors," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 602–604, Jun. 2009.

[20] J. Knoch and J. Appenzeller, "Tunneling phenomena in carbon nanotube field-effect transistors," *Phys. Status Solidi A*, vol. 205, no. 4, pp. 679–694, Apr. 2008.

[21] M. Luisier and G. Klimeck, "Simulation of nanowire tunneling transistors: From the Wentzel–Kramers–Brillouin approximation to full-band phonon-assisted tunneling," *J. Appl. Phys.*, vol. 107, no. 8, pp. 084507-1–084507-6, Apr. 2010.

[22] E. O. Kane, "Zener tunneling in semiconductors," *J. Phys. Chem. Solids*, vol. 12, no. 2, pp. 181–188, 1959.

[23] (2013, Jul.). *New Semiconductor Materials. Characteristics and Properties* [Online]. Available: http://www.ioffe.ru/SVA/NSM/

[24] P. Yu and M. Cardona, *Fundamentals of Semiconductors: Physics and Material Properties*. New York, NY, USA: Springer-Verlag, 2010.

[25] M. A. Khayer and R. K. Lake, "Performance of *n*-type InSb and InAs nanowire field-effect transistors," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 2939–2945, Nov. 2008.

[26] W. Vandenberghe, B. Soree, W. Magnus, and G. Groeseneken, "Zener tunneling in graphene based semiconductors—The k.p method," in *Proc. Int. Conf. Electron Dyn. Semicond., OptoElectron. Nanostruct.* vol. 193. 2009, pp. 1–4.

[27] E. O. Kane, "Theory of tunneling," *J. Appl. Phys.*, vol. 32, no. 1, pp. 83–91, Jan. 1961.

[28] L. Liu, D. Mohata, and S. Datta, "Scaling length theory of double-gate interband tunnel field-effect transistors," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 902–908, Apr. 2012.

[29] C. P. Auth and J. D. Plummer, "Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's," *IEEE Electron Device Lett.*, vol. 18, no. 2, pp. 74–76, Feb. 1997.

[30] Q. Zhang, Y. Lu, H. G. Xing, S. J. Koester, and S. O. Koswatta, "Scalability of atomic-thin-body (ATB) transistors based on graphene nanoribbons," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 531–533, Jun. 2010.

[31] *Sentaurus Device User Guide Version E*, Synopsys Inc., Mountain View, CA, USA, 2010.

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