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Transistor Switches Using Active Piezoelectric Gate Barriers

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ABSTRACT This paper explores the consequences of introducing a piezoelectric gate barrier in a normal field-effect transistor. Because of the positive feedback of strain and piezoelectric charge, internal charge amplification occurs in such an electromechanical capacitor resulting in a negative capacitance. The first consequence of this amplification is a boost in the ON-current of the transistor. As a second consequence, employing the Lagrangian method, we find that using the negative capacitance of a highly compliant piezoelectric barrier, one can potentially reduce the subthreshold slope of a transistor below the room-temperature Boltzmann limit of 60 mV/decade. However, this may come at the cost of hysteretic behavior in the transfer characteristics.

INDEX TERMS Electromechanical capacitor, electrostriction, negative capacitance, piezoelectric barrier, piezoelectric field-effect transistor (PiezoFET), subthreshold slope (SS).

I. INTRODUCTION

SCALING of the size of field-effect transistors (FETs) has improved their performance and integration densities in integrated circuits for over two decades. Most conventional transistors make use of a passive insulating barrier layer between the gate metal and the semiconductor channel to modulate the density of the conduction channel electrons or holes. Because the intrinsic properties of a passive-gate barrier do not change with the applied voltage, they impose certain fundamental limitations on the resulting device performance.

One such limitation is the subthreshold slope (SS), i.e., the gate voltage required to change the drain current by an order of magnitude [1], [2], given by SS $= m \times 60$ mV/decade at room temperature [3], [4]. Here, $m = 1 + C_{sc}/C_{ins}$ is the body factor, C_{sc} is the semiconductor channel capacitance, and C_{ins} is the gate insulator capacitance. In a traditional FET switch with a passive-gate dielectric, such as SiO_2, $C_{ins} > 0$ and thus $m > 1$, which leads to SS > 60 mV/decade [4]. This result, combined with circuit requirements for the ON-current I_{ON} and the ON/OFF ratio I_{ON}/I_{OFF}, establishes a minimum supply voltage V_{dd}, which does not scale in direct proportion with the feature size [1], [2], [5]. Scaling of V_{dd} has hit a roadblock, giving rise to heat generation associated with the large power dissipation density in ICs [1], [2], [5], [6], since the dissipated power is proportional to the square of the voltage $P_{diss} \propto V_{dd}^2$ [2], [7], [8]. Many ideas based on alternate transport mechanisms in the semiconductor channel, such as interband tunneling, or impact ionization are being explored to lower V_{dd}.

An interesting alternative is to replace the passive-gate barrier with an active one. A first proposal of an active ferroelectric insulator [3] predicts internal voltage gain: the voltage across the gate insulator layer is larger than the applied external gate voltage. The origin of the internal voltage gain is the collective alignment of the microscopic electric dipoles in the ferroelectric layer in response to the external electric field produced by the gate voltage. The alignment of dipoles generates a voltage of its own, thus amplifying the voltage that makes it to the semiconductor channel. Under appropriate bias conditions [3], the insulator capacitance provided by the ferroelectric is mathematically negative ($C_{ins} < 0$), causing $m = 1 + C_{sc}/C_{ins} < 1$ and SS < 60 mV/decade. Then, such an active-gate FET will require a lower gate voltage to create the same charge as a conventional FET with passive-gate dielectrics [3], thereby facilitating device scaling.

In this paper, we explore the device consequences of using a piezoelectric insulator as the active gate barrier in a transistor instead of the ferroelectric barrier.

Piezoelectric gate barriers are at the heart of commercially available III-nitride heterostructure transistors [9], [10]. We first consider an active compliant piezoelectric layer as the insulator in a parallel-plate capacitor. We find that this simple electromechanical capacitor system exhibits a remarkably rich range of behavior. We show that negative capacitance emerges as a natural response to the applied voltage. In this regime of negative capacitance, we show that we obtain a higher charge than in a corresponding capacitor with a passive dielectric. Nontrivial capacitance–voltage behavior in such capacitors has also been reported experimentally [11], [12]. Next, we port the parallel-plate electromechanical capacitor to the gate capacitor of a FET. We show how this piezoelectric gate-stack enables a higher ON-current than in a transistor with a passive dielectric due to the internal charge amplification. Finally, building upon [13]–[15], we discuss the possibility of using the negative capacitance regime of a highly compliant piezoelectric barrier to obtain sub-60-mV/decade switching in a transistor.

II. ELECTROMECHANICAL CAPACITOR

We begin by discussing the piezoelectric parallel-plate capacitor. Consider the parallel-plate capacitor of area A shown in Fig. 1(a). The equilibrium thickness t_0 of the piezoelectric insulator layer sandwiched between the metal plates changes to $t = t_0 - \delta$ when a voltage V is applied on the plates, as shown in Fig. 1(b). The strain is defined as $s = \delta/t_0$. The equal and opposite sheet charge σ_m that develop on the metal plates set up an attractive force between them, which strains the insulator. This effect, called electrostriction, is the electric-field-induced reduction of the thickness of a material; it occurs in all insulators, whether or not the layer is piezoelectric. However, if the insulator is piezoelectric, the strain amplifies the surface charge of the insulator. This mechanism sets up a positive feedback between the thickness and the electric field, and is responsible for the appearance of negative capacitance. To find the capacitance in the presence of such electromechanical coupling, one must first find the net metal charge σ_m as a function of the external (battery) voltage, and then take its derivative. This requires us to identify the values of surface charge σ_s that develops at the surface of the insulator. The resulting electric-field profile is constant, equal to $E = V/t$, and the voltage drops linearly across the insulator.

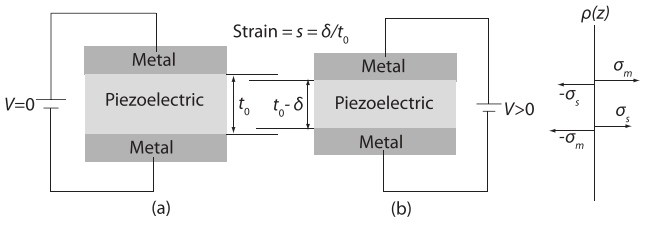

FIGURE 1. (a) Schematic cross section of a parallel-plate electromechanical capacitor with a piezoelectric barrier layer of thickness t_0 at $V = 0$ V. (b) Layer thickness shrinks to $t_0 - \delta$ when voltage V is applied. Sheet charge distribution $\rho(z)$ with $\pm\sigma_m$ on the metal plates and surface charges $\pm\sigma_s$ on the piezoelectric insulator layer.

Maxwell's boundary conditions across the metal–insulator interface require the normal components of the displacement vector to obey $D_d - D_m = \sigma_m$. D_d is the displacement field in the dielectric related to the values of the surface charge σ_s by $D_d = \epsilon_0 E + \sigma_s$, where $\sigma_s = (\epsilon_d - \epsilon_0)E + e_{33}s + \sigma_{sp}$ or $D_d = \epsilon_d E + e_{33}s + \sigma_{sp}$. Here, $\epsilon_d = \epsilon_0(1 + \chi_d)$ is the net dielectric constant of the piezoelectric layer, and χ_d is its electric susceptibility. The electric field is $E = V/t$, where $t = t_0(1 - s)$ is the thickness of the strained insulator layer. We explicitly allow for both piezoelectric polarization and spontaneous polarization for an active dielectric material. The strain-induced piezoelectric contribution to the charge (to linear order) is $e_{33}s$, where e_{33} is the piezoelectric coefficient in units of C/m^2, and $s = \delta/t_0$ is the strain along the field. The charge due to spontaneous polarization is σ_{sp}, also in units of C/m^2. Inside the metal, $D_m = 0$. Therefore, we obtain the relation

$$\sigma_m = \epsilon_d \frac{V}{t_0(1-s)} + e_{33}s + \sigma_{sp}. \tag{1}$$

This relation illustrates how the strain s explicitly enters the electrostatic relation between the metal charge and the voltage across the capacitor. If one neglects the spontaneous polarization ($\sigma_{sp} \to 0$), piezoelectric effect ($e_{33} \to 0$), and strain ($s \to 0$), we get $\sigma_m = C_0 V$, (with $C_0 = \epsilon_d/t_0$), the standard textbook formula of a parallel-plate capacitor. However, we note that one can turn OFF the spontaneous polarization and the piezoelectric polarization by the choice of material, and yet the factor $(1 - s)$ in the denominator will persist: this is the electrostriction term.

The mechanical pressure P experienced by the insulator is the electrical force F per unit area A. It is thus related to the metal charge [16], [17] via $P = F/A = \sigma_m^2/\epsilon_d$. To linear order, the pressure depends on the strain via the stiffness coefficient $P = C_{33}s$, where C_{33} is in units of N/m^2 or pascal. Thus, we obtain the strain as a function of the metal charge: $s = \sigma_m^2/\epsilon_d C_{33}$. Substituting in (1) and rearranging, we have the desired relation between the metal charge in response to an applied voltage

$$C_0 V = \sigma_m - \sigma_{sp} + \frac{(\sigma_{sp} - e_{33})}{\epsilon_d C_{33}}\sigma_m^2 - \frac{1}{\epsilon_d C_{33}}\sigma_m^3 + \frac{e_{33}}{(\epsilon_d C_{33})^2}\sigma_m^4. \tag{2}$$

The right-hand side is a fourth-order polynomial in σ_m, and captures the electromechanical coupling physics. Let us explore its consequences. The sheet charge on the metal $n_m = \sigma_m/q$ from (2) is plotted as a function of the applied voltage V in Fig. 2 for different sets of material parameters. For example, $e_{33} = 3.1$ C/m^2 and $\epsilon_d = 15\epsilon_0$ correspond to the piezoelectric material $Sc_xAl_{1-x}N$ [18], [19]. The value of C_{33} is allowed to vary arbitrarily in order to investigate the range of behavior of the piezoelectric capacitor. We also

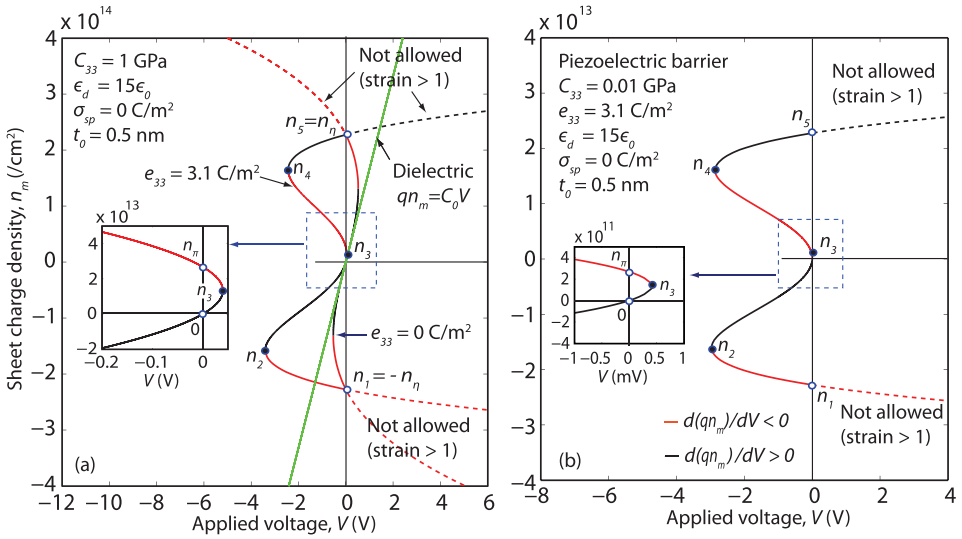

FIGURE 2. **(a) Charge–voltage ($qn_m - V$) characteristic of the electromechanical capacitor. Various charge states, such as the positive capacitance segments $[n_2, n_3]$, $[n_4, n_5]$, where the values of slope $C_{PE} = d(qn_m)/dV > 0$ are positive, and negative capacitance segments $[n_1, n_2]$, $[n_3, n_4]$, where $C_{PE} = d(qn_m)/dV < 0$, are shown. (b) Characteristics of a piezoelectric capacitor with a lower stiffness and more compliant barrier with $C_{33} = 0.01$ GPa make negative capacitance accessible at a lower charge $\sim 10^{11}$ cm^{-2}, as shown in the inset.**

assume $\sigma_{sp} = 0$. A nonzero value of σ_{sp} merely causes a horizontal shift of the $\sigma_m - V$ curve (see Section I of the supplementary material for details). The physics of the piezoelectric capacitor with $\sigma_{sp} = 0$ becomes apparent by factoring (2) into

$$V = \frac{q}{C_0}(n_m)\left(1 - \frac{n_m}{n_\eta}\right)\left(1 + \frac{n_m}{n_\eta}\right)\left(1 - \frac{n_m}{n_\pi}\right) \qquad (3)$$

where $qn_m = \sigma_m$, $qn_\pi = \epsilon_d C_{33}/e_{33}$, and $qn_\eta = (\epsilon_d C_{33})^{1/2}$. Setting $V = 0$ in (3), we obtain four real roots $n_{m0} = 0, +n_\eta, -n_\eta$, and $+n_\pi$. For a rigid ($C_{33} \to \infty$), nonpiezoelectric ($e_{33} = 0$) insulator, $n_\eta, n_\pi \to \infty$, whereupon we recover $\sigma_m = qn_m = C_0 V$, and the metal charge is a linear function of voltage as shown in Fig. 2(a) (green line).

On the other hand, for a compliant nonpiezoelectric insulator, $C_{33} > 0$, (3) reduces to a cubic equation with roots $0, \pm n_\eta$ at $V = 0$. This is in fact a prototypical description of a nanoelectromechanical switch [20]. The two additional roots $\pm n_\eta$ make the dependence of σ_m on V nonlinear with two additional zero crossings. Multiple zero crossings of the $qn_m - V$ curve mathematically guarantee that there must be the regions of negative slope $d(qn_m)/dV < 0$. This is shown in red in the flipped S-shaped curve of Fig. 2(a), where $C_{33} = 1$ GPa is assumed. In these regions, the electromechanical capacitor has a negative capacitance.

However, the negative capacitance corresponds to very high values of charge density ($>10^{14}$ cm^{-2}) and strain s (>0.3), as shown in Fig. 3(a). Though rapid progress is being made in the solid-state electrostatic gating of ever increasing carrier densities in semiconductors [21], methods to reduce the charge and strain are desirable. Now, consider the piezoelectric insulator, where $C_{33} > 0$ and $e_{33} > 0$.

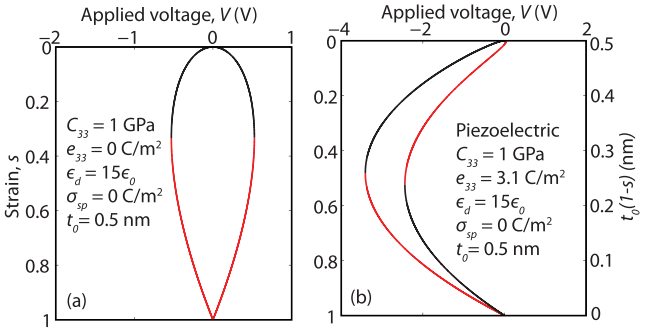

FIGURE 3. **Strain as a function of voltage in (a) nonpiezoelectric insulator layer with $C_{33} = 1$ GPa, $e_{33} = 0$ C/m^2, and $t_0 = 0.5$ nm and (b) piezoelectric insulator layer with $C_{33} = 1$ GPa and $e_{33} = 3.1$ C/m^2. Strain $s < 1$ is physically accessible in solid state, where the remaining layer thickness $t_0(1 - s) > 0$. Red (black) curves: strain corresponding to the negative (positive) capacitance charge states.**

Notice that n_η is independent of e_{33}. The root n_π depends on e_{33}, and its location determines the shape of the $qn_m - V$ curve. If $e_{33} > (\epsilon_d C_{33})^{1/2}$, then $0 < n_\pi < n_\eta$ and negative capacitance appears in the two charge segments $[n_1 = -n_\eta, n_2]$ and $[n_3, n_4]$ shown in Fig. 2 (red). It is important to realize that piezoelectricity lowers both the charge density ($\sim 10^{13}$ cm^{-2}) [inset of Fig. 2(a)] and strain <0.01 [Fig. 3(b)] at which negative capacitance appears, compared with electrostriction alone. For vanishingly small voltages around zero, the piezoelectric capacitor behaves exactly like a parallel-plate capacitor—a straight line. But the additional benefit of the above coupling is the increased charge density compared with a passive dielectric due to the piezoelectric amplification—this effect will boost the ON-state current in a transistor. From (3), the piezoelectric amplification is

$n_m - (C_0 V/q) \approx (n_m^2/n_\pi) + \cdots$ to leading order. Finally, if we use a highly compliant piezoelectric, for example, with $C_{33} = 0.01$ GPa, negative capacitance can be accessed at very low charge density $\sim 10^{11}$ cm^{-2}, as shown in Fig. 2(b). These highly compliant piezoelectrics can potentially enable the design of transistors with steep subthreshold behavior, but require new materials as will be described later. We also remark here that Pauli's exclusion principle of solid matter and quantum compressibility restricts $s < 1$. Therefore, for piezoelectric insulators, the metal charge will be restricted to $-n_\eta < n_m < +n_\eta$. It may be possible to go beyond these restrictions [$s > 1$, Fig. 2 (dashed lines)] in gaseous plasmas, where charged ion plate electrodes can pass through each other. But we do not pursue that line of analysis here, by restricting the discussion to solid metals and dielectrics.

III. TRANSISTOR WITH A PIEZOELECTRIC BARRIER

We now explore how the presence of the piezoelectric capacitor in the gate of a transistor with a semiconductor channel changes the traditional characteristics. The semiconductor channel could be formed of a gapped 2-D crystal, such as MoS_2, or a 3-D crystal semiconductor such as Si or GaN. The semiconductor is characterized by the valley degeneracy g_v of the conduction (or valence) band. We assume the energy dispersion of each valley to be the same, characterized by an effective mass $m^\star$ and spin degeneracy $g_s = 2$. Carrier transport in the semiconductor channel is assumed to be 2-D, which holds both for monolayer 2-D crystals and in FETs made of 3-D semiconductors, where transport occurs in a quasi-2-D electron/holes gas. The occupation of multiple 2-D subbands can then be treated as individual 2-D channels—we consider a single subband model.

The semiconductor channel of length L and width W is assumed to be connected to very low-resistance ohmic contacts at the source and drain, as shown in Fig. 4. The energy band diagram in Fig. 4 shows the potential barrier controlled by the voltage on the gate metal. Electrical charge neutrality requires $\sigma_m = qn_s$, where n_s is the mobile carrier sheet density at the top of the barrier in the energy band diagram along the length of the channel. The energy band diagram from the metal to the semiconductor requires $q\phi_B + qV - \Delta E_c + (E_{Fs} - E_c) = qV'_{gs}$. By suitable choice of materials, we assume that $q\phi_B = \Delta E_c$; if this is not the case, the difference can be absorbed in a shift of threshold voltage. When no drain voltage is applied, carriers in the semiconductor are in thermal equilibrium with the source and drain reservoirs, which for a parabolic 2-D bandstructure means $qn_s = C_{sc} V_{th} \ln(1+\exp[(E_{Fs}-E_c)/kT])$ or $E_{Fs} - E_c = kT \ln(\exp[qn_s/C_{sc}V_{th}] - 1)$, where $C_{sc} = q^2 g_s g_v m^\star/2\pi\hbar^2$ is the density of states semiconductor capacitance and the thermal voltage $V_{th} = kT/q$. From the energy band diagram in Fig. 4, the relation between the applied gate voltage V'_{gs} and the voltage drop V across the piezoelectric insulator is $qV'_{gs} = qV + (E_{Fs} - E_C)$. Here, $(E_{Fs} - E_c)/q = (V'_{gs} - V) = \psi_s$ is the surface potential. Using the carrier density expression and (2), the gate-induced charge qn_s in the semiconductor channel is self-consistently calculated. Finally, using this new dependence of charge on the voltages and the piezoelectric coefficients, the current–voltage characteristics of the piezo-FET are obtained from the ballistic transport model [22] (see Section III of the supplementary material for details) incorporating the quantum contact resistances of 0.026 k$\Omega \cdot \mu$m [23] at the source and the drain ends.

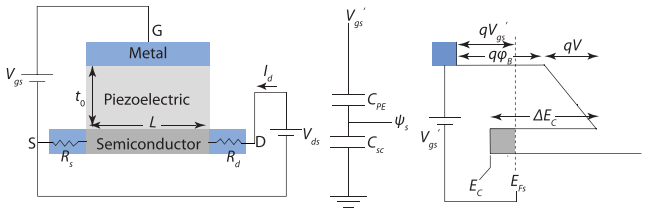

FIGURE 4. Schematic cross section of a transistor (piezo-FET) with a piezoelectric gate barrier, semiconductor channel, such as Si, GaN, or 2-D material, MoS_2, and source and drain ohmic contacts. The gate capacitance circuit is a series combination of the piezoelectric capacitance C_{PE} and the semiconductor capacitance C_{sc}. Here, intrinsic gate voltage $V'_{gs} = V_{gs} - I_d R_s$ and intrinsic drain voltage $V'_{ds} = V_{ds} - I_d(R_s + R_d)$, where R_s and R_d are the source and drain contact resistances. The energy band diagram is shown for the metal–piezoelectric–semiconductor stack of the transistor. $\psi_s = V'_{gs} - V = (E_{Fs} - E_C)/q$ is the surface potential.

Fig. 5 shows the gate capacitance $C_g = d(qn_s)/dV'_{gs}$ and device characteristics (I–V) of a ballistic piezo-FET with a GaN channel ($m^\star = 0.2m_0$ and $g_v = 1$) [24]. Fig. 5(a) shows that a higher gate C_g is obtained in the piezo-FET (solid line), as compared with a FET with a passive gate (dashed line). The higher C_g is due to the negative capacitance resulting from piezoelectric charge amplification: $C_{PE}C_{sc}/(C_{PE} + C_{sc}) > C_0 C_{sc}/(C_0 + C_{sc})$ when $C_{PE} < 0$. Fig. 5(b) shows the solution of the piezoelectric and the semiconductor charge equations graphically, following the load-line approach [25]. The blue lines depict charge in the semiconductor channel, and the green, black, and red lines depict the charge drawn into the metal from the battery. They must be equal to maintain global charge neutrality, meaning that the locus of intersections is the operating points of the device. The green line is the charge on the metal for a traditional passive-gate dielectric, and the red/black lines for a piezoelectric gate. When the transistor is ON ($V'_{gs} \sim 0.3$ V), an increase in the charge at point a_2 in Fig. 5(b) is seen for the piezoelectric compared with point a_1 for a passive dielectric. This increased charge boosts the ON-current as shown in Fig. 5(c), consequently improving the I_{ON}/I_{OFF} ratio. This sort of piezoelectric amplification is an interesting method to boost the ON-current in any transistor. Since much of the high-performance characteristics, such as gain and cutoff frequencies, depend on I_{ON}, corresponding boosts can be expected in these parameters. This may be especially useful for boosting the current in FETs made of relatively low-mobility channel materials. Note, however, in Fig. 5(c) that this device still has an SS of 60 mV/decade. This is because the negative capacitance regime is only accessible for charge densities $\geq 1.5 \times 10^{13}$ cm^{-2}: at this

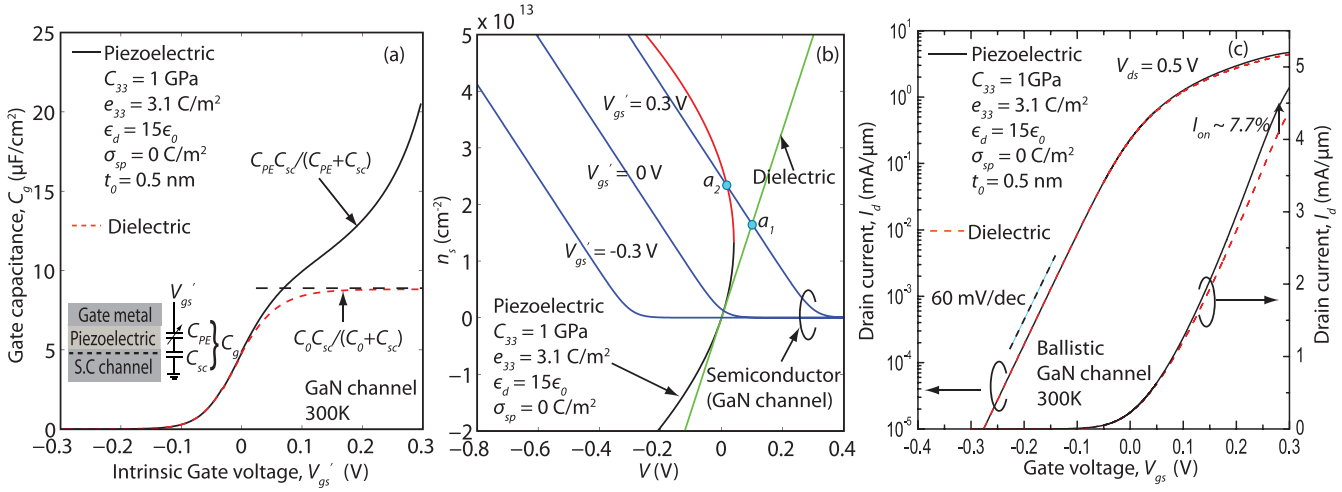

FIGURE 5. **(a) Gate capacitance C_G versus intrinsic gate voltage $V_{\mathbf{gs}}'$ for transistors with piezoelectric (solid line) and dielectric (dashed line) insulators. (b) Graphical load line analysis to obtain sheet carrier density n_s for different values of $V_{\mathbf{gs}}'$. Blue curves: semiconductor charge for different values of $V_{\mathbf{gs}}'$. Green curve: metal charge in the case of a passive dielectric. Red (black) curve: metal charge in the negative (positive) capacitance regimes of the piezoelectric capacitor. Intersections a_1 and a_2 of the above characteristics define the operating points of the system. (c) Transfer curve depicts the drain current I_d versus external gate voltage $V_{\mathbf{gs}}$ at drain voltage $V_{\mathbf{ds}}$ = 0.5 V for GaN transistors with piezoelectric (solid line) and dielectric barriers (dashed line).**

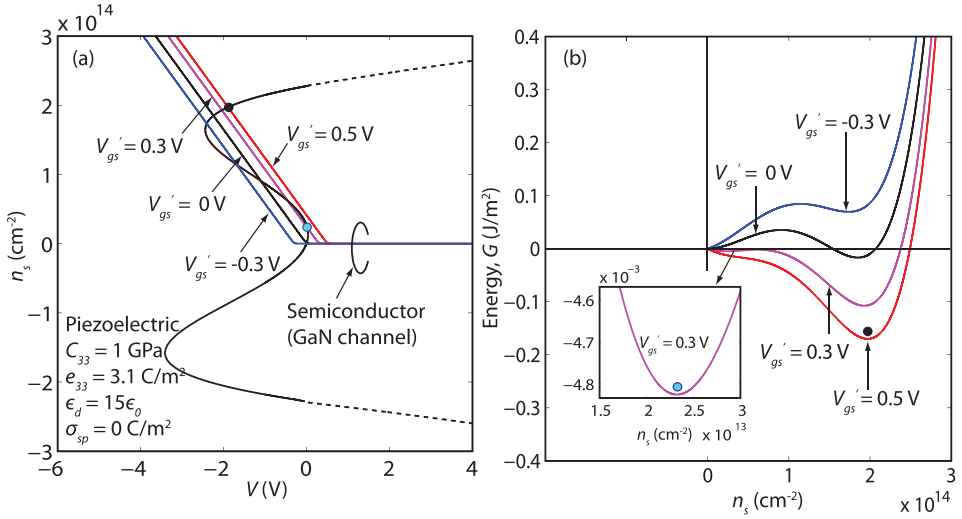

FIGURE 6. **(a) Load line analysis showing multiple intersections of the piezoelectric and semiconductor characteristics for different values of $V_{\mathbf{gs}}'$. (b) Free-energy landscape of the piezoelectric–semiconductor stack at various values of $V_{\mathbf{gs}}'$. Blue and black dots: stable operating points.**

high level of charge, the transistor is in its ON-state, rather than in the subthreshold regime. Here, we point out that the ON-current boost is 7.7% [Fig. 5(c)], while the increment in gate capacitance C_g is >100% [Fig. 5(a)]. This is due to the effect of source and drain contact resistances in the gate and drain terminal bias voltages of the transistor. Note that in Fig. 5(c), we plot the drain current I_d as a function of external gate voltage $V_{\rm gs}$ and drain voltage $V_{\rm ds}$ incorporating source and drain contact resistances $R_s = R_d = R_c$, while in Fig. 5(a), we plot the gate capacitance C_g as a function of intrinsic gate voltage $V_{\rm gs}' = V_{\rm gs} - I_d R_s$.

Because the charge–voltage characteristic of the piezoelectric capacitor is highly nonlinear, it can have multiple intersections with the semiconductor load line. Cherry [26] developed a systematic procedure to understand such nonlinear systems based on the Euler–Lagrange equations of motion (see Section V of the supplementary material for details). For this analysis, we define a free-energy G in units of J/m^2 for the piezoelectric–semiconductor stack: $G(\sigma_m, V_{\rm gs}') = \int V d\sigma_m + \int \psi_s d\sigma_m - \sigma_m V_{\rm gs}'$, where V is the voltage drop across the gate insulator and ψ_s is the surface potential. Minima in this free-energy landscape correspond to stable charge solutions of the nonlinear system. If there are multiple minima, the actual solution $\sigma_m = qn_s$ depends on the previous state or the history of the system.

For example, Fig. 6(a) shows the load lines, and the corresponding evolution of the free-energy landscape for different values of $V_{\rm gs}'$ is shown in Fig. 6(b). The shape of

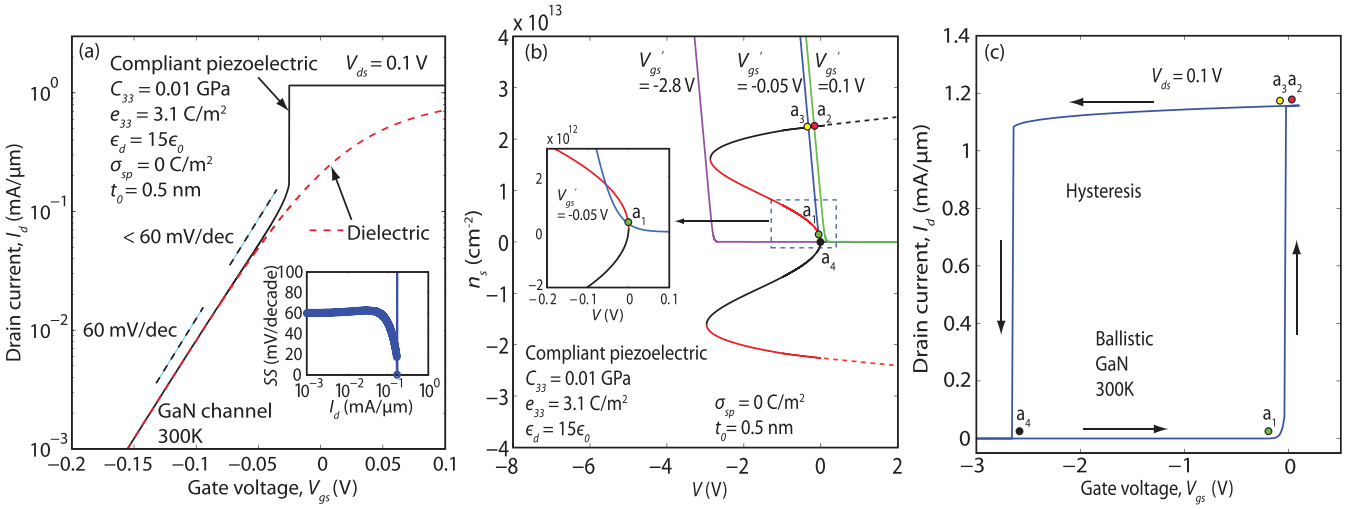

FIGURE 7. (a) I_d versus V_{gs} curves at V_{ds} = 0.1 V for a GaN channel piezo-FET with a compliant piezoelectric with C_{33} = 0.01 GPa. A boost in the ON-current and sub-60-mV/decade SS (inset) are obtained as compared with a passive-gate dielectric. (b) Load line characteristics to explain the hysteresis with gate bias voltages V_{gs}'. (c) Calculated hysteresis in the transfer curve I_d versus V_{gs} for forward and reverse sweeps is shown for a GaN channel piezo-FET.

the energy landscape changes with the applied voltage. There are two energy minima in the range $-0.35 < V_{gs}' < 0.35$ V, and a single minimum otherwise. Let us assume that there is no charge to begin with on the capacitor, and ramp the gate from a negative to a positive voltage. Until around $V_{gs}' = 0.35$ V, the system remains in the minimum, corresponding to the lower charge state ($\sim 2.3 \times 10^{13}$/cm^2) shown in Fig. 6(a) (blue dot) and (b) (inset). But when $V_{gs}' > 0.35$ V, it is driven into the higher charge state shown as a black dot. Thus, provided $V_{gs}' < 0.35$ V, the transistor displays no hysteresis in its I–V characteristics.

It is pertinent here to note an important difference in the nature of negative capacitance of the piezoelectric and the ferroelectric insulators. The ferroelectric capacitor possesses negative capacitance at zero charge, whereas the capacitance of the piezoelectric capacitor is positive at zero charge. This property of the ferroelectric capacitor is exploited in achieving SS < 60 mV/decade, since the semiconductor load line can intersect the negative capacitance regime of the ferroelectric characteristic at the very low charge densities corresponding to subthreshold operation of the transistor. Can a similar negative capacitance be obtained in the SS regime ($V_{gs}' < 0$ V) using piezoelectric gates? We explore this by tuning the piezoelectric material properties.

We find that if a lower stiffness, highly compliant piezoelectric barrier with $C_{33} \sim 0.01$ GPa is used, it can enable the reduction of the SS below 60 mV/decade and also boost the ON-current. This is shown in Fig. 7(a). Here, negative capacitance is accessed in the subthreshold region, shown by the operating point a_1, in the load line characteristics at $V_{gs}' = -0.05$ V, shown in Fig. 7(b). The ON-state operation of this transistor corresponds to the higher charge state determined by the operating point a_2 in the load line characteristics at $V_{gs}' = 0.1$ V. However, this also results in hysteresis in the transistor characteristics with V_{gs}' sweep, as shown in the I_d–V_{gs} characteristics in Fig. 7(c), which is calculated using the Lagrangian method. Hysteresis is undesirable in purely switching applications, but desirable for memory. Furthermore, the strain in the higher charge states a_2 and a_3 is very close to 100%, which is not feasible in realistic materials. If suitable, new piezoelectric materials with ultralow C_{33} and high e_{33} could be developed (see Section IV of the supplementary material for various piezoelectrics with different values of C_{33} and e_{33}), and sub-60-mV/decade switching can be achieved with hysteresis with a suitable choice of semiconductors. Investigation of other transistor designs incorporating the piezoelectric barrier, such as the quantum metal transistor [27], to eliminate the hysteresis and reduce strain could be the focus of future work.

In this paper, we have considered a piezoelectric barrier with thickness $t_0 = 0.5$ nm. When using a piezoelectric barrier of such low thickness, it is important to consider the problem of gate leakage due to tunneling current. Note, however, that since this proposed piezoelectric gate transistor is for low-power switching applications, the operating voltage is <0.3 V. This will result in a lower leakage current than in the conventional MOS devices that operate at higher supply voltages. Therefore, our proposal using ~0.5 nm piezoelectric barrier is probably feasible. Another way to mitigate the leakage current problem is to use a relatively thicker barrier. A thicker barrier comes with the advantage of reduced gate leakage current, but at the cost of a relatively higher voltage to obtain the same charge as the thinner barrier (see Section II of the supplementary material for a detailed discussion on the effect of various piezoelectric barrier thicknesses on the properties of the piezoelectric capacitor).

Finally, we discuss the possibility of the mechanical switching frequency of the piezoelectric barrier, limiting the speed of the transistor. The mechanical switching frequency

due to elastic strain in the piezoelectric barrier is defined as $f_{\text{switch}} = v/t_0 \approx 10^3/(0.5 \times 10^{-9}) = 2$ THz, where v is the acoustic wave velocity in the piezoelectric material $\sim 10^3$ m/s [28], and $t_0 = 0.5$ nm. Note that f_{switch} is high, and therefore will not be an impediment to developing high-speed transistors using a piezoelectric barrier.

We also emphasize that we have assumed linear piezoelectric parameters in this paper to keep the model simple, and yet capture the new physics. The nonlinear material response needs to be explored in future.

IV. CONCLUSION

To conclude, the behavior of transistor switches using active piezoelectric gate barriers was explored. Because of electrostriction and piezoelectricity, negative capacitance is predicted to appear in a piezoelectric capacitor. Using this negative capacitance and a ballistic transport model, we predict that compliant piezoelectric barriers can boost the gate capacitance and increase the ON-currents of transistors. In addition, steep switching with sub-60-mV/decade SS is predicted when the negative capacitance of the piezoelectric barrier is accessed in the OFF-state operation of the transistor, and this steep behavior is predicted to be assisted by hysteresis based on the Lagrangian method of stability of the transistor system.

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