GaN-on-GaN p-n power diodes with 3.48 kV and 0.95 mΩ·cm^2: a record high figure-of-merit of 12.8 GW/cm^2

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Abstract

We report GaN p-n diodes on free-standing GaN substrates: a record high Baliga's figure-of-merit (V_B^2/R_{on}) of 12.8 GW/cm^2 is achieved with a 32 μm drift layer and a diode diameter of 107 μm exhibiting a BV > 3.4 kV and a R_{on} < 1 mΩ·cm^2. The leakage current density is low: 10^{-3} - 10^{-4} A/cm^2 at 3 kV. A record low ideality factor of 1.1-1.3 is signature of high GaN quality. These are among the best-reported GaN p-n diodes.

Introduction

GaN based devices have marked excellent records for high-frequency [1,2], high-power [3-8] and high-efficiency [9,10] applications. Most GaN-based power devices have been fabricated on GaN-on-Si or sapphire for low cost or GaN-on-SiC. However, the large lattice mismatch between GaN and the substrate leads to high threading dislocation densities (TDD) over 10^8 -10^9 cm^{-2}, causing significant leakage currents in vertical devices and often an ideality factor in p-n diodes significantly higher than unity. To this end, GaN-on-GaN vertical power devices hold much promise since the bulk GaN substrates today are reported to have TDDs between 10^2 -10^6 cm^{-2}.

Experiments

The GaN p-n junction epi-structures were grown by metalorganic vapor phase epitaxy (MOVPE) on free-standing GaN substrates with a TDD of ~ 2×10^6 cm^{-2}, which are from Hitachi Metals Inc. using the VAS method [11]. As shown in **Fig.1**, three device layer structures have been grown with a varying n-GaN drift layer thickness of 20, 25 and 32 μm while keeping the rest of the layers the same. For the 20 μm epi-design, the drift layer doping concentration was kept constant, which is confirmed by the capacitance-voltage (C-V) measurement on these power diodes; the net N_D-N_A concentration extracted from CV measurements showed a constant value of 5×10^{15} cm^{-3} in the top 10 μm. For the 25 and 32 μm epi-designs, the top 6 μm of the n-GaN drift layer was grown to have the lowest doping concentration: a net N_D-N_A concentration of ~1×10^{15} cm^{-3} was extracted from CV measurements while a Si concentration of 2.5×10^{15} cm^{-3} was measured by secondary ion mass spectrometry (SIMS) on a similar epi-wafer. For the 2nd n-GaN drift layer, a net N_D-N_A concentration of 2-3$\times10^{15}$ cm^{-3} was extracted from CV measurements in both the 25 and 32 μm power diodes.

The power diodes were fabricated by dry-etching first to define the diode mesa. Circular Pd-based anodes were formed by a liftoff process on the p$^+$-GaN cap layer. Then a spinning-on-glass (SOG) insulating layer was spun on the wafer, followed by curing in furnace. Contact holes were subsequently formed and Ti/Au was deposited to fabricate the FP structures. Finally, a Ti-based cathode was formed on the backside of the GaN substrate. Five different device processes are compared in terms of the effectiveness of electric field management: no field-plate (NFP), spin-on-glass passivated with no field-plate (SOG-NFP), long field-plate (LFP), beveled-mesa with and without FP.

Results and Discussion

In **Fig. 2** the representative cross-section of four completed diode types are shown: no field-plate (NFP) without SOG, no field-plate but with SOG passivation (SOG-NFP), steep-mesa and beveled-mesa with a long field plate (LFP and beveled-LFP) that extends 20 μm beyond the mesa bottom edge (beveled mesa with no field-plate is not shown). *The diode size is defined by the bottom mesa diameter, ranging from 70 to 707 μm*.

In **Fig. 3**, the representative forward bias I-V characteristics of these power diodes are plotted, showing a current swing near 14 orders of magnitude and an leakage current level <10^{-9} A/cm^2 (limited by the measurement instrumentation). Negligible difference is seen in the forward bias I-Vs of the five device types. A differential specific on-resistance (R_{on}) of about 1 mΩ·cm^2 is extracted at high current densities (> 1 kA/cm^2). The current density and R_{on} are normalized using the bottom mesa area since, according to our TCAD device simulations, current spreading at high-current densities is small (< 5 μm). The current flow at high densities therefore was primarily restricted by the device mesa isolation. The diode ideality factor (n) of ~2 is found in a bias window of 2 – 2.5 V then n decreases to ~1.3 near 2.8 V; the sharp increase in n after diodes turns on ~3 V is

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due to diode series resistances. In some of the diodes, n reaches 1.1-1.2 (not shown). The near-unity ideality factor is remarkable since it signifies the superb quality of GaN grown on GaN substrates in these p-n diodes.

Fig. 4 shows the representative reverse bias *I-V* characteristics of various diode types fabricated on the 25-μm epi-wafer. The device *BV* is the lowest in diodes with no field-plate (~1-1.4 kV), as expected; *BV* increases moderately in diodes with SOG passivation but no field-plate (~1.6 kV), improves further in diodes with long field-plate and steep mesa (~3.0 kV) and reaches > 3.2 kV in diodes with long field-plates and beveled mesa. It is interesting to note that employing both long field-plate and beveled mesa dramatically improves the uniformity of device performance, especially in the large area diodes (> 300 μm); it is extraordinary that diodes with a diameter of 707 μm (bottom mesa size) have reached a *BV* > 3 kV.

Fig. 5 shows avalanche breakdown capability in these GaN p-n junction diodes and the temperature dependent forward bias *I-V* characteristics. With increasing temperature, both turn-on voltage and the minimum ideality factor window move to a lower bias due to enhanced thermal emission of electrons and holes (the ideal diode current components: drift-diffusion). Increase of *BV* at elevated temperatures is the signature of avalanche breakdown in these power diodes.

The benchmark plot is shown in **Fig. 6**, demonstrating a record Baliga's figure of merit of > 12 GW/cm^2 obtained in the 32 μm epi-design. Also shown is that the p-n power diode *BV* increases with the increasing n-GaN drift-layer thickness while R_{on} remains nearly the same ~1.0 mΩ·cm^2. If the minority carrier lifetime is short, a p-n diode can be assumed to operate like a unipolar device thus R_{on} is dominated by the n-GaN drift region. Assuming a carrier concentration of 5×10^{15} cm^{-3} and a mobility of 2000 cm^2/Vs, the specific resistance of a 20 μm n-GaN drift layer is calculated to be ~1.25 mΩ·cm^2. The observed record low R_{on} might arise from other mechanisms including high level injection, photon recycling effects [12-15], which warrants further investigation.

Conclusions

We report GaN p-n junction diodes on free-standing GaN substrates with record performance: a low specific on-resistance (R_{on}) of ~ 1 mΩ·cm^2 and high breakdown voltages (*BV*) ranging from 2.3 to 3.5 kV for drift layer thicknesses ranging from 20 to 32 μm. The low R_{on} can be attributed to low contact resistances achieved on p-GaN and high quality n-GaN drift layers in these diodes. Five different device processes are compared in terms of the effectiveness of electric field management: no field-plate (NFP), spin-on-glass passivated with no field-plate (SOG-NFP), long field-plate (LFP), beveled-mesa with and without FP. It is observed that LFP alone leads to more significant improvement in *BV* in comparison to beveled-mesa alone; that when both LFP and beveled-mesa are employed in the same device, *BVs* in large area diodes (diameter > 300 μm) increase dramatically.

Acknowledgement

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References

(1) Y. Yue, Z. Hu, J. Guo, B. S. Rodriguez, G. Li, R. Wang, F. Faria, T. Fang, B. Song, X. Gao, S. Guo, T. Kosel, G. Snider, P. Fay, D. Jena, and H. Xing, "InAlN/AlN/GaN HEMTs with regrown ohmic contacts and f_T of 370 GHz", *IEEE EDL,* Vol. 33, No. 7, pp. 988-990, July 2012

(2) K. Shinohara, D. Regan, A. Corrion, D. Brown, Y. Tang, J. Wong, G. Candia, A. Schmitz, H. Fung, S. Kim, and M. Micovic, "Self-aligned-gate GaN-HEMTs with heavily-doped n$^+$-GaN ohmic contacts to 2DEG", *IEEE IEDM,* pp. 681-684, December 2013

(3) I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Bour, T. Prunty, and D. Disney, "3.7 kV vertical GaN pn diodes", *IEEE EDL,* Vol. 35, No. 2, pp. 247-249, February 2014

(4) K. Nomoto, Y. Hatakeyama, H. Katayose, N. Kaneda, T. Mishima, and T. Nakamura, "Over 1.0 kV GaN p-n junction diodes on free-standing GaN substrates", *Phys. Status Solidi A* 208, No. 7, pp. 1535-1537, 2011

(5) Y. Hatakeyama, K. Nomoto, N. Kaneda, T. Kawano, T. Mishima, T. Nakamura, "Over 3.0 GW/cm2 figure-of-merit GaN p-n junction diodes on free-standing GaN substrates", *IEEE EDL,* Vol. 32, No. 12, pp. 1674-1676, December 2011

(6) Y. Hatakeyama, K. Nomoto, A. Terano, N. Kaneda, T. Tsuchiya, T. Mishima, and T. Nakamura, "High-breakdown-voltage and low-specific-on-resistance GaN p-n junction diodes on free-standing GaN sunstrates fabricated through low-damage field-plate process", *JJAP*, 52, pp. 028007-1-3, 2013

(7) Y. Yoshizumi, S. Hashimoto, T. Tanabe, and M. Kiyama, "High-breakdown voltage pn-junction diodes on GaN substrates", *Journal of Crystal Growth,* 298, pp. 875-878, January 2007

(8) M. Zhu, B. Song, M. Qi, Z. Hu, K. Nomoto, X. Yan, Y. Cao, W. Johnson, E. Kohn, D. Jena and H. G. Xing, "1.9-kV AlGaN/GaN lateral Schottky barrier diodes on silicon ", *IEEE Electron Dev. Lett.*, Vol. 36, No. 4, April 2015

(9) Y. Wu, M. J. Mitos, M. L. Moore, and S. Heikman, "A 97.8% efficient GaN HEMT boost converter with 300-W output power at 1 MHz", *IEEE EDL,* Vol. 29, No. 8, pp. 824-826, August 2008

(10) T. Morita, S. Tamura, Y. Anda, M. Ishida, Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, "99.3% efficiency of three-phase inverter for motor drive using GaN-based gate injection transistors", *IEEE IEDM*, pp. 481-484, December 2011

(11) Y. Oshima, T. Eri, M. Shibata, H. Sunakawa, K. Kobayoshi, T. Ichihashi, and A. Usui, "Preparation of freestanding GaN wafers by hybride vapor phase epitaxy with volid-assisted separation", *JJAP*, Vol. 42, Pt. 2, No. 1A/B, pp. L1-L3, January 2003

(12) K. Mochizuki,K. Nomoto, Y. Hatakeyama, H. Katayose, T. Mishima, N. Kaneda, T. Tsuchiya, A. Terano, T. Ishigaki, T. Tsuchiya, R. Tshuchiya, and T. Nakamura, "Photon-recycling GaN p-n diodes demonstrating temperature-independent, extremely low on-resistance", *IEEE IEDM*, pp. 591-594, December 2011

(13) K. Mochizuki, T. Mishima, A. Terano, N. Kaneda, T. Ishigaki, and T. Tsuchiya, "Numerical analysis of forward-current/voltage characteristics of vertical GaN Schottky-barrier diodes and p-n diodes on free-standing GaN substrates", *IEEE TED*, Vol. 58, No. 7, pp. 1979-1985, July 2011

(14) K. Mochizuki, T. Mishima, K. Nomoto, A. Terano, and T. Nakamura, "Optical-thermo-transition model of reduction in on-resistance of small GaN p-n diodes", *JJAP*, Vol. 52, pp. 08JN10-1-4, May 2013

(15) K. Mochizuki, T. Mishima, Y. Ishida, Y. Hatakeyama, K. Nomoto, N. Kaneda, T. Tsuchiya, A. Terano, T. Tsuchiya, H. Uchiyama, S. Tanaka, and T. Nakamura, "Determination of lateral extension of extrinsic photon recycling in p-GaN by using transmission-line-model patterns formed with GaN p-n junction epitaxial layers", *JJAP*, Vol. 52, pp. 08JN22-1-4, May 2013

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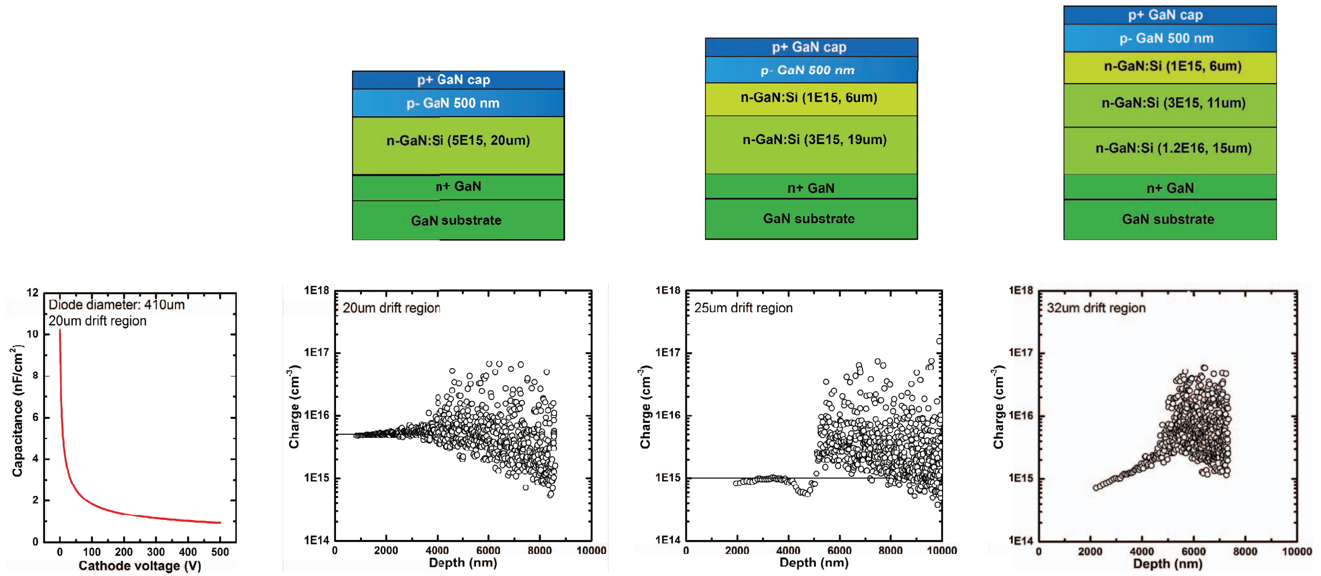

Fig. 1 (upper row) MOVPE p-n junction epi-structures on free-standing GaN substrates with a varying n-GaN drift layer thickness: 20, 25 and 32 µm, while keeping all the rest of the layers the same. The carrier concentrations indicated therein are determined by C-V measurements at 100 kHz except the very bottom n-GaN layer in the 32 µm epi-design. (lower row) Measured capacitance versus cathode voltage up to 500 V for GaN-on-GaN p-n power diodes, extracted charge concentration (cm^{-3}) depth profiles in the drift layer for the corresponding epi designs.

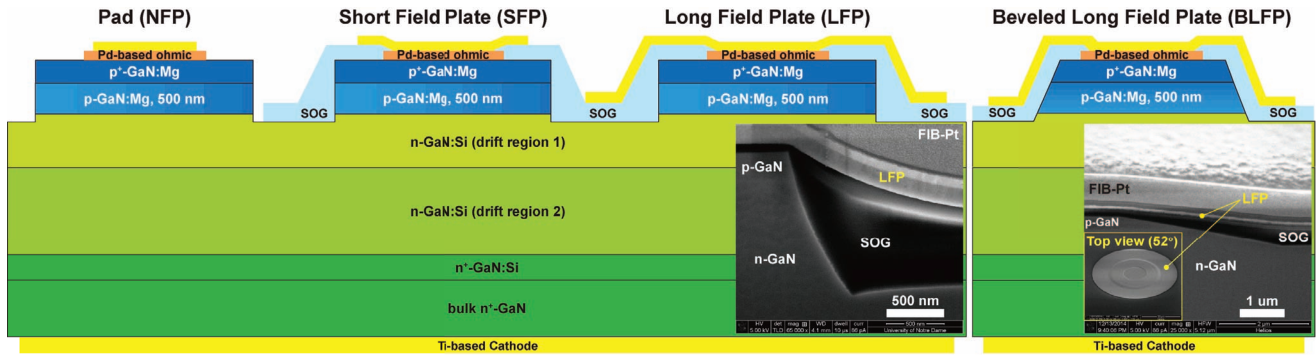

Fig. 2 Schematic cross-sections of 4 device types arising from processing variations. From left to right, with no field-plate (NFP), with SOG passivation and no field-plate (SOG-NFP), steep mesa with a long-field plate (LFP), and beveled mesa with a long-field plate (beveled-LFP). Also included are the scanning electron microscopy (SEM) cross-section images showing the steep and beveled mesa sidewalls in fabricated devices.

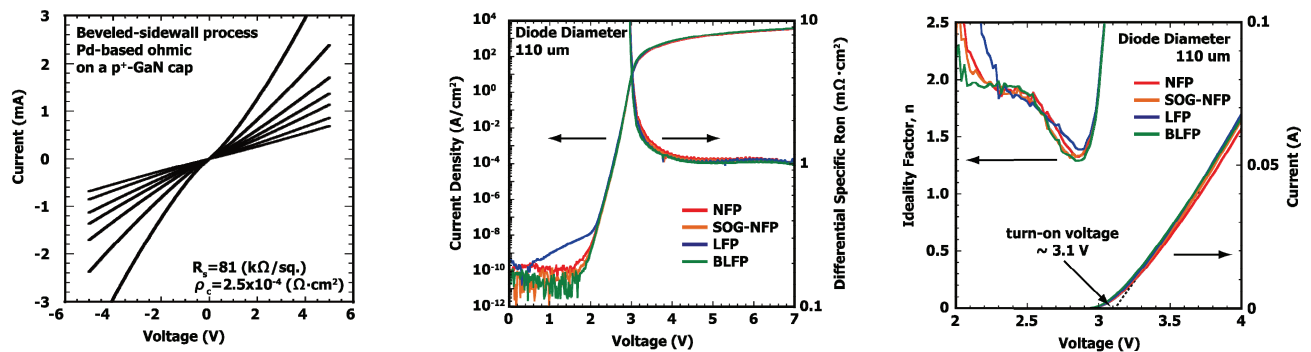

Fig. 3 (left) Representative TLM *I-V* characteristics of ohmic contacts on p-GaN, a low contact resistance of 2.5×10^{-4} Ω·cm² is extracted with a p-GaN sheet resistance of 81 kΩ/sq.. (middle) forward bias *I-V*s and the specific on-resistance in a semi-log scale and (right) ideality factor and forward bias *I-V* characteristics in a linear scale, for NFP, SOG-NFP, LFP, BLFP (beveled-LFP) power diodes fabricated on the 25 µm epi-wafer. Low differential specific R_{on} of 1 mΩ·cm² and an ideality factor of ~1.3 are achieved simultaneously. The differences in the forward *I-V* characteristics are negligible among all the device types.

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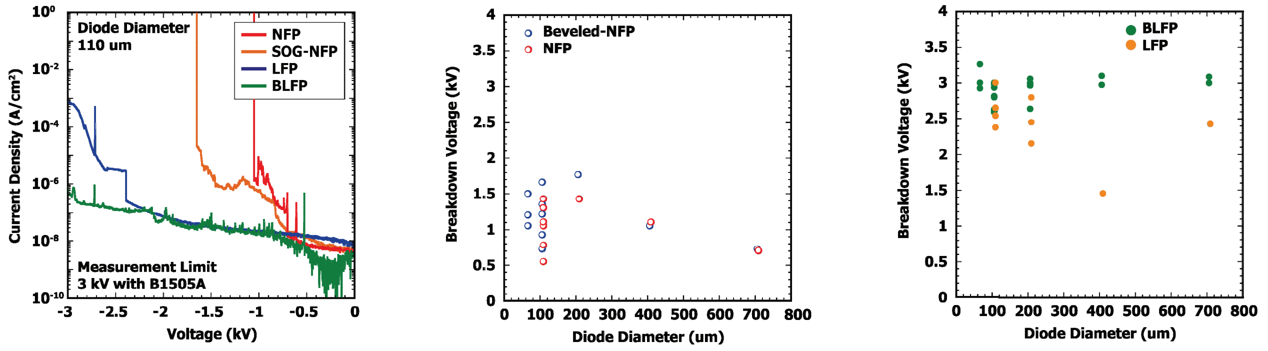

Fig. 4 Reverse bias *I-V* characteristics of NFP, SOG-NFP, LFP, BLFP (beveled-LFP) GaN p-n power diodes fabricated on the 25 µm epi-wafer. With the employment of field plate, the breakdown voltage increases significantly from ~1 kV to ~3 kV for the devices with steep sidewall. Combining the field plate and the beveled mesa sidewall, the device breakdown voltage increases further to >3.2 kV. Interestingly, the breakdown voltage increases dramatically in the large area diodes employing the beveled-LFP process.

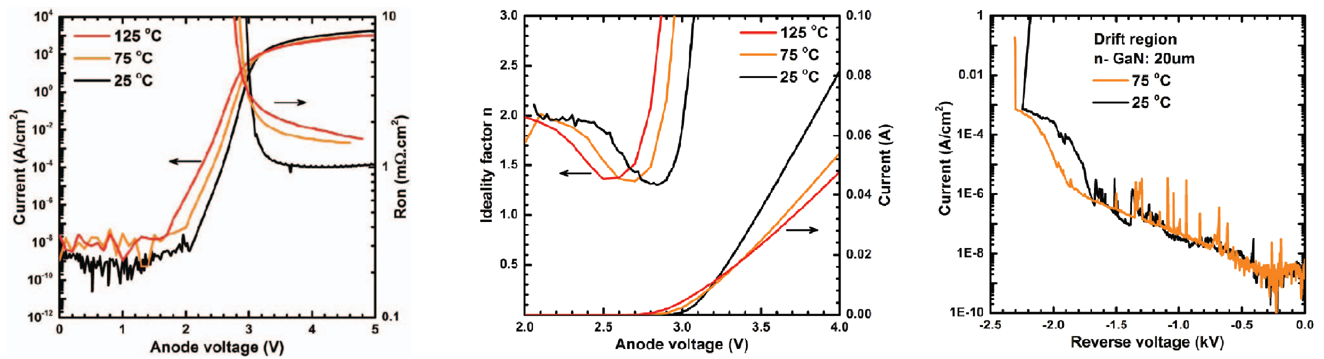

Fig. 5 Temperature dependent forward *I-V*s, specific on-resistance, ideality factor and reverse bias *I-V* characteristics, measured on beveled-LFP devices fabricated on the 20 µm epi-wafer. The increase in *BV* at elevated temperatures signifies the avalanche breakdown capability in these GaN p-n junction diodes. The temperature dependent measurements were not carried out on the 25 and 32 µm diodes due to the measurement instrumentation limitation.

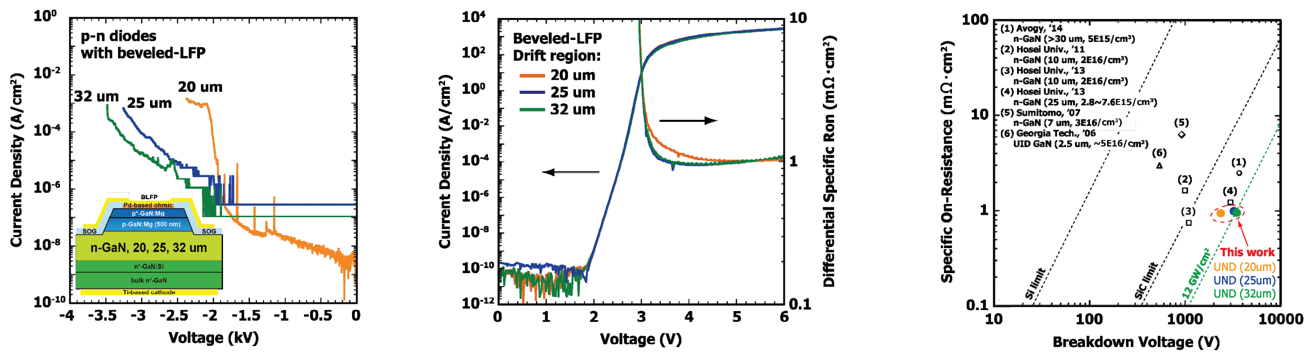

Fig. 6 (left) Reverse and (middle) forward bias *I-V* characteristics of representative p-n diodes employing the beveled-LFP process flow. (right) Baliga's figure-of-merit benchmark plot of reported vertical GaN-on-GaN p-n diodes. The diode current and R_{on} are normalized with respect to the mesa area determined by the bottom diameter of the mesa. The specific on-resistance for all devices (this work and from the literature) is compared without considering current spreading. For the results from Hosei Univ., data have been updated since the diode area used in the original reports is the electrode size, which is smaller than the mesa size.

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