Steep subthreshold swing tunnel FETs: GaN/InN/GaN and transition metal dichalcogenide channels

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Abstract

As the understanding of tunnel field-effect transistors (TFET) advances, new approaches are emerging to lower off-currents, lower defect density in tunnel junctions, and to increase the highest current at which the subthreshold swing of 60 mV/decade (I_{60}) appears. III-N heterojunctions and transition-metal-dichalcogenide (TMD) materials are forcing some new thinking in junction design and doping.

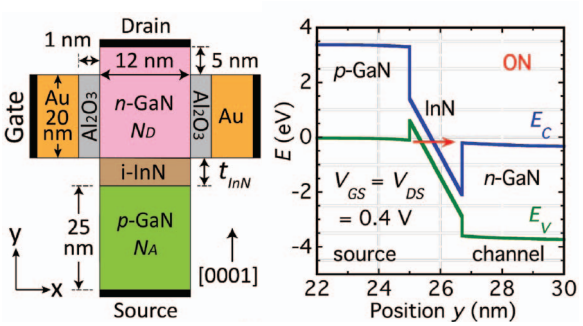
Introduction

TFETs continue to be a leading option for low voltage beyond-CMOS transistors [1, 2]. However, the preferred channel material, gate stack, and geometry for the TFET is still undecided. Among more than 25 laboratories working on TFETs worldwide there is little overlap in materials or approaches and this will likely continue until materials and gate stacks advance to reveal the viable options. This paper discusses two promising new directions for tunnel junction formation that alter the subthreshold and off-state leakage characteristics of the TFET. These characteristics can be dominated by defects that mediate leakage currents through and around the junction and degrade subthreshold swing. Reduction of defect-assisted transport processes stands as a critical challenge in the development of TFETs [3].

GaN/InN/GaN TFET

The spontaneous and piezoelectric polarization in *p*-GaN/InN/*n*-GaN tunnel junctions allows the formation of peak electric fields for tunneling of ~20 MV/cm [4, 5], 5× higher than can be obtained using heavy doping in group IV and III-V tunnel junctions [6]. Polarization engineering of graded layers enables high carrier concentrations to be obtained without high impurity concentrations [7]. Figure 1 shows a double-gate III-N heterojunction TFET and its corresponding energy band diagram. The narrow band gap of InN (0.7 eV) promotes interband tunneling and the wide band gap of GaN (3.2 eV) suppresses off-current. The relatively large density-of-states masses ($m_E = 0.2$, $m_H = 1.5$) in GaN are effective in suppressing quantization and favors scaling.

Figure 2 shows simulated transfer characteristics for the GaN/InN/GaN double-gate TFET and dependences on the fin thickness L_D and the drain doping N_D. The drain current I_D per unit width W has an optimum L_D of 10 to 20 nm, see inset of Fig. 2(a). For thinner fin widths, the current falls off due to a loss of current cross section. For widths exceeding 20 nm, gate electrostatic control is degraded resulting in lower current. The dependence of current on channel doping N_D is shown in Fig. 2(b) for a fin thickness of 12 nm. Tunnel current is largely insensitive to doping until channel doping exceeds 10^{18} cm^{-3}; see inset of Fig. 2(b). The current decreases above 10^{18} cm^{-3} due to increased channel density and reduced states available for tunneling.



(a) (b)

Fig. 1. GaN/InN/GaN double-gate fin TFET: (a) schematic and (b) computed energy band diagram in the on state.

The best gate control for the GaN/InN/GaN should be obtained in the nanowire geometry [8]. Shown in Fig. 3 are the transfer characteristics and common source characteristics for a nanowire TFET with a diameter of 18 nm. Current drive as high as 60 μA/μm is predicted using Synopsis TCAD.

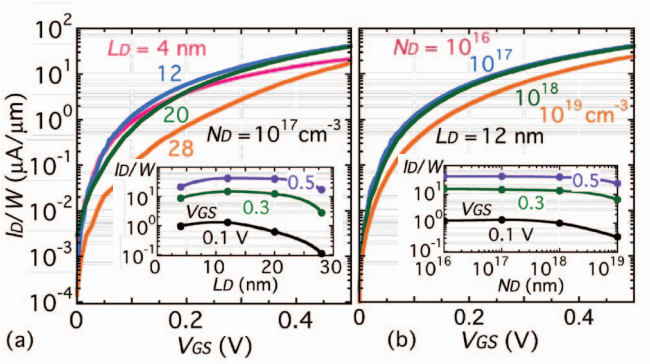


Fig. 2. Synopsis TCAD simulations of the GaN/InN/GaN TFET transfer characteristics: (a) drain doping N_D and (b) fin thickness dependence L_D for the transistor specified in Fig. 1 with gate length $L_G = 20$ nm, equivalent oxide thickness EOT = 0.43 nm, and $V_{DS} = 0.5$ V.

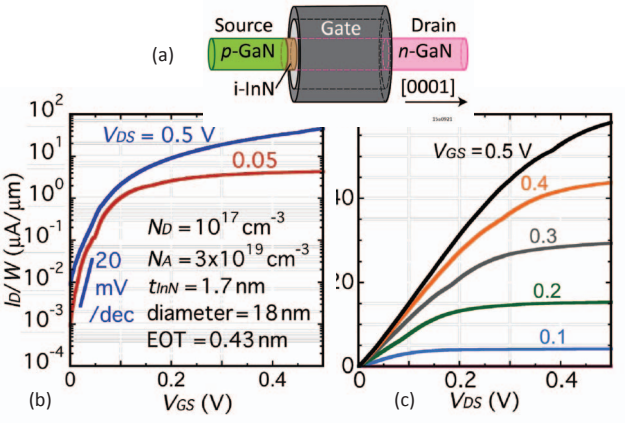


Fig. 3. (a) GaN/InN/GaN nanowire TFET. Synopsis simulations of (b) transfer characteristics and (c) common source characteristics.

Transition metal dichalcogenide TFETs

Two-dimensional (2D) crystals, including the transition metal dichalcogenides (TMDs) also possess properties that are well suited to TFETs [9, 10], including energy band gaps in the range of interest for scaled, low-power devices (0.8−1.2 eV), fully-terminated surfaces, and atomically-thin bodies. Figures 4 and 5 show simulated transfer characteristics for TFETs based on two-dimensional (2D) channels like graphene and the TMDs. The simulated data are benchmarked against experimental characteristics for 14 nm Si FinFETs.

In TMDs electrostatic doping can be used to create internal electric fields higher than can be achieved by substitutional doping, as desired for high tunnel current. Shown in Fig. 6 is a schematic cross section and energy band diagram of a WSe_2 TFET. Schottky barriers arise at the contacts and while these are undesired, they factor into the transport. Electrostatic doping applied by the back gate (BG) is used to induce holes in the source. Ion doping with Cs^+ is used to induce electrons in the drain [11]. The cesium ion is moved into position by a separate field plate not shown here, but discussed later. With the doping set, the top gate is used to open a tunneling window between the source and the channel as indicated in the band diagrams.

Ion doping of TMDs

Electrostatic doping using Li^+ and ClO_4^- ions in polyethylene oxide (PEO) has been shown to induce electron and hole sheet densities exceeding 10^{14} cm^{-2} in graphene [12] and Cs^+ doping in the same polymer has been shown to induce carrier densities of approximately 2 x 10^{13} in $MoTe_2$ [11]. By applying a potential on a side-gate, an electric field in the PEO is established to drift the ions into place at the TMD surface. Depending on the polarity, the ion induces an electron or hole to form an electric double layer with charge separation of less than a nanometer.

Figure 7 shows how the ions are used to dope the WSe_2 channel and control the channel conductivity between *n* and *p*-type. The location of the ions is controlled by a field plate

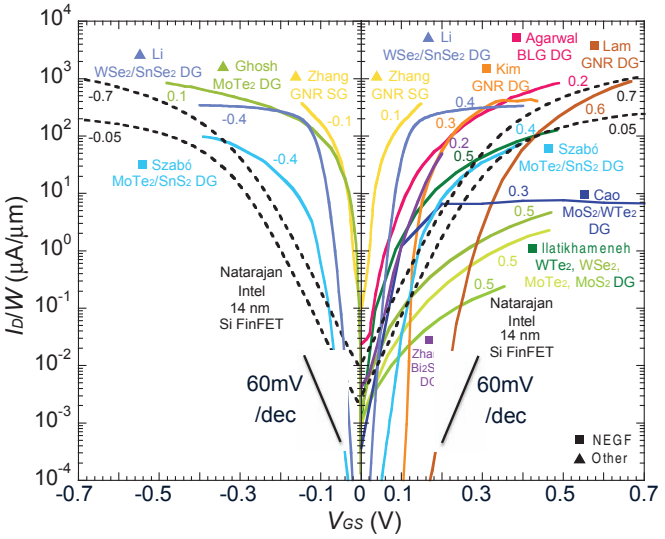


Fig. 4. Simulated TFET current-voltage characteristics for 2D crystal TFETs vs. 14 nm Si CMOS (dashed lines). References used here and in Fig. 2 are T. K. Agarwal et al. *IEEE EDL* 35, 1308-1310 (2014). Q. Zhang in K. Bernstein et al. *IEEE Proc.* 98, 2169-2184 (2010). J. Cao et al. *EUROSOI-ULIS*, 245-248 (2015). R. K. Ghosh, S, Mahapatra, *IEEE J. Electron Dev. Soc.* 1, 175-180 (2013). S. Kim et al. *Appl. Phys. Lett.* 104, 243113 (2014). K.-T. Lam et al. *IEEE Electron Dev. Lett.* 32, 431-433 (2011). M. Li et al. *IEEE J. Electron Dev. Soc.* 3, 200-207 (2015). Intel 14 nm, S. Natarajan et al. *2014 IEDM*, 3.7.1-4. Á. Szabó et al. *IEEE Electron Dev. Lett.* 36, 514-517 (2015). Q. Zhang et al. *IEEE Electron Dev. Lett.L* 35, 129-131 (2014).

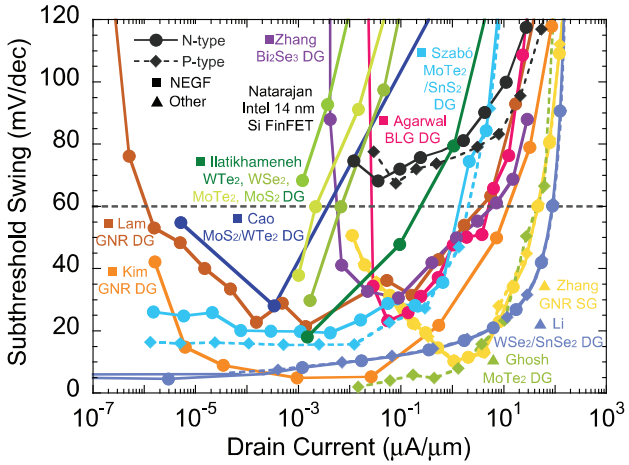
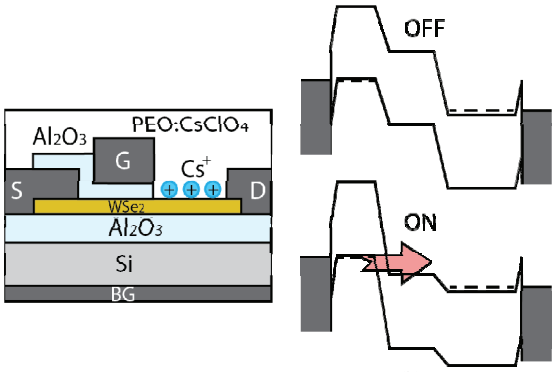


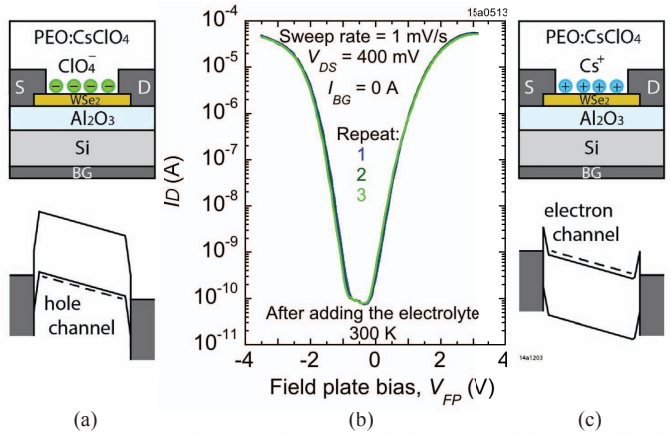
Fig. 5. Simulated subthreshold swing vs. current for 2D crystal TFETs of Fig. 4 vs. 14 nm Si CMOS indicaed by the black circles and diamonds.

(not shown), which in this case is located on the top surface of the approximately 1 μm thick PEO. Shown in Fig. 7(a) is the ion arrangement produced with the field plate biased negatively to drive ClO_4^- ions to the WSe_2 surface where they induce holes. The band diagram in Fig. 7(a) shows the formation of tunneling contacts at the Schottky barriers. The transfer characteristics of the WSe_2 FET shown in Fig. 7(b) illustrate the effectiveness of this doping with currents of 60 μA for a channel width of approximately 4 μm. The drain current measurements are made at a low drain bias, V_{DS} = 0.4 V, as needed for TFETs.



(a) (b)

Fig. 6. WSe_2 TFET with drain doping using polyethylene oxide (PEO) and cesium perchlorate ($CsClO_4$); (a) schematic cross section and (b) energy band diagrams in the OFF and ON states.



(a) (b) (c)

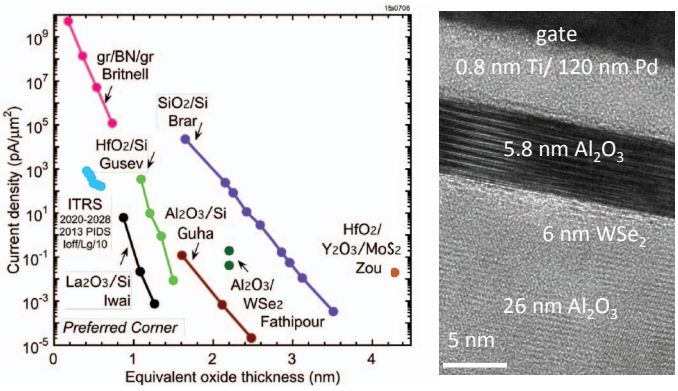
Fig. 7. Experimental demonstration of ion doping in a multilayer exfoliated WSe_2 FET (channel thickness 6.5 nm) using polyethylene oxide (PEO) as the ion conductor and cesium perchlorate, $CsClO_4$ as the ion source. The $CsClO_4$ dissociates into Cs^+ and ClO_4^- in the PEO. Wafer F4, device 17. The source and drain contacts are Ti(1 nm)/Pd(90 nm).

By sweeping the field-plate bias from negative to positive voltage, the ClO_4^- ions are removed from the WSe_2 surface and replaced by Cs^+ ions as shown in Fig. 7(c). The band diagram in Fig. 7(c) shows how the Cs^+ ions induce electrons and create a tunneling drain Schottky contact. Referring again to the transfer characteristic, it is seen that the ion doping produces approximately equal currents in both branches and achieves a current modulation of approximately 5 x 10^5.

Shown also in Fig. 7(b) are repeated scans of the field plate bias, demonstrating that the ions can be moved on and off the channel surface without chemical reactions and with reproducible characteristics. To establish the initial conditions prior to each field-plate bias sweep, all device contacts, source, drain, back-gate, and field plate, are set to zero for 5 minutes between scans. Measurements are made in a Cascade Microtech PLC50 vacuum probe station.

TMD gate stacks

Top-gated TMD FETs and TFETs require a uniform and pinhole-free gate dielectric, and subnanometer equivalent oxide thicknesses (EOT) to achieve sub-60-mV/decade



(a) (b)

Fig. 8. Measured gate current density at 1 V for selected high-k oxides on Si vs. best high-k oxides on transition metal dichalcogenides (TMD). The transmission electron micrograph at right is a 2.2 nm EOT Al_2O_3 on WSe_2 (5.8 nm physical thickness). References: B. Brar et al. *APL* 69, 2728-2730 (1996). L. Britnell et al. *Nano Lett.*12, 1707-1710 (2012). S. Fathipour et al. Dev. Res. Conf. 213-214 (2015). H. Iwai et al. *IEDM*, 625-628 (2002). E. P. Gusev et al. *IEDM, 20.1.1-4* (2001). X. Zou et al. *Adv. Mat.* 26, 6255-6261 (2014). Guha, *Appl. Phys. Lett*. 90 (2001).

subthreshold swing. However, the deposition of a thin, uniform high-k dielectric on a TMD surface without functionalization is challenging [13] due to the lack of surface dangling bonds. Titanyl (TiO) phthalocyanine ($C_{32}H_{18}N_8$), TiOPc, has been used as a seeding layer on WSe_2 to enable the atomic layer deposition of Al_2O_3. Record low EOT of 2.2 nm (ε_{Al2O3} = 9) and a gate leakage current density of 0.2 pA/μm^2 at 1 V gate bias have recently been demonstrated [14] and since then 0.046 pA/μm^2 has been achieved at the same EOT with process improvements.

As a measure of dielectric quality, the leakage current at 1 V gate bias is shown for representative metal-oxide-semiconductor gate systems on Si including also projections of gate leakage requirements from the International Semiconductor Technology Roadmap. There are few reports of gate leakage current in TMDs that are sufficiently thin to include on this plot. Exfoliated graphene/boron nitride/ graphene structures are shown with 1, 2, 3, and 4 ML thicknesses. These produce sub-1-nm equivalent oxide thicknesses, but leakage is far above the requirements for TFETs and MOSFETs. The results using TiOPc as a functionalization layer have produced the lowest reported leakage at the lowest EOT. The transmission electron micrograph in Fig. 8(b) shows the formation of a uniform Al_2O_3 dielectric on WSe_2 without degradation of the WSe_2 interface. The functionalization layer is a monolayer or a bilayer thick at the interface between the Al_2O_3 and the WSe_2.

TMD TFET status

At this writing, no published reports of TMD TFETs have appeared showing sub-60-mV/decade subthreshold swing, although unpublished reports are circulating. Shown in Fig. 9 are measurements of a WSe_2 TFET and the corresponding device cross-section with a top gate field plate, while Fig. 10 provides a transmission electron micrograph of the device.

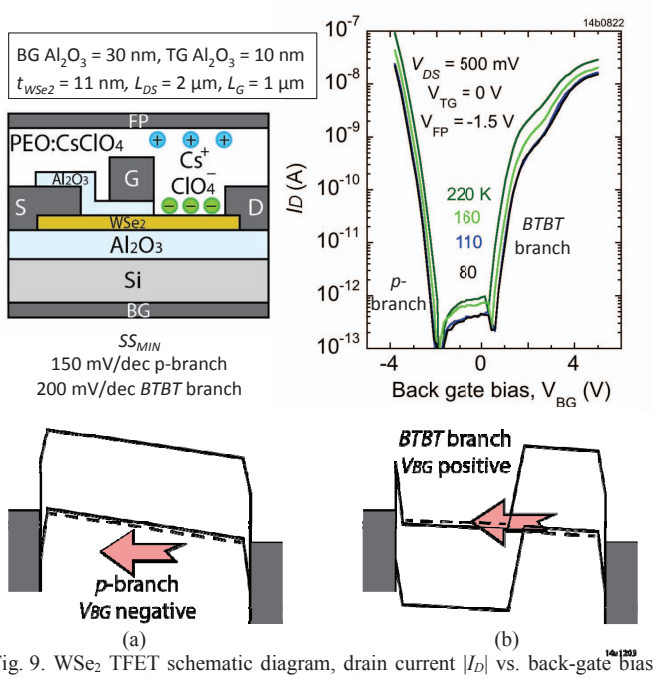


Fig. 9. WSe_2 TFET schematic diagram, drain current $|I_D|$ vs. back-gate bias V_{BG}, with the field plate (FP) biased to induce *p*-type drain doping. The band diagrams are drawn for the cases of (a) strongly negative and (b) positive back gate bias. The weak temperature dependence of the current-voltage characteristics in both back gate bias polarities is an indication that transport is controlled by tunneling and not thermionic emission. The source/drain contacts are Ti (1 nm)/Pd (90 nm).

Referring to the device cross section in Fig. 9(a). The field plate is biased negatively with respect to the source and the drain electrodes to move perchlorate ions (ClO_4^-) to the drain access region where they induce holes in the WSe_2. In preparation for the measurements, ClO_4^- ions are moved into position at room temperature in a vacuum probe station. The device is then cooled below the glass transition temperature of the electrolyte (240 K) to lock the ions into place. Once locked into place, the transistor is ready for testing.

On this particular transistor, leakage in the Al_2O_3 top gate dielectric prevented use of the top gate; however, with the ClO_4^- ions locked into place, it was possible to test the TFET using the back gate with the source and top gate set to zero volts. In this configuration, the top gate current is negligible. Figure 9 shows the transfer characteristic at a sweep rate of 170 mV/s. The back gate controls the TMD charge in the regions not controlled by the electric double layer. For negative back-gate biases, holes are induced, making the channel *p*-type as shown in the energy band diagram of Fig. 9(a). For positive back-gate biases, the channel conductivity outside of the ion-doped region changes to *n*-type, which is in a polarity to open up a band-to-band-tunneling (BTBT) window, see Fig. 9(b).

The direction of hole transport in both cases is indicated by the red arrows. The weak temperature dependence of the current indicates that the transport is controlled by tunneling, but why does the BTBT tunneling branch have higher subthreshold swing, 200 mV/decade, vs. the *p*-branch, 150 mV/decade? The reason is that as the back-gate is biased positively (Fig. 9(a) the current turns on due to modulation of

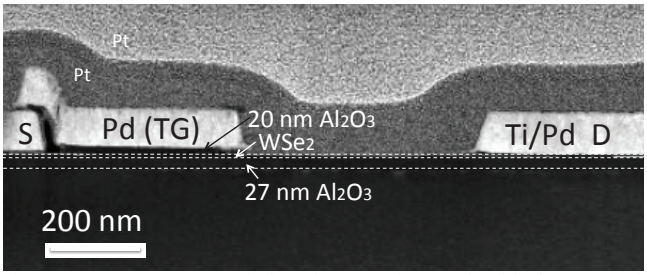


Fig. 10. WSe_2 TFET transmission electron micrograph with first generation 20 nm gate oxide after etching the Al_2O_3 in the drain access region to enable ion doping. Wafer F2, device A2-2.

the tunneling current in the source Schottky contact, while in the BTBT branch (red arrow in Fig. 9(b) the back-gate bias not only modulates the tunneling window of the *p-n* junction, but also modulates the tunneling resistance of the source Schottky contact. The lower subthreshold swing in the branch labeled BTBT tunneling is simply explained by this series connection. Both branches are tunneling branches, which is why they are both insensitive to temperature. The fact that there are two series tunneling processes in the BTBT branch is further seen in the I_D-V_{BG} characteristic by the second current inflection at V_{BG} of approximately 2.5 V. The I_D-V_{DS} characteristic was measured at V_{BG} = 5 V (not shown) to look for negative differential resistance (NDR), the signature of a *p-n* tunnel junction. NDR was not observed, consistent with the argument that the drain voltage drops primarily across the source Schottky. The last feature to explain in the transfer characteristic of Fig. 9 is the drain current reversal at low back-gate bias. This is due to photogeneration in the *p-n* junction after the tunneling window is closed.

Conclusions

Over the past 50 years, numerous technical obstacles have been encountered and overcome in the development of scaled CMOS. Similarly, the challenges facing TFET development are being systematically solved.

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