Two-dimensional semiconductors for transistors

Manish Chhowalla[1,2], Debdeep Jena[3,4] and Hua Zhang[5]

Abstract | In the quest for higher performance, the dimensions of field-effect transistors (FETs) continue to decrease. However, the reduction in size of FETs comprising 3D semiconductors is limited by the rate at which heat, generated from static power, is dissipated. The increase in static power and the leakage of current between the source and drain electrodes that causes this increase, are referred to as short-channel effects. In FETs with channels made from 2D semiconductors, leakage current is almost eliminated because all electrons are confined in atomically thin channels and, hence, are uniformly influenced by the gate voltage. In this Review, we provide a mathematical framework to evaluate the performance of FETs and describe the challenges for improving the performances of short-channel FETs in relation to the properties of 2D materials, including graphene, transition metal dichalcogenides, phosphorene and silicene. We also describe tunnelling FETs that possess extremely low-power switching behaviour and explain how they can be realized using heterostructures of 2D semiconductors.

[1]*Materials Science & Engineering, Rutgers University, Piscataway, New Jersey 08854, USA.*
[2]*Electrical and Computer Engineering, Rutgers University, Piscataway, New Jersey 08854, USA.*
[3]*Electrical and Computer Engineering, Cornell University, Ithaca, New York 14853, USA.*
[4]*Materials Science and Engineering, Cornell University, Ithaca, New York 14853, USA.*
[5]*School of Materials Science and Engineering, Nanyang Technological University, Nanyang Avenue 639798, Singapore.*

Correspondence to M.C and D.J.
manish1@rci.rutgers.edu; djena@cornell.edu

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Field-effect transistors (FETs) — three-terminal systems consisting of source, drain and gate electrodes — are integral in many electronic devices, allowing them to achieve energy-efficient high-speed switching. Semiconducting materials, also known as the channel of a FET, span the source and drain electrodes. The channel is electrically isolated from the gate electrode by the gate dielectric. The effective operation of FETs relies on efficient electrostatic coupling between the electric field induced by the gate voltage and the channel, without allowing electrons to flow between them.

Traditional FETs are, most often, based on bulk or 3D semiconductor channels composed of silicon and the III–V semiconductors, GaAs and GaN. These 3D materials have been successfully scaled down to nanoscale dimensions over the past 5 decades following Moore's law, which in 1965 predicted that the density of transistors in a chip will double every 2 years[1–4]. The semiconductor industry has established long-term strategies and research goals based on Moore's Law, but this prediction has recently started to falter and substitutes are under consideration[5].

Short-channel effects

The dimensions of FETs, and hence the lengths of the channels, continue to decrease in the quest for higher performance. Devices with shorter channel lengths have begun to experience high off-state currents; that is, some charge carriers are able to flow between the source and drain electrodes even on application of a gate voltage that suppresses the flow of current. The presence of an off-state current increases the static power (the product of the drain voltage and off-state current). As a result, the reduction in size of FETs has been limited by the rate at which heat, caused by static power, is dissipated. The current leakage and the resulting challenges associated with heat dissipation caused by an increase in static power are collectively termed short-channel effects[6,7]. The consequences of short-channel effects are detrimental for device operation and energy efficiency to the extent that the International Technology Roadmap for Semiconductors (ITRS) predicts that transistor densities will double every 3 years rather than every 2 years[8]. To address these short-channel effects, devices such as multiple gate transistors[9,10], FinFETs[11,12] and ultrathin body transistors (UTB)[13–15] are being actively pursued.

There is a need to identify new semiconductor materials that can mitigate short-channel effects. In addition, these materials should be compatible with existing complementary metal oxide semiconductor (CMOS) infrastructure. A starting point for identifying semiconductors for transistor channels is the examination of the FET electrostatics described by Poisson's equation. This equation yields a characteristic channel 'scaling length' given by $\lambda = \sqrt{t_s t_b (\varepsilon_s/\varepsilon_b)}$, where t_s is the semiconductor thickness, t_b is the gate dielectric thickness, and ε_s and ε_b are the semiconductor and gate insulator dielectric constants, respectively[6,7]. In reality, UTB semiconductors made from decreasing the thickness of 3D (bulk) materials suffer from dangling bonds, leading to scattering

of the charge carriers[16,17] (FIG. 1a). As a result, the expected enhancement in gate electrostatic properties and substantial degradation of FET performance are observed. More specifically, the mobility, μ, of charge carriers decreases with thickness to the sixth power, $\mu \sim t^6$, and the bandgap, E_g, increases by the square of the thickness, $\Delta E_g \sim t^2$ (REF. 16). For transistors made from UTB 3D semiconductors, the substantial decrease in performance is observed because of the presence of dangling bonds, undesirable coupling with phonons and the creation of interface states (that occur when the gate dielectric and the source/drain electrodes are deposited on top of the semiconductor). In 3D semiconductor short-channel FETs, current leakage arises from poor electrostatics between some electrons in the channel and the electric field applied by the gate (FIG. 1b). However, in FETs that have a channel made from 2D semiconductors, all electrons are confined in naturally atomically thin channels and, hence, all carriers are uniformly influenced by the gate voltage[17] (FIG. 1d). This excellent gate coupling allows the suppression of current leakage if a gate voltage is applied.

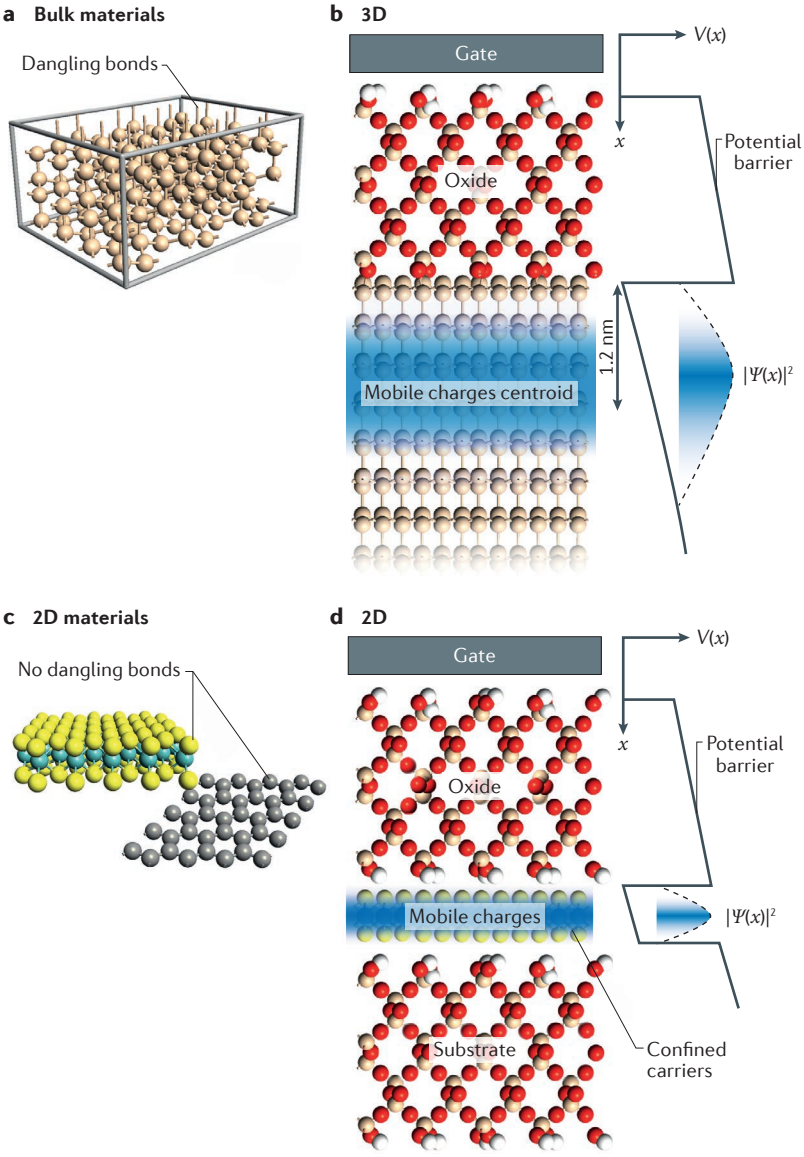

Figure 1 | **Advantages of 2D materials compared with 3D materials for FETs.** **a** | Ultrathin 3D (bulk) semiconductors have dangling bonds that form traps for electrons and reduce the performance of field-effect transistors (FETs). **b** | Gate electrostatics and mobile charge distribution in 3D semiconductors. $V(x)$ is the gate voltage as a function of the distance x. The potential barrier is the energy level of the gate dielectric and $|\psi(x)|^2$ refers to the probability function of the carriers in the semiconductors. The majority of the mobile charge carriers are located approximately 1.2 nm from the semiconductor gate dielectric interface. **c** | By contrast, 2D materials have pristine surfaces. **d** | In 2D materials, charge carriers are confined in the atomically thin semiconductor, resulting in a narrower mobile charge distribution. This confinement of charge carriers allows the carriers to be easily controlled by the gate voltage, leading to excellent gate electrostatics. Figure is adapted with permission from REF. 17, SPIE Journals and Proceedings.

2D materials

The range of 2D materials for application as the semiconducting component of FETs includes graphene, hexagonal boron nitride (h-BN), transition metal dichalcogenides (TMDs), silicene and phosphorene. Substantial research has been devoted to graphene, the 'original' 2D material, which has revealed interesting electronic[18–21] and photonic[22,23] phenomena. However, the absence of an energy bandgap makes graphene less desirable for use in FET switching settings that require high on-state currents but low off-state currents. Hence, the field has expanded into other 2D materials, predominantly semiconducting TMDs because they possess bandgaps in the range of 1–2 eV. The weak, van der Waals interactions between the layers of the corresponding bulk materials enable atomically thin layers of graphite, molybdenum disulfide (MoS_2) and black phosphorus to be isolated relatively easily by exfoliation. This approach usually results in a low density of dangling bonds and minimal surface roughness (FIG. 1c). The subsequent transfer of these 2D materials onto thin-layered insulators — for example, in the case of graphene transferred onto h-BN — almost completely eliminates dangling bonds in the insulator[24] and mitigates the effect of charged impurities by changing the dielectric environment in 2D semiconductors[25]. In another example, devices consisting of six-layered MoS_2 (semiconductor) encapsulated by few-layered h-BN (gate insulator) show high mobilities, which reach 34,000 $cm^2 V^{-1} s^{-1}$ at low temperatures[26]. Recent progress suggests that such atomically thin 2D materials could be one pathway for electronic devices in the future[27–29].

Characteristic of FETs

To highlight the advantages of using 2D materials as semiconductors in FETs, the important characteristics of the devices must be covered first (FIG. 2). A typical FET is a three-terminal device consisting of a semiconducting channel between the source and drain electrodes. The current between the source and drain electrodes — passing through the semiconducting channel — is modulated by the application of a gate voltage. The transverse electric field created by the gate voltage can either deplete the channel of carriers so that no current flows between the source and drain electrodes (off-state), or enhance the concentration of carriers in the channel, allowing current to flow (on-state). Ideally, the off-state current is as small as possible and the on-state current is $>10^4$ compared with the off-state current (that is, an on/off ratio of $>10^4$).

A FET with a semiconductor channel composed of a single-layer TMD and its operating mechanisms are shown in FIG. 2. The gate barrier is an insulator of thickness t_b, the dielectric constant is ε_b and the capacitance is $C_b = \varepsilon_b/t_b$. The channel length along the x axis is L and the width along the y axis is W. Mobile electrons in the conduction (or valence) bands of the TMD layer form Bloch waves that must fit in the rectangular channel. This restricts the Bloch waves to $k_x = n_x(2\pi/L)$ and $k_y = n_y(2\pi/W)$, where n_x, $n_y = \ldots, -1, 0, +1, \ldots$ are integers, obtained by enforcing periodic boundary conditions, and k_x and k_y are wave vectors that represent the direction of electron wavefunction propagation in the crystal lattice. The density of mobile carriers in the 2D semiconductor sheet is given by summing all of the occupied allowed electron states over all of the spins and valleys:

$$n_s = (1/WL) \cdot \sum_{(k_x, k_y) \in \text{all spin, valley}} f(k_x, k_y) \qquad (1)$$

The central problem of FET physics is determining how two voltages — one between the gate and source electrodes, V_{gs}, and the other between the drain and source electrodes, V_{ds} — control the occupation of the allowed channel modes, $f(k_x, k_y)$. The knowledge of this occupation function determines all of the output characteristics of the device. To solve this problem, we make three simplifications without neglecting important features of the FET. First, the gate insulator is ideal and allows no current to leak between the gate and the source and drain electrodes. Second, the contacts are ideal, which means there is no voltage drop at the source and drain contacts. Third, there is no scattering of electrons in the semiconductor channel. On the basis of these assumptions, we develop a detailed quantitative model for the operation of FET-based 2D materials (Supplementary information S1,S2 (box, figure)).

A FET based on 2D semiconductors has several key operating mechanisms[30,31]. When the source and drain electrodes are grounded ($V_{ds} = 0$) and a positive voltage is applied on the gate electrode, the gate battery draws electrons from the gate metal and pumps the electrons into the semiconductor channel through the source and drain contacts. The physics of FET operation can be captured by understanding how the electron density of the mobile sheet, n_s, in the semiconductor channel depends on the gate voltage. The sheet charge is often assumed to be the gate capacitance, $C_b = \varepsilon_b/t_b$, multiplied by the 'excess' voltage, $qn_s = C_b(V_{gs} - V_T)$, where q is charge and V_T is the threshold voltage determined by the difference in the work functions of the metal and the semiconductor. This is an approximation that is only true for a range of voltages when the transistor is deep in the on state — specifically, when $V_{gs} - V_T >> V_{th}$ (where the thermal voltage, $V_{th} = kT/q$, has a value of 26 mV at room temperature). This assumption fails near V_T and for off states of the FET, which may be appreciated by noticing that because n_s is the sheet density of filled states, it cannot be negative — however, $V_{gs} - V_T < 0$ for $V_{gs} < V_T$.

The energy levels of the gate metal, insulator and 2D semiconductor along the z direction of the device are plotted in FIG. 2b. The relative position of the energy levels can be represented by $q\varphi_B + qV_i - \Delta E_c + (E_{Fs} - E_c) = qV_{gs}$, where $q\varphi_B$ is the metal–dielectric barrier height, qV_i is the voltage drop in the insulator, ΔE_c is the conduction band offset, E_{Fs} is the quasi-Fermi level of the source electrode, E_c is the energy of semiconductor conduction band and qV_{gs} is the barrier modification by the applied gate voltage.

The carriers entering the channel through the source move to the right (red in FIG. 2c–f) and are in equilibrium with the energy level of the source electrode. The carriers entering the channel from the drain move to the left (blue in FIG. 2d–f) and are in equilibrium with the drain contact. The carriers cannot change direction in the channels because no scattering of electrons can occur. This results in a modal distribution of electrons in the 2D (k_x, k_y) space (FIG. 2c–f). By analysing the changes that occur in the energy levels in the presence of applied V_{gs} and V_{ds}, it is possible to derive the relationship between the carrier density and the gate voltage as,

$$e^{\frac{n_s}{n_b}}\left(e^{\frac{n_s}{n_q}} - 1\right) = e^{\frac{V_{gs} - V_T}{V_{th}}} \qquad (2)$$

where n_s is the net carrier density, n_q is a characteristic 2D quantum concentration defined in the Supplementary information and n_b is the characteristic carrier density from the electrostatic capacitance (Supplementary information S1 (box)). This is a transcendental equation, the solution to which gives the mobile carrier density in the semiconductor channel as a function of the gate voltage, $n_s(V_{gs})$.

Ideal FET output characteristics

We can use the solutions derived in the Supplementary information S1,S2 (box, figure) to calculate the output characteristics of a TMD channel FET in which transport is ballistic — that is, when electrons travel in the channel without being scattered. There are two ways to present the performance of a FET: by the assessment of either transfer characteristics (curve in FIG. 2c; FIG. 3a,b) or output characteristics (curve in FIG. 2g; FIG. 3c). Transfer characteristics are obtained by plotting drain current, I_d, as a function of the gate voltage (FIG. 3a,b). The on-state current of FETs can be obtained from transfer characteristics at different source–drain voltages. A subthreshold slope (SS; the gate voltage required to increase the drain current by a factor of ten), which indicates the switching speed of the FET, can be extracted from a transfer curve. In our simulated FET consisting of a 2D channel, the switching properties are notable in that the SS is close to 60 mV dec^{-1} at 300 K using equation 3 (REF. 16).

$$SS = \left(1 + \frac{C_s}{C_b}\right)\frac{kT}{q}\ln 10 \qquad (3)$$

where C_s is the semiconductor capacitance. The current saturates as a function of the drain voltage because it becomes energetically difficult for the drain electrode to inject carriers into the channel (FIG. 2d,g). At a fixed drain voltage, varying the gate voltage changes the number of electron energy levels that are filled at the injection point of the source, because the band edge states are capacitively coupled to the gate electrode. This changes the current exponentially when $V_{gs} - V_T << V_{th}$, and as a power

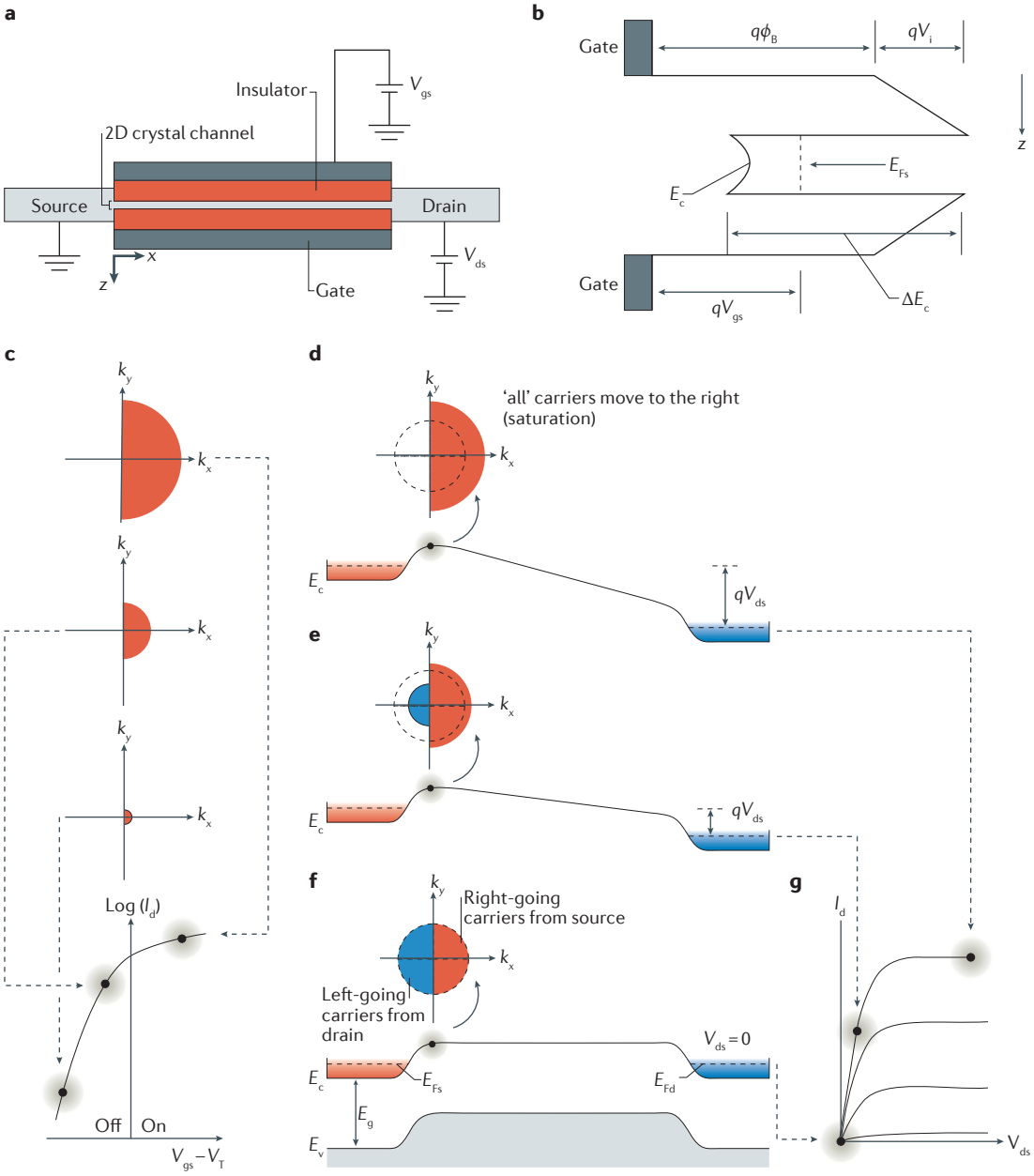

Figure 2 | **Operating principles of a FET with 2D semiconducting materials forming the channels. a** | The cross-section of a typical field-effect transistor (FET) device with source and drain electrodes, a 2D semiconductor channel and a gate electrode that is electrically separated from the channel by an insulator. V_{gs} is the gate voltage, V_{ds} is the drain bias and V_T is the threshold voltage determined by the difference in the work functions of the metal and the semiconductor. **b** | The energy-band diagram in the vertical direction near the source end of the gate, defining various energy scales and band offsets. $q\varphi_b$ is the metal–dielectric barrier height, E_{Fs} is the quasi-Fermi level of the source electrode, qV_i is the voltage drop in the insulator, E_c is the energy of the semiconductor conduction band, ΔE_c is the conduction band offset and qV_{gs} is the barrier modification by the applied gate voltage. **c** | A schematic diagram of the switching transfer characteristics of the FET with the drain biased at saturation, showing how the gate voltage controls the electron population in k space in the on and off states. $k_{x,y}$ are the wavevectors that represent the direction of electron wavefunction propagation. **d**–**f** | The energy-band diagram along the channel from the source to the drain electrode, at various drain voltages as indicated in panel **g**; E_{Fd} is the quasi-Fermi level of the drain electrode. **g** | Output characteristics of the FET. The electron distribution in the k space at the source injection point is shown at different drain voltages. The colours indicate the origin of carriers in the channel: red indicates right-moving carriers injected from the source and blue is for left-moving carriers injected from the drain. At a fixed gate voltage, the net density of the right- and left-going carriers does not change, which is why the area of the two half-circles does not change. The change with the gate voltage is indicated in panel **c**. At a large drain voltage shown in panel **d**, it is energetically unfavourable for the drain to inject carriers to the source injection point, which means all carriers at that point are from the source electrode, and the current is saturated beyond this drain voltage (panels **d** and **g**).

law when $V_{gs} - V_T >> V_{th}$ (REFS 30,31). When the transistor is switched on, the drain current in a 2D semiconductor FET is $I_d \sim V_{gs}^{3/2}$. This is similar to electron transport in a vacuum tube, which is the predecessor of the solid-state switch. This is not a coincidence, because if the transport of electrons is ballistic, the electrons effectively do not see the atoms in their path.

Output characteristics are obtained by plotting I_d as a function of V_{ds} for several gate voltages (FIG. 3c). A FET should demonstrate saturation of I_d above a certain V_{ds}. This constant current with V_{ds} is important because, in an integrated circuit, several devices are interconnected and the V_{ds} being supplied to each device is variable, but the current from each device will be the same because of the saturation behaviour. In digital circuits, the I_d of a FET has to drive the gates of a few other FETs. This is called fan-out and depends on the saturation of the I_d of a FET above a certain V_{ds}. If saturation does not occur, V_{ds} will oscillate, and the I_d and the output current of the FET will change. This causes failure of fan-out and reduces the gain of the integrated circuit. The output current of a FET should only depend on the input (gate) voltage and not on the voltage of the integrated circuit. This unidirectionality is at the heart of gain and the practical utility of digital operations of FETs.

The variation of the gate voltage provides useful information about output characteristics of the FET. If the gate voltage is modulated from +0.4 to −0.4 V, that is over 0.8 V, an on/off ratio of ~10^8 is possible (FIG. 3a). On-state current densities of ~1 mA μm^{-1} (FIG. 3a,b) are achievable at gate and drain voltages of less than 0.5 V. As a result, FETs comprising TMD semiconductors as the channels can be used for energy-efficient, low-power switching applications. Indeed, the performance of TMD FETs is comparable to silicon and III–V semiconductor FETs with shorter channels[11–15]. Moreover, the short-channel degradation is reduced in 2D channels compared with similar down-scaled FET sizes in silicon and III–V semiconductor devices.

If the swing of the gate voltage is reduced to 0.4 V (from +0.2 to −0.2 V), the achievable on/off ratio reduces to ~10^4, at a current of nearly half of that of the on current. This is an endemic problem with FETs; if the input power is constrained by the supply voltage, the switching speed (proportional to the on current) and the probability of successful operation of the electronic task (proportional to the on/off ratio) decrease. With passive gate dielectrics, the best performance is achieved in FETs in which transport is ballistic, because electrons in the channel do not lose energy as a consequence of scattering. This is because ballistic FETs are capable of achieving higher on/off ratios but maintaining high performance under the constraint of low power. One potential way of achieving this is by using a variant of the FET in which transport is not over the barrier but through it, called a tunnelling FET. 2D semiconductors are believed to be highly attractive for use in tunnelling FETs, especially in the scaling limits.

Influence of effective mass and valleys

Valleys — the local maximum in the valence band or the local minimum in the conduction band — are important features of 2D TMD semiconductors. Valleys could potentially offer additional degrees of freedom beyond the charge and spin of the electrons used in present day electronics. The first Brillouin zone — a primitive unit cell in the reciprocal lattice (or the k space) — of MoS_2 is shown in FIG. 3d. Unlike conventional semiconductors, in some 2D TMD semiconductors there is large (approximately hundreds of millielectron volts) splitting of the valence band because of broken crystal symmetries coupled to a strong spin–orbit coupling[32] (FIG. 3e). The presence of valleys offers opportunities to explore the relative effects of the effective mass of electrons, valley degeneracy and spin degeneracy on the drive current of a ballistic FET. Naïvely, it may be assumed that a small effective mass (that is, a higher velocity) and a large number of valleys will maximize the current. However, the drain current in a ballistic FET is similar to the drive current of FETs with channels composed of III–V semiconductors[33]. The dependence of the on-state current on the effective mass is non-linear (FIG. 3f). More specifically, for effective masses larger than ~$0.2m_0$, the number of valleys has a small influence on the drive current; however, at smaller effective masses, a higher number of valleys leads to a proportionately higher drive current. The spatial spread of the wavefunction is high for a very small z-directed effective mass, which is undesirable for the scaling of FETs.

Contact resistance in FETs

We now consider the realistic impact of contact resistance, R_c, on FET performance. To reap the benefits of ballistic FETs, the R_c must be reduced far below the state of the art[8]. The R_c acts as a severe source-choke – that is, it strongly restricts the injection of electrons into the channel. In addition, the effective gate voltage seen at the source injection point is not V_{gs} but $V_{gs} - I_d R_s$. This reduction in effective voltage leads to degradation in the performance of the transistor, because the current depends very strongly on the effective gate voltage at the source injection point. To appreciate the importance of the R_c, let us assume that $R_c \approx 1\,k\Omega\,\mu m$. To push a current of ~1 mA μm^{-1}, the voltage drop across the contacts is $2I_d R_c \approx 2V$. The R_c must be below ~0.1 kΩ μm to reach the ballistic limits in scaled FETs for energy-efficient logic switching. Reduction of R_c will not just benefit the performance of short-channel ballistic FETs, but also long-channel FETs. This is because the maximum drive current of long-channel FETs is severely limited by the source-choking effect in the presence of a large R_c. That is, when the channel becomes very long such that there is a significant chance for scattering in the channel, the drain current is written as $I_d = qn(x)v(x)W$, where $n(x)$ is the sheet density of carriers along the channel at point x and $v(x)$ is the ensemble velocity of the carriers at that point.

William Shockley introduced the classic model for long-channel FETs by identifying $qn(x) = C_b(V_{gs} - V_T - V(x))$, where $V(x)$ is the local channel potential, and the ensemble velocity may be written as

$$v(x) = \frac{\mu F(x)}{1 + \mu F(x)/v_{sat}} \quad (4)$$

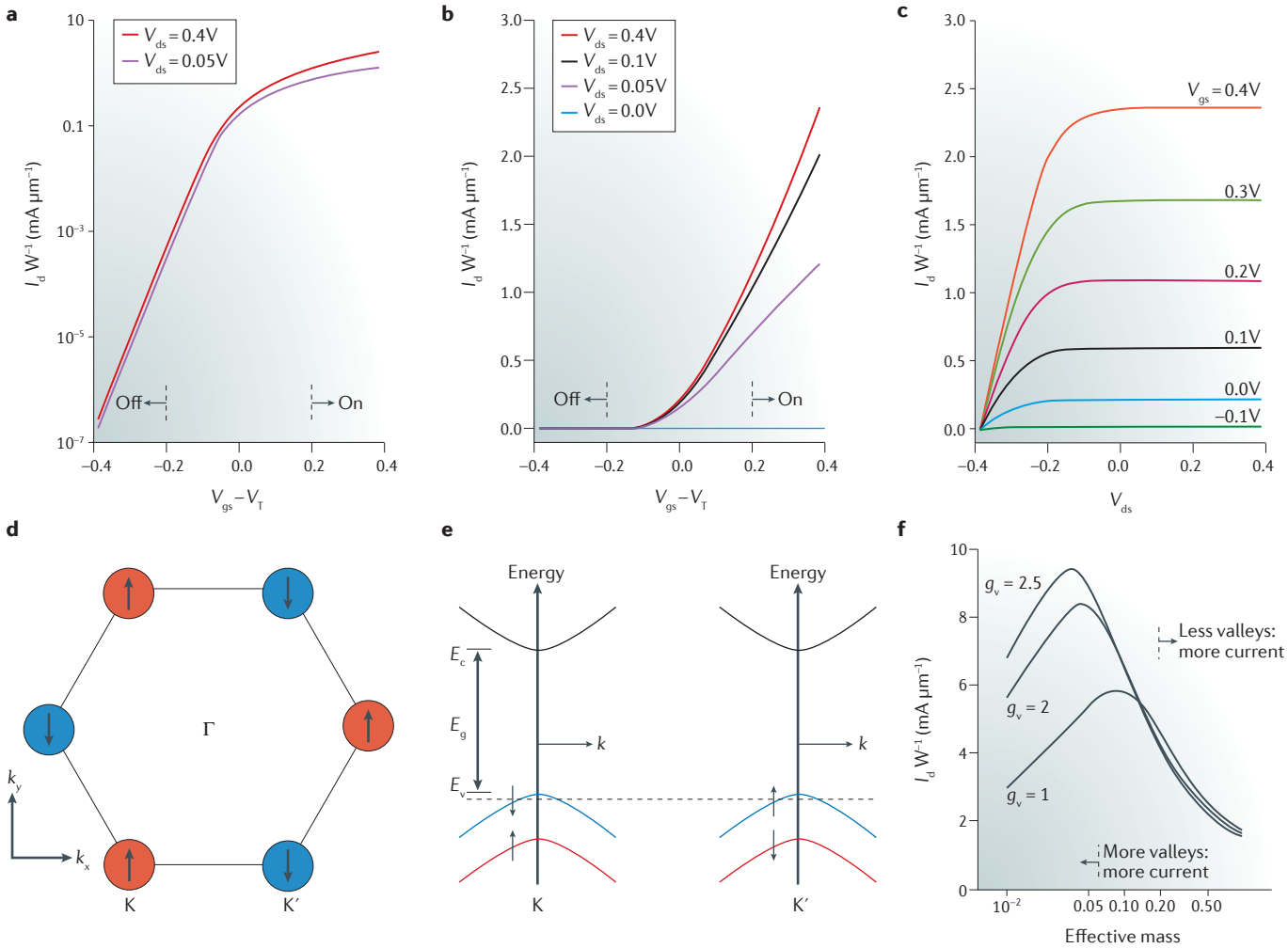

Figure 3 | **Calculated FET characteristics and spin–valley locking in the valence band of 2D TMDs.** The output characteristics of a transition metal dichalcogenide (TMD) ballistic field-effect transistor (FET) with $m_c^* = 0.5m_0$, $\varepsilon_b = 20\varepsilon_0$ and $t_b = 3$ nm are calculated (panels **a**–**c**). **a** | Transfer characteristics with the drain current, I_d, in logarithmic form for two different drain voltages (V_{ds}). **b** | Transfer characteristics in linear from at different drain voltages. **c** | Calculated output characteristics of a prototype ballistic 2D semiconductor channel FET at different gate voltages. Note that these calculations do not consider contact resistances. **d** | The electronic structure of a unit cell — referred to as the first Brillouin zone — of monolayer MoS_2. The high symmetry points (K, K′ and Γ) of the unit cell in the momentum space are indicated. The K and K′ points are two inequivalent momentum valleys: the energy maxima and minima. The arrows indicate spins of the valence electrons occupying that valence state. $k_{x,y}$ are the wavevectors that represent the direction of electron wavefunction propagation. **e** | The valence band splits at these valleys as a consequence of strong spin–orbit coupling. Time reversal symmetry requires spins to be opposite at different valleys. **f** | Drain current as a function of effective mass for three different values of valley degeneracy (g_v). The drain currents were obtained for V_{gs} and $V_{ds} = 0.4$ V. The cross-over of current scaling with valleys and effective mass depends on the gate capacitance.

where μ is the mobility, v_{sat} is the saturation velocity and $F(x) = -\partial V(x)/\partial x$ is the local channel field directed along the channel. In the absence of R_c, the on-state current for a channel length, L, evaluates to

$$I_d = \mu C_b \frac{W}{L}\left[(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}\right] \Big/ \left(1 + \frac{\mu V_{ds}}{v_{sat} L}\right) \quad (5)$$

This expression highlights the importance of mobility, saturation velocity and channel length in long-channel FETs. In this scattering-dominated limit, the details of the band structure, such as valleys and spin, are lumped into the parameters of mobility and the saturation velocity. The R_c still has a major role — whenever the voltage drop at the source side is comparable to the applied V_{ds}, the R_c causes a severe source-choke.

Semiconducting 2D materials for FETs

The demonstration of high performance FETs based on <1-nm thick single-layer MoS_2 has been an exciting development in the field of 2D electronics[34]. The first single-layer MoS_2 FETs showed on/off ratios of 10^8, mobility values of ~200 cm^2 V^{-1} s^{-1} and, importantly, SS values of 70–75 mV dec^{-1} at room temperature[34]. Although these initial mobility values were subsequently revised

downwards[35], the SS values were close to the theoretical value of 60 mV dec^{-1} for standard FET configuration[16]. In addition, the devices showed respectable on-state currents of 2.5 μA μm^{-1}. These device properties were viewed as promising because sharp turn-on, high drive current and high on/off ratios are important parameters for FETs, even for devices with moderate mobility values. These efficient properties reflect the promise of 2D materials for use in low-standby-power integrated circuits.

Graphene

2D materials can be made by mechanical or chemical exfoliation of bulk layered materials or by chemical vapour deposition of atomically thin layers[36,37]. Graphene is the most widely studied 2D material because it has an extraordinary mobility of ~25,000 cm^2 V^{-1} s^{-1} at room temperature and lacks dangling bonds. Graphene comprises an sp^2-hybridized carbon-atom arrangement in which three valence electrons form the strong in-plane covalent bonds, and the fourth electron remains in the p orbital and forms the out-of-plane π bonds. The electrons in the p orbitals are easily delocalized among the atoms, giving rise to the unique linear dispersion in graphene[38]. Graphene is often referred to as a zero bandgap semiconductor, because carriers in graphene can be influenced by gate voltage in a FET device[39]. However, the absence of a bandgap due to the delocalized electrons in graphene means that it is not possible to switch off a FET comprising graphene as the channel material, which results in impractical on/off ratios of typically <10 (REF. 39). A bandgap of ~0.1 eV can be introduced by making narrow (~10-nm wide) graphene nanoribbons; however, the fabrication of nanoribbons is challenging. In addition, this approach forms edge states in the 2D structure and thus introduces scattering, resulting in low mobility[40]. Recently, large arrays of 10-nm graphene nanoribbons have been used to make FETs with a bandgap of 140 meV. These FETs show conventional band transport at room temperature and interband tunnelling at low temperatures[41], which suggest that the edges are smooth. For comparison, it should be stated that world-record-breaking n-type and p-type FETs have been demonstrated with InSb, which has a bandgap of 170 meV, mobilities of ~30,000–40,000 cm^2 V^{-1} s^{-1} at room temperature and a carrier concentration of 10^{12} cm^{-2} (REFS 42,43). Thus, the optimization of the fabrication of graphene nanoribbons could result in FETs with attractive properties.

In recent years, the FET community has shifted its interest to 2D materials with sizable (>0.3 eV) bandgaps so that low off-state currents and high on-state currents can be realized. More specifically, mono- and few-layered TMDs[34,35,44–61], phosphorene[62–73] and silicene[74] have been incorporated into FETs.

2D transition metal dichalcogenides

TMDs have the general formula of MX_2, where M is a transition metal from group 4, 5 or 6, and X is a chalcogen atom (that is, sulfur, selenium or tellurium). A single layer of these materials consists of three atomic layers in the form of X–M–X (REF. 37). Adjacent layers of TMDs are weakly held together by van der Waals forces, which allow them to be easily exfoliated. There are approximately 40 possible members in the TMD family, many of which have been synthesized. TMDs possess diverse properties: for example, MoS_2, WS_2 and $MoSe_2$ are semiconductors; WTe_2 and $TiSe_2$ are semimetals; HfS_2 is an insulator; and NbS_2 and VSe_2 are true metals. The bandgap of most semiconducting TMDs changes with layer thickness. Bulk layered materials are indirect bandgap semiconductors, whereas single layered TMDs are direct band semiconductors[45,75]. In addition, there is an increase in the value of the bandgap for monolayers compared with the bulk; therefore, it is possible to obtain 2D semiconductors with variable band gaps from 1.1 to 2.2 eV (REF. 37). However, some TMDs, such as ReS_2, are direct bandgap semiconductors in the bulk and in single-layer forms[76]. The energy bands of some important semiconducting TMDs, graphene, h-BN, phosphorene and silicon are shown in FIG. 4a (REF. 16).

The electron orbitals of TMDs are different from those in graphene and h-BN. h-BN has an sp^2-hybridized atom arrangement and comprises three valence electrons in in-plane sp^2-hybridized orbitals, like graphene; however, the two remaining electrons of nitrogen form a highly localized lone pair, thus making h-BN a wide bandgap insulator. In contrast to graphene and h-BN, the electronic properties of TMDs are governed by the d orbitals of the transition metals, and the degree of filling of these orbitals has implications on the electronic structure as well as giving rise to interesting condensed matter phenomena, such as charge density waves, superconductivity, magnetism and hidden states[16,77–79].

MoS_2 and other TMD FETs. Despite the large number of semiconducting TMDs, research on these materials for use in electronic devices has almost exclusively focused on MoS_2, although devices with WS_2, WSe_2 and other TMDs have also been demonstrated[47,50,54–59]. MoS_2 has attracted this attention because it is readily available (in its natural form), and high quality 2D crystals can be obtained relatively easily. MoS_2 is also mechanically and chemically robust. In 2007, mechanically exfoliated crystals of MoS_2 (8–40 nm in thickness) were used as a channel material in very thin TMD FETs[80]. In a back-gated FET configuration and at a gate voltage of −50 V, n-type transport was observed with mobilities of up to 50 cm^2 V^{-1} s^{-1} and an on/off ratio of >10^5. In 2010, top-gated monolayer MoS_2 transistors with HfO_2 as the gate dielectric showed mobilities in the range of tens of cm^2 V^{-1} s^{-1} (REFS 34,35), high on/off ratios, high on currents at a source–drain voltage of 0.5 V and a low SS of 74 mV dec^{-1}. These initial results demonstrated that useful FET properties could be achieved from very thin semiconductor channels and provided encouragement for the community to pursue 2D materials for electronics.

Quantum transport simulations using the non-equilibrium Green's function have been performed to determine the scaling limits of single-layer MoS_2 transistors with high on/off ratios and good short-channel behaviour, suggesting that MoS_2 transistors could be suitable for low-power applications[46]. To demonstrate that MoS_2 transistors are immune to short-channel

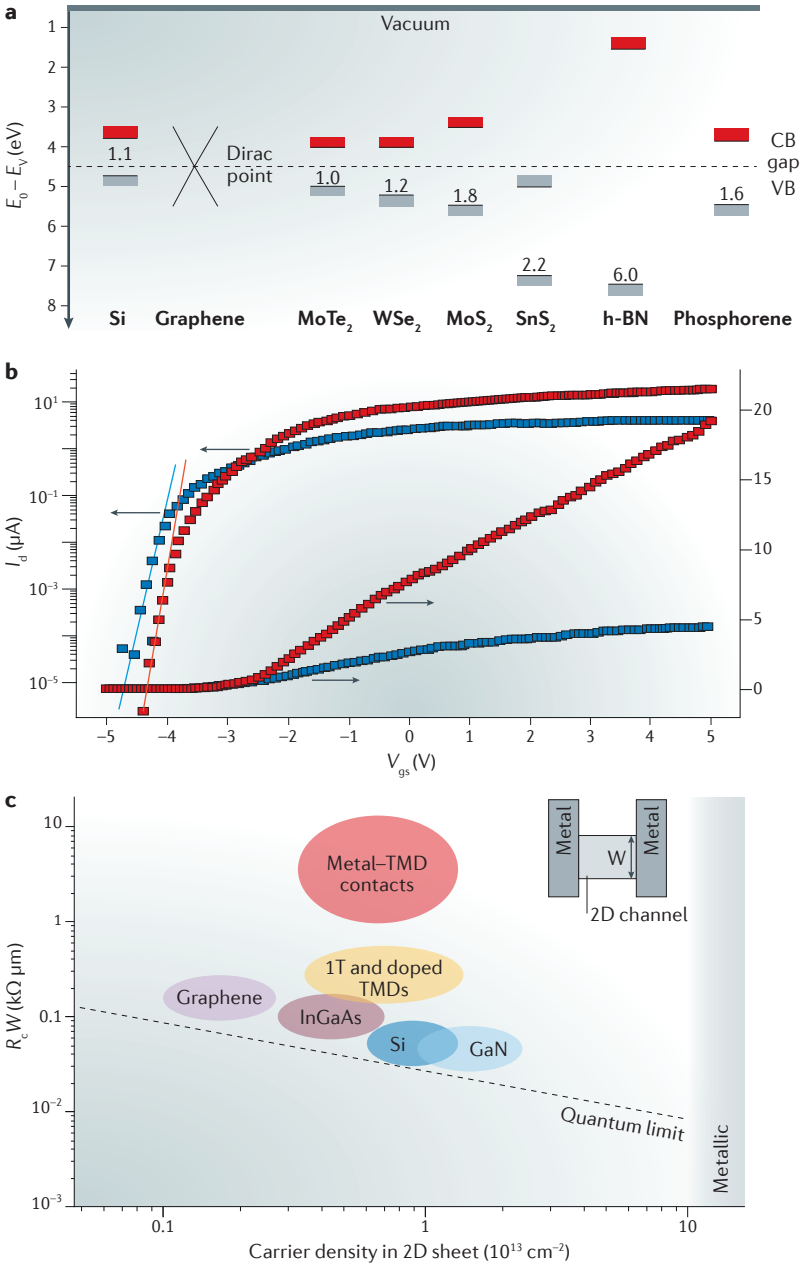

Figure 4 | **Energy band alignments and device properties of 2D materials. a** | Energy levels of various 2D materials compared with that of silicon. The numbers between the valence band (VB) and conduction band (CB) energies indicate the bandgaps of the materials. The energies with respect to the vacuum level (the work function or the electron affinity) are approximate and subject to experimental refinement. **b**,**c** | The importance of contact resistance in MoS_2 field-effect transistors (FETs). **b** | Transfer characteristics of a top-gated device measured at a drain voltage, V_{ds}, of 1 V. The red curves represent transfer characteristics of phase-engineered low-resistance contacts and the blue curves are for high-resistance contacts. Higher on-state current and lower subthreshold slopes are apparent in the phase-engineered (optimized) device. The linear fits can be used to extract the values of the subthreshold slopes, which are 95 mV dec^{-1} for the phase-engineered contacts and 100 mV dec^{-1} for the high-resistance contacts. A logarithmic scale of the drain current, I_d, is shown on the left and a linear scale is on the right. **c** | Contact resistance as a function of 2D-sheet carrier density for various semiconductors against the quantum limit. The use of metallic 1T phase transition metal dichalcogenides (TMDs) as contacts makes it possible to decrease the contact resistance. A schematic illustration of a device is shown in the inset. Panel **a** is adapted with permission from REF. 16, IEEE. Panel **b** is from REF. 60, Nature Publishing Group. Panel **c** is from REF. 88, Nature Publishing Group.

effects, FETs with channel lengths of up to 100 nm have been fabricated[81]. In addition, the performance limit of these MoS_2 transistors is a consequence of the high R_c between the contacts and the MoS_2 channel, and as such, contacts that allow full transmission of electrons from the electrodes to the channel are required for the realization of high performance short-channel devices. In a further study, the performance metrics of 5-nm-channel FETs were shown to be comparable to the ITRS 2026 low operating power technology requirements[82]. MoS_2 transistors have been fabricated with a range of metals as the contact electrodes, and it has been shown that Fermi-level pinning at the conduction band of MoS_2 strongly influences the metal/MoS_2 interface[49]. The best device performance was achieved for scandium contacts owing to high carrier injection and a low R_c of 0.65 kΩ μm (REF. 49). Another interesting approach for ensuring a low R_c, and hence high performance devices, is to degenerately dope the contacts of MoS_2 with elements, such as potassium[52]. However, doping with materials or chemicals that readily react with the environment or that evolve just above room temperature introduces instability and can cause the properties of the device to deteriorate over time. In addition to single-layer MoS_2 FETs, interesting characteristics — including mobilities of ~100 $cm^2 V^{-1} s^{-1}$ — can be obtained from multilayer MoS_2 FETs[83]. Multilayer MoS_2 has other attractive features, such as high current modulation, low SS and the ease of growing multilayer MoS_2 over a large area.

Challenges for MoS_2 FETs. MoS_2 FETs exhibit promising results; however, fundamental and practical challenges remain. For example, although the effective masses of the conduction and valence band edges have been calculated to be approximately symmetric (that is, the electron effective mass is ~0.57 and the hole effective mass is ~0.66), MoS_2 FETs usually exhibit n-type characteristics, suggesting that the channel material has been unintentionally doped[34]. The exact origin of the n-type behaviour is unclear, but the presence of impurities, such as rhenium and gold, sulfur vacancies and Fermi-level pinning near the conduction band, are possible causes[84,85]. It is also important to note that 2D MoS_2 is non-stoichiometric with a variable Mo/S ratio from ~1:1.8 to 1:2.3 (REF. 85) and that the energy of the Fermi level can vary over the surface. The structural defects, such as sulfur vacancies[86], along with impurities can limit the performance of 2D MoS_2 FETs. Synthesis of high purity and stoichiometric MoS_2 should allow the realization of ambipolar FETs. Furthermore, development of controlled doping techniques is required for tuning the polarity of the devices. These limitations can be partially overcome by sandwiching MoS_2 between layers of h-BN, which reduces the effect of charged impurities on transport properties and allows mobilities that are close to what is theoretically possible (~30,000 $cm^2 V^{-1} s^{-1}$) to be obtained, although at low temperatures[26]. Other TMDs — for example, WSe_2 — exhibit primarily p-type characteristics[47], and WS_2, which tends to be more stoichiometric than MoS_2, exhibits ambipolar behaviour[87].

Improving contact resistance. The resistance of contact electrodes is a major limitation in short-channel FETs comprising silicon and III–IV semiconductors. It has also limited the performance of FETs incorporating TMD or other 2D materials as the channel material[88,89]. Resistance at the source and drain contacts is around 10 kΩ μm in MoS_2-based FETs[49,60] — over 100 times higher than that of silicon-based electronics[8] (<20 Ω μm). Contacts in silicon or III–IV electronics are degenerately doped or regrown to achieve exceptionally low resistance and sharp interfaces[15]. These methodologies pose challenges in 2D materials because of their atomically thin nature. Future FETs will require single-layer channels and multilayer heavily doped contacts. In multilayered MoS_2 FETs, scandium electrodes[49] and doping by physisorbed molecules[52] have been successfully implemented to reduce the R_c. In another study, graphene has been shown to be an effective contact electrode material for ultrathin MoS_2 FETs[26,90,91]. Phase engineering has also been used to decrease the R_c in 2D MoS_2 devices down to 200 Ω μm (REF. 60). More specifically, TMDs can exist in either the semiconducting 2H phase or the metallic 1T phase, and interfacing these two phases in a controllable manner results in atomically sharp metal/semiconductor junctions[92]. The decrease in R_c using phase engineering allows current capacities to exceed 100 μA $μm^{-1}$ in TMD FETs[60] (FIG. 4c). Recently, phase engineering in $MoTe_2$ by laser irradiation has been shown to fabricate Ohmic contacts[93]. Phase engineering, therefore, offers a route for building lateral heterostructures with low R_c, but additional work is necessary to achieve values comparable to state-of-the-art materials and to approach the quantum limit[88,89] (FIG. 4d). In addition, methods that are compatible with electronic processing and have sufficiently good spatial resolution for device patterning are required.

Calculations have revealed that the effective masses of electrons and holes pose fundamental challenges for achieving high switching speeds in MoS_2 and other TMD-based FETs[46]. However, the large effective masses of TMDs are beneficial for switching devices, such as tunnelling FETs. Nevertheless, the excellent performance of FETs outlined above offers opportunities for realizing large area, transparent and flexible electronics[90,91,94–98]. Recent progress on the wafer-scale synthesis of high quality MoS_2 suggests that large-area monolayer MoS_2-based FETs[99] could find use in electronics for which exceptionally high processing speeds are not required.

Phosphorene FETs

In 1914, black phosphorus was synthesized by compressing red phosphorus under high pressure and at high temperatures[100]. Black phosphorus is a layered material with covalent bonds in the layers and weak, van der Waals bonds between the layers[62,101] (FIG. 5). The layers have a puckered honeycomb structure that, if stretched laterally, would result in a graphene-like hexagonal structure. Each layer consists of phosphorus atoms with three valence *p*-orbital electrons that form three covalent bonds to each other. Because all valence electrons are involved in covalent bonding, black phosphorus is a semiconducting material with a bandgap of ~0.3 eV (REF. 102). It typically behaves as a p-type semiconductor, but the origin of this behaviour is unclear, although the polarity of the FETs can be tuned by selecting contact metals with appropriate work functions. The weak bonding between each layer allows the material to be exfoliated down to a few layers with ease[62–73]. The bandgap varies as a function of the number of layers and reaches a value of ~2 eV for single-layer black phosphorus[103]. Single- and few-layered black phosphorus is referred to as phosphorene. The bulk electronic properties of black phosphorus are intriguing. In particular, electron and hole mobilities of ~1,000 $cm^2 V^{-1} s^{-1}$ have been observed[62,66]. At low temperatures, mobilities as high as 15,000 $cm^2 V^{-1} s^{-1}$ for electrons and up to 50,000 $cm^2 V^{-1} s^{-1}$ for holes have been predicted[104]. This has motivated research in electronic properties of 2D phosphorene for applications in photodetectors[105] and solar cells[65], as well as in FETs[62–68].

Single-layer phosphorene FET devices have not been widely reported because there has not been a pressing need to isolate phosphorene monolayers for this application. This is because although the value of the bandgap varies with the number of layers, phosphorene remains a direct bandgap semiconductor. The thickness of few-layered phosphorene in electronic devices is around 10 nm (REF. 106). Isolation and eventual growth of stable single- or few-layered phosphorene is essential for the development of high performance, scalable FETs. Typical transfer and output characteristics of back-gated phosphorene FETs are shown in FIG. 5b,c (REF. 66). Most reported FETs incorporating phosphorene have been in the back-gated configuration; these devices yield mobilities ranging from 100 to 1,000 $cm^2 V^{-1} s^{-1}$ with on/off ratios of ~10^4 and a SS of 1 V dec^{-1} (REFS 62–68). Top-gated devices improve the SS values to ~100 mV dec^{-1} (REF. 107). The drive current capacity of phosphorene is ~100 μA $μm^{-1}$ at a drain bias of 0.5 V, which is comparable to that achieved in TMDs. Saturation in the output characteristics, similar to the output curves of MoS_2 FETs, is also observed in phosphorene FETs. A Hall mobility, μ, reaching 6,000 $cm^2 V^{-1} s^{-1}$ has been achieved in few-layer phosphorene, which has enabled the observation of the quantum Hall effect at temperatures of <10 K (REF. 108).

An interesting feature of phosphorene is that it is electronically anisotropic; that is, transport in the armchair direction (*x* direction in FIG. 5a) is much more efficient than in the zigzag direction (*y* direction in FIG. 5a). Polarization-resolved infrared spectroscopy and angle-resolved direct current conductance measurements have been performed to elucidate the degree of anisotropy in phosphorene (REFS 62,66). Using the directional dependence of low-field conductivity for an anisotropic material given by $\sigma_\theta = \sigma_x \cos^2(\theta - \varphi) + \sigma_y \sin^2(\theta - \varphi)$ to calculate the conductance, an excellent fit with the experimentally measured data that is observed (FIG. 5d). In the equation, σ_x and σ_y are the conductivities in the *x* and *y* directions in the crystal (FIG. 4a), θ is the angle with respect to 0° along which the conductance is measured, σ_θ is the conductivity in the θ direction and, finally, φ is the angle between the *x* direction and the 0° reference. It has been reported that $\varphi = -8°$, which is in agreement with results using polarized infrared spectroscopy[66]. The high and low conductivity

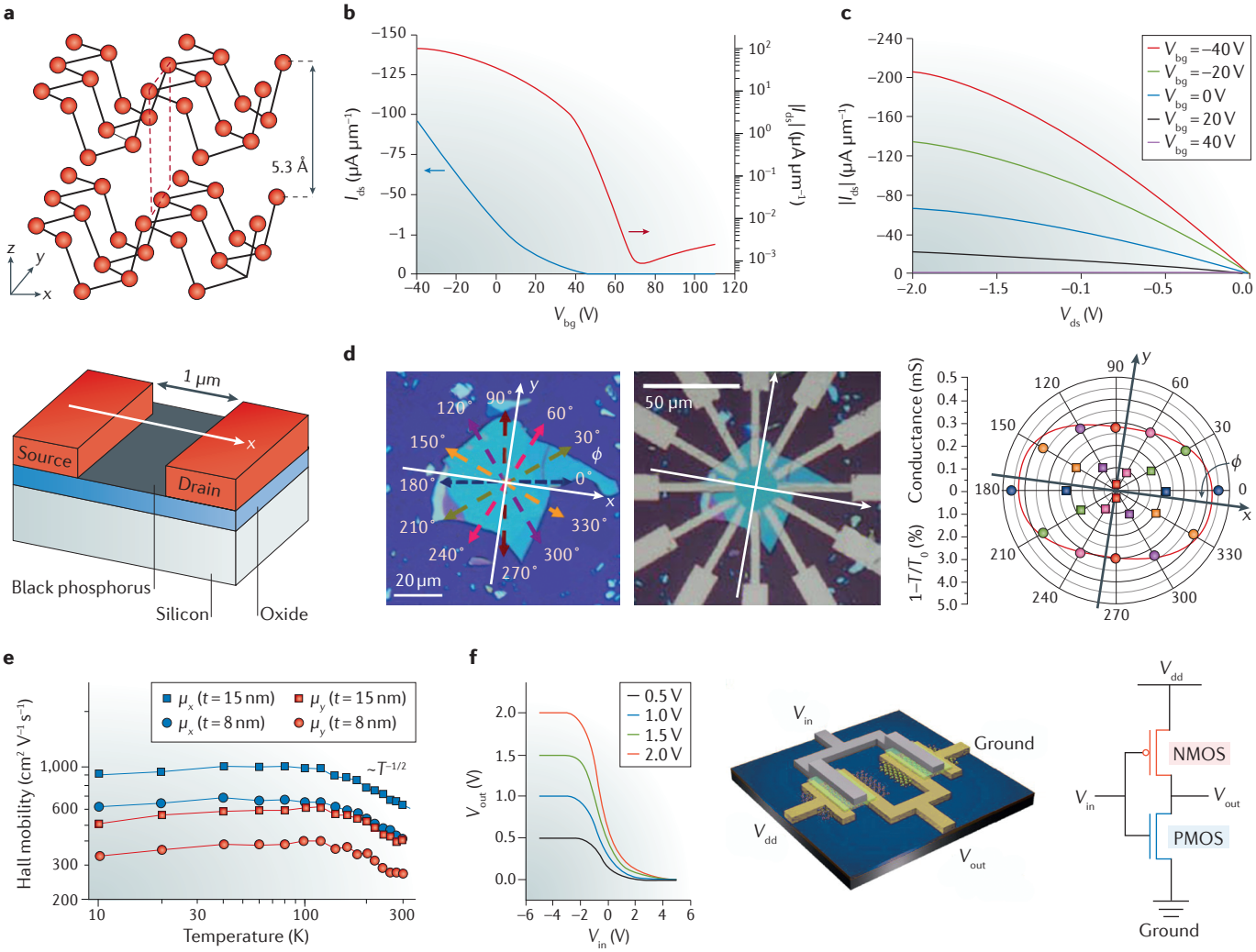

Figure 5 | **2D phosphorene for FETs. a** | The orthorhombic crystal structure of black phosphorus (top) from which few-layered phosphorene is obtained. Each phosphorus atom is bonded to three other phosphorus atoms to form a six-membered ring. The individual puckered sheets are linked by weak van der Waals bonding with a spacing of 5.3 Å. A schematic illustration of the back-gated field-effect transistor (FET) is depicted below. The *x* direction in the FET device is correlated with the *x* direction of the phosphorene lattice. **b** | Drain–source current, I_{ds}, as a function of back gate bias, V_{bg}, transfer curves for a 5-nm thick phosphorene channel of length $L = 1$ μm, showing p-type behaviour. **c** | I_{ds} versus drain-source voltage (V_{ds}) output characteristics showing current saturation. **d** | An optical micrograph of a 30-nm black phosphorus flake (left); black phosphorus flake with 12 electrodes spaced 30° apart (middle); and direct-current conductivity and relative infrared extinction (right) measured along the six directions shown in the image on the left. The circles represent direct current conductance and the squares represent polarization-resolved extinction at 2,700 cm^{-1}. The colours of the dots and squares correspond to the colours in the image on the left. **e** | Angle-resolved Hall mobility, $\mu_{x,y}$, measurements for phosphorene films show that thicker films have higher mobilities. Also, mobility along the *x* direction is ~1.8 times higher than in the *y* direction. The hole carrier concentration is constant at 6.7×10^{12} cm^{-2}. **f** | The voltage transfer curve of an inverter device consisting of n-type metal-oxide semiconductor (NMOS) MoS_2 FET and few-layer phosphorene p-type metal-oxide semiconductor (PMOS) FET (left). A schematic diagram of the inverter device is shown in the middle, and a circuit representing the inverter device is depicted on the right. V_{dd}, power supply voltage; V_{in}, input voltage; V_{out}, output voltage. Panels **a**–**e** are from REF. 66, Nature Publishing Group. Panel **f** (left) is courtesy of P. Ye, Purdue University, USA. Panel **f** (middle and right) is published with permission from REF. 62, American Chemical Society.

directions also represent the high and low mobility directions, and the ratio of σ_x/σ_y can be extracted to be ~1.5, which is slightly smaller than the experimentally measured Hall mobility values (FIG. 5e). Hall mobility measurements in the *x* and *y* directions yield a μ_x/μ_y ratio of ~1.8, because the calculations do not consider the spreading of current in the material[66].

A CMOS logic circuit has been demonstrated that consists of top-gated p-type phosphorene and few-layered n-type MoS_2 FETs[69] (FIG. 5f). Voltage transfer characteristics of these FETs show a clear transition to zero within the input voltage range from −5 to +5 V. These results also highlight the integration of two heterogeneous 2D materials for FETs.

A principal challenge associated with phosphorene is its environmental stability[109–114]. The surface of phosphorene is hydrophilic as a consequence of a permanent out-of-plane dipole moment and, as a result, it readily oxidizes[111]. More specifically, it has been recently elucidated that a combination of oxygen, light and moisture leads to rapid degradation of the material[110]. Some progress has been made on capping phosphorene using h-BN[112], atomic layer deposited Al_2O_3 (REFS 113,114) and a double-layer comprising Al_2O_3 and a hydrophobic fluoropolymer[110]. The latter double-layer approach appears to offer indefinite stability by ensuring conformal sidewall coverage to prevent diffusion from edges and moisture resistance from an effective hydrophobic surface.

Phosphorene also suffers from a high R_c, thus limiting the overall performance of the FETs. Using Ti–Au contacts, Schottky barrier heights of around 0.2 eV have been measured. New graphene side contacts have been achieved but the overall R_c remains in the kΩ-μm range[112]. However, unlike MoS_2, the Fermi level is not pinned and both p- and n-type devices can be achieved. This also suggests that phosphorene has good structural integrity and a low defect concentration, as long as the material is not exposed to the environment.

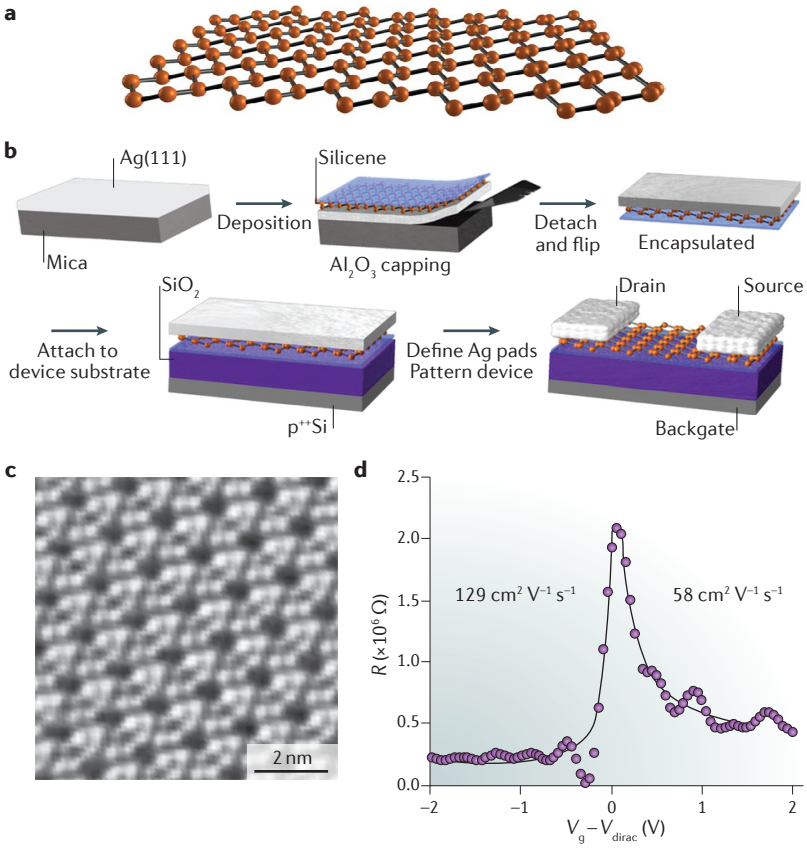

Figure 6 | **2D silicene FETs. a** | A schematic illustration of silicene showing the buckled six-membered ring structure. **b** | A fabrication route to a silicene back-gated field-effect transistor (FET) showing epitaxial growth of silicene on an Ag(111) crystalline film, *in situ* capping with Al_2O_3, delamination and encapsulation of the film, and the use of the native Ag film to produce the contact electrodes. **c** | Scanning tunnelling microscope image of Si overlayers with 4 × 4 superstructures. **d** | A transfer curve plotted of response ($R = V_d/I_d$, where V_d is the drain voltage and I_d is the drain current) as a function of overdrive voltage ($V_g - V_{dirac}$, where V_g is the gate voltage and V_{dirac} is the voltage at which R_{max} occurs). The mobility values for electrons and holes are indicated. The device indicates the range of electron and hole mobility values that can be obtained from silicene FETs. The devices fabricated[74] indicate that the bandgap in silicene is ~0.2 eV. Panels **a**–**d** are from REF. 74, Nature Publishing Group.

Silicene FETs

Silicene is an allotrope of silicon with a buckled, six-membered ring 2D structure that is analogous to graphene[115] (FIG. 6a). It is, like phosphorene, highly unstable under ambient conditions because of mixed sp^2–sp^3 hybridized bonding[116]. The use of silicene in electronic devices is particularly exciting because, if high performance devices can be realized, the existing CMOS infrastructure that is based almost entirely on the processing of silicon could be easily applied.

Silicene deposited under ultrahigh vacuum conditions on bulk single-crystal Ag(111) or thin-film substrates has been reported (FIG. 6c). An effective encapsulation and transfer process (FIG. 6b) has allowed the fabrication of silicene-based FETs, which have good mobilities at room temperature[74] (FIG. 6d). More fundamentally, the density of states in silicene is predicted to be tuned between gapped (semiconducting) and gapless (metallic) to gapped states by applying a vertical electric field. The gapless version of silicene is predicted to host topologically non-trivial states, which is why its physics, in some sense, is richer than that of graphene or sp^3-hybridized silicon. The reported transfer characteristics of silicene FETs are similar to those obtained for graphene with an on/off ratio of ~10, and hole and electron mobilities of ~129 $cm^2 V^{-1} s^{-1}$ and ~58 $cm^2 V^{-1} s^{-1}$, respectively, using the ambipolar diffusive transport model[74]. The intrinsic carrier concentration in silicene (~5×10^9 cm^{-2}) is believed to be an order of magnitude less than that in graphene, although the Fermi velocity is comparable[117,118]. These factors suggest that silicene has a small but finite bandgap of ~210 meV (REF. 74). The room-temperature oscillatory conductivity behaviour reported for silicene (FIG. 6d) could potentially point towards rich transport physics, which is sure to be explored in the future.

Tunnelling FETs based on 2D Materials

In the discussion of ballistic and long-channel FETs, constraints on the voltage swing were shown to severely restrict the on/off ratio and the current drive. The combined metric for such Boolean (on/off-based) logic operations is termed the energy–delay product, which must be minimized. The energy–delay product to complete the same circuit-level operation for several electronic and magnetic logic devices are shown in FIG. 7a (REF. 119). Some of these devices (for example, CMOS) are common, some have been experimentally demonstrated and others have only been proposed. The delay in a charge-based device is of the form $\tau = CV/I$, where I is the current drive and $Q = CV$ is the net charge to be switched. The most desirable situation (or preferred corner shown in FIG. 7a) is for FETs to perform very fast computation (lowest delay) with the least amount of energy. We see that a high-performance CMOS is fast but takes more energy to perform logic operations; these devices form

the core of powerful microprocessors in electronics today. By contrast, a low-voltage CMOS consumes less energy (by an order of magnitude), but is slower and has enabled the recent explosion of computational devices for portable electronics, such as smart phones and tablets. These slower devices lack the number-crunching capability of desktop and notebook computers but can be operated using battery power for at least 24 hours. A major challenge in semiconductor device design today is to build a device that gets closer to the preferred corner (FIG. 7) of a low-energy and low-delay product.

In a traditional metal oxide semiconductor FET, thermal electrons in a semiconductor band go over a gate-controlled barrier and, as a result, there is a tail of high-energy electrons that do not see the barrier and trickle from the source to the drain electrode[30,31]. This gives rise to a leakage current in the off state of the device. The electrostatics that drive the flow of charges in a FET give a SS close to ~60 mV dec^{-1} (as calculated in FIG. 3a and described in FIG. 8a). To reach the desired energy–delay product, the device switch needs to be made with a steeper SS (FIG. 8b). This can be achieved by changing

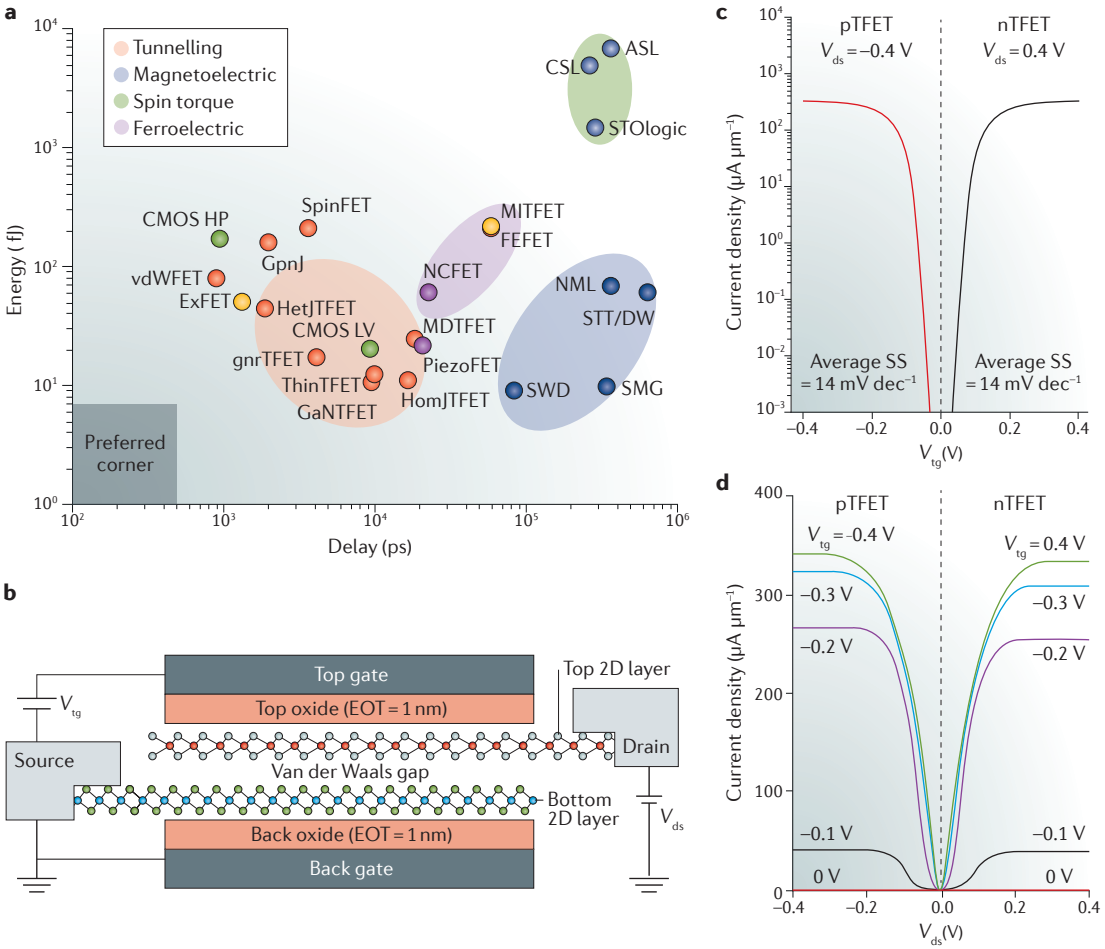

Figure 7 | **Future FET technologies. a** | Intel's benchmarking of future field-effect transistor (FET) technologies comparing complementary metal-oxide semiconductor (CMOS) high-performance and CMOS low-voltage in the energy–delay product metric for digital logic circuits. 2D semiconductor-based tunnelling FETs, such as the graphene nanoribbon tunnelling FET and the thin-tunnelling FET, show significant promise. **b** | A schematic illustration of the thin-tunnelling FET projected performance of the device. The device structure consists of vertically stacked p- and n-type transition metal dichalcogenides (TMDs) connected to drain and source electrodes, respectively. V_{tg} is the gate voltage in a tunnelling FET and V_{ds} is the drain voltage. **c** | The transfer properties reveal exceptionally low subthreshold slopes and high on/off ratios. **d** | The output characteristics exhibit excellent ambipolar modulation with tunnel gate voltage as well as current saturation. ASL, all spin logic; CMOS HP, high-performance silicon CMOS; CMOS LV, low-voltage silicon CMOS; CSL, charge spin logic; EOT, equivalent oxide thickness; ExFET, excitonic FET; FEFET, ferroelectric FET; GaNTFET, gallium nitride tunelling FET; gnrTFET, graphene nanoribbon TFET; GpnJ, graphene p–n junction; HetJTFET, heterojunction III–IV TFET; HomJTFET, Homojunction III–IV TFET; MITFET, metal–insulator transistor FET; NCFET, negative capacitance FET; NML, nanomagnetic logic; PiezoFET, piezoelectric FET; SMG, spin majority gate; SpinFET, spin FET (Sughara–Tanaka); STO, spin torque oscillator; STT/DW, spin torque domain wall; SWD, spin wave device; ThinTFET, 2D heterojunction interlayer TFET; vdW FET, van der Waals solids (or 2D Materials) FET. Panel **a** is adapted with permission from REF. 119, IEEE. Panels **b**–**d** are adapted with permission from REF. 120, IEEE.

from a passive gate insulator to an active one, for example, by using a ferroelectric layer that could boost the gate potential and possibly enable a steeper SS[120,121].

Another method to achieve a steep SS is to remove the high-energy tail that leaks from the source to the drain electrode in a normal FET. This 'energy filtering' can be achieved by introducing an energy gap at the appropriate energies in the density of states of the source of the FET. For example, inserting superlattices in 1D materials to break up the continuous energy band into a set of discrete minibands with gaps can lead to steep subthreshold FETs[122]. An easier way is if the source of the electrons is from the top of the valence band, then the valence band edge and the gap above it are a natural energy filter (FIG. 8c). However, for electrons to flow, they must overcome the barrier of the energy gap. Electrons have a wave-like nature that allows them to use evanescent states to tunnel through the gap at a low-energy cost. Transistors based on interband tunnelling, termed tunnelling FETs, are expected to enable low-power transistor switches that beat the SS limit of 60 mV dec^{-1} (REF. 123) (FIG. 8b). Getting below the traditional SS value has not been difficult; semiconductor tunnelling FETs that show steeper than 60 mV dec^{-1} switching have been demonstrated using silicon, germanium and carbon nanotubes[124]. The current drives in many such tunnelling FETs have been extremely low, leading to long delays, *CV*/*I*, making them less attractive than, for example, the low-voltage CMOS in FIG. 7a. The interband tunnelling current decreases as an exponential function of the bandgap. Narrow-bandgap semiconductors allow larger tunnelling currents, but because they are scaled down to nanoscale dimensions, the bandgaps in thinned 3D materials increase owing to strong quantum confinement effects[16].

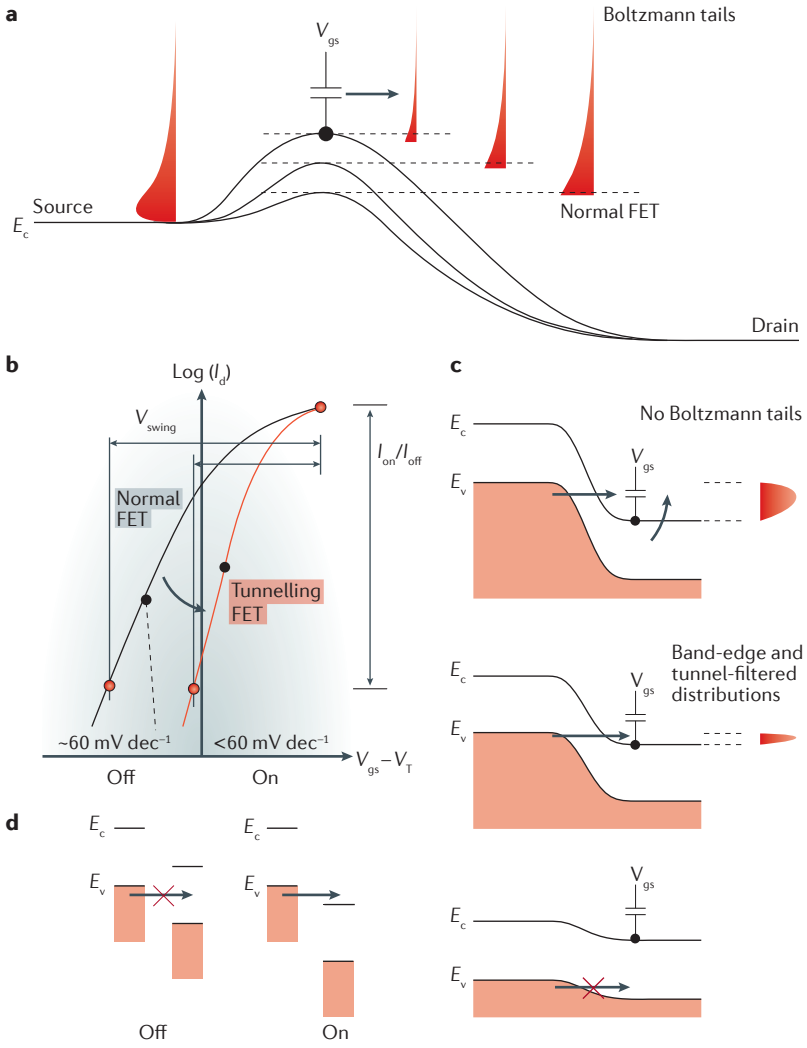

Figure 8 | **Operating mechanism of tunnelling FETs. a** | An energy band diagram showing the Boltzmann tail of electrons in a semiconductor band that leads to the 60 mV dec^{-1} subthreshold slope (SS) and drain current, I_d, leakage in a normal field-effect transistor (FET). The barrier for injection from the source can be lowered by the application of a gate voltage, V_{gs}. **b** | The transfer characteristics (drain current as a function of gate voltage of a FET) of a normal FET and a tunnelling FET. The tunnelling FET can switch at a SS of <60 mV dec^{-1} that can reduce the voltage swing (V_{swing}) — the voltage difference between the off and on states — but maintain the same on/off ratio. **c** | If the source is replaced by a filled band, the Boltzmann tail is cut off by the energy gap (top). Interband Zener tunnelling and the density-of-states overlap of the filter electrons of the valence and conduction bands in a narrow energy window, enabling a sharper turn-off, are depicted in the middle and bottom. **d** | The on current can be significantly boosted by choosing two 2D crystals with type-II or type-III heterostructure band alignment, and by interlayer tunnelling of carriers between them. The tunnelling FET can potentially allow for energy-efficient switching, because it reduces the voltage swing necessary to achieve high on current by virtue of the steep SS. E_c, energy of the conduction band; E_v, energy of the valence band; I_{off}, off-state current; I_{on}, on-state current; V_T, threshold voltage.

In this field of tunnelling FETs, crystalline 2D semiconductors are expected to provide a unique solution. Although the bandgap of a single-layer 2D crystal semiconductor is well defined, by choosing a suitable heterojunction of two layers — one n-type layer and one p-type layer (FIG. 7b) — it is possible to maximize the interlayer tunnelling current but maintain a very low SS. The tunnelling current can be boosted by the proper choice of heterojunction band offsets between the two 2D crystal layers. For example, in III–V heterostructures, the tunnelling current has been significantly increased by the choice of type-II (staggered) or type-III (broken) band alignments[125] (FIG. 8d). Similar heterostructure design opportunities exist for 2D crystal interlayer tunnelling FETs. This type of tunnelling transistor could be the thinnest possible manifestation of a tunnelling FET, which can also be scaled to the smallest dimensions, far below what may be feasible with traditional 3D semiconductors. The race is currently on to realize this proposed device, called the thin-tunnelling FET. A first step in this direction is the demonstration of interlayer tunnelling in layered 2D crystal gapped semiconductor heterostructures[126–128]. A tunnelling FET with a 2D MoS_2 channel contacted with highly doped germanium source electrodes has been reported with a SS of ~32 mV dec^{-1} and a supply voltage of <0.1 V, although at low current values[129]. The goal of achieving such tunnelling FETs is also forcing controlled growth, doping and heterostructure design, and will open several new opportunities in the future of 2D crystal electronics.

Conclusions

The inherent advantages of 2D materials — for example, the absence of dangling bonds and excellent gate

electrostatics — make them promising candidates for high performance electronics. However, the implementation of 2D semiconductors in electronic devices remains in its infancy, and some basic techniques of modern electronics are yet to be developed.

Research on 2D materials for electronics has largely focused on achieving high carrier mobilities, and this parameter is often used as a figure of merit for evaluating potential materials for FETs. However, parameters such as low SS across a wide range of gate biases, resulting in large on/off ratios at low input voltages, are more relevant for addressing the challenges of the field of electronics. In addition, contact resistance is a major factor limiting performance of 2D semiconductor FETs, especially at short-channel lengths, and must be lowered by at least an order of magnitude to <100 Ω μm. This requires the contact regions to be degenerately doped by either the direct growth of metallic multilayer 2D materials or implantation. In 2D TMDs, using metallic 2D phases is promising for the fabrication of low resistance side contacts. More generally, controllable and stable doping of 2D semiconductors is a major challenge that must be overcome in the realization of both n-type and p-type semiconductor FETs. Enhancing our knowledge on doping and uniform growth of 2D semiconductors and heterostructures should enable the next generation of low-power, high-speed devices, such as thin-tunnelling FETs, to be fabricated.

In addition to device-related challenges, uniform growth and environmental stability of 2D TMDs in their semiconducting and metallic phases are topics for future research. Although tremendous progress has been made in the uniform growth of graphene by chemical vapour deposition, large-area growth of two-element compounds (for example, MoS_2) has proven more difficult. Although polycrystalline MoS_2 and WS_2 have been grown successfully using metal–organic chemical vapour deposition, the stoichiometry, chemical purity and yield must be optimized. A fact about TMDs that is frequently overlooked is that they are rarely stoichiometric or chemically pure as a consequence of impurities in the precursors. The ability to precisely control the phases and the number of layers of TMDs also remain challenges to be addressed. Epitaxial growth methods are currently being used to fabricate 2D materials for electronic applications. These methods could be particularly important for the development of 2D semiconductors for high performance FETs as well as thin-tunnel FETs that require high-quality heterostructures. In addition, large-area growth of high-quality 2D semiconductors by chemical vapour deposition or solution-phase exfoliation could fulfil the requirements for flexible electronics.

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Competing interests
The authors declare no competing interests.

SUPPLEMENTARY INFORMATION
See online article: S1 (box) | S2 (figure)

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Box 1. Quantitative description of FET

Here we quantitatively describe the fundamental operating principles of FETs to highlight the advantages of 2D semiconductors. A typical FET with a single-layer TMD semiconductor channel and its operating mechanisms are schematically described in FIG. 2 of the manuscript. For modal distribution of electrons in the 2D (k_x, k_y)-space such as those shown in Figure 2d, the net carrier density is

$$n_s = \frac{g_s \cdot g_v}{(2\pi)^2} \frac{m_c^* kT}{\hbar^2} \pi \ln[(1+\eta_s)(1+\eta_d)], \quad (1)$$

where g_s and g_v are the spin and valley degeneracy values, m_c^* is the effective mass of carriers, $(E_{Fs} - E_c)/kT = \eta_s$ and $(E_{Fd} - E_c)/kT = \eta_d$ (E_{Fs} and E_{Fd} is the quasi-Fermi-level of the source and drain electrodes, E_c is the energy of the conduction band) are the important dimensionless source and drain degeneracy terms. When $V_{ds} = 0$, $E_{Fs} = E_{Fd}$, the relation becomes

$$n_s = D_0 kT \ln[(1+\exp[\eta_s])], \quad (2)$$

where the 2D band-edge density of states is

$$D_0 = g_s \cdot g_v \frac{m_c^*}{2\pi\hbar^2} \quad (3)$$

We identify the degeneracy energy as $\eta_s = \ln[e^{n_s/n_q} - 1]$, where $n_q = D_0 kT = C_q V_{th}/q$ is a characteristic 2D carrier concentration, defined by the product of the quantum capacitance $C_q = q^2 D_0$ and the thermal voltage. A characteristic carrier density from the electrostatic capacitance is $n_b = C_b V_{th}/q$. With these connections, we rewrite the relation of the carrier density with the gate voltage as

$$e^{\frac{n_s}{n_b}}(e^{\frac{n_s}{n_q}} - 1) = e^{\frac{V_{gs} - V_T}{V_{th}}} \quad (4)$$

the solution to which gives the mobile carrier density $n_s(V_{gs})$ in the semiconductor channel as a function of the gate voltage V_{gs}.

The drain current

$$I_d / W = J_0[F_{1/2}(\eta_s) - F_{1/2}(\eta_d)] \quad (5)$$

is obtained by summing the contribution from all modes. Here the coefficient for the current density per unit width of the transistor is $J_0 = qn_q v_{inj}$, with n_q the 2D quantum concentration, $v_{inj} = \sqrt{2kT/\pi^2 m_c^*}$ a characteristic velocity, and $F_j(\eta) = \int_0^\infty du \frac{u^j}{1+e^{u-\eta}}$ are Fermi-Dirac integrals of order j that depend on the terminal voltages $\eta_s = (E_{Fs} - E_c)/kT$ and $\eta_d = (E_{Fd} - E_c)/kT$, with $\eta_s - \eta_d = qV_{ds}/kT = v_d$. In an electrostatically well-designed FET, at the source-injection point, the gate is in complete control over the 2D carrier density. So we also have

$$n_s = \frac{D_0}{2} kT \ln[(1+\exp[\eta_s])(1+\exp[\eta_s - v_d])] \quad (6)$$

This leads to a self-consistent solution

$$\eta_s = \ln[\sqrt{(1+e^{v_d})^2 + 4e^{v_d}(e^{2n_s(V_{gs})/n_q} - 1)} - (1+e^{v_d})] - \ln 2 \quad (7)$$

where $n_s(V_{gs})$ is the solution to the central equation (4).

The three equations capture the entire output characteristics of the ballistic FET. Neither the channel length *L*, nor the carrier mobility appear in the ballistic FET current because there is no scattering. The process for mathematical evaluation of each FET component to extract the FET performance is summarized in Figure S1. The solutions can be evaluated easily on a computer and discussed in the main manuscript.

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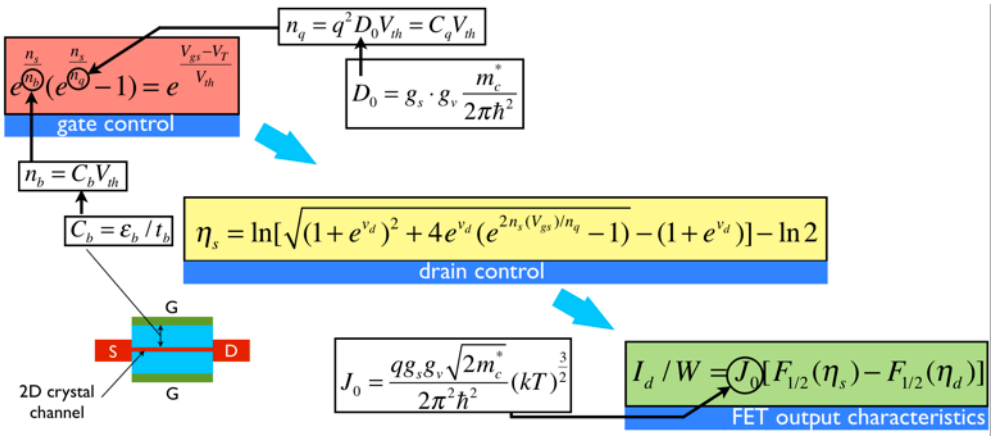

Figure 1. Flowchart for assessing performance of FETs

Flowchart for evaluating the key parameters of a ballistic FET consisting of a 2D channel, shown schematically in the lower left corner (G = gate, S = source, D = drain, blue region is the gate dielectric). The application of a gate bias V_{gs} introduces a gate capacitance (C_b), which in turn results characteristic carrier density in the channel (n_b) above the threshold voltage. The tuning of the carrier concentration via modulation of gate voltage results in an expression that relates the mobile carrier density $n_s(V_{gs})$ in the semiconductor channel as a function of the gate voltage V_{gs} [equation (4)], which includes the 2D carrier concentration (n_q) term that is related to the density of states at the band edge of the 2D semiconductor (D_0). The influence of the drain voltage, V_{ds}, on the can be obtained from the dimensionless degeneracy source term (η_s). From the gate and drain electrostatics, it is possible to extract the FET operation characteristics in terms of the drain current with gate voltage from the equation shown in the bottom right corner.