

Novel III-N Heterostructure Devices for Low-Power Logic and More*

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Abstract— Future ultra-scaled logic and low-power systems require fundamental advances in semiconductor device technology. Due to power constraints, device concepts capable of achieving switching slopes (SS) steeper than 60 mV/decade are essential if scaling of conventional computational architectures is to continue. Likewise, ultra low power systems also benefit from devices capable of maintaining performance under low-voltage operation. Towards this end, tunneling field effect transistors (TFETs) are one promising alternative. While much work has been devoted to realizing TFETs in Si, Ge, and narrow-gap III-V materials, the use of III-N heterostructures and the exploitation of polarization engineering offers some unique opportunities. From physics-based simulations, performance of GaN/InGaN/GaN heterostructure TFETs appear capable of delivering average SS approaching 20 mV/decade over 4 decades of drain current, and on-current densities exceeding 100 $\mu\text{A}/\mu\text{m}$ in aggressively scaled nanowire configurations. Experimental progress towards realizing III-N based TFETs includes demonstration of GaN/InGaN/GaN backward tunnel diodes by both MOCVD and MBE, and nanowires grown selectively by MBE and used as the basis for device fabrication.

I. INTRODUCTION

The continued increase in logic circuit complexity and capability depends critically on advances in device technology and scaling. While conventional CMOS logic is approaching fundamental limits as dimensional scaling nears material and impurity distribution limits and fabrication processing becomes increasingly challenging, perhaps a more problematic issue is one of power constraints. For many applications, power dissipation effectively limits the activity and functionality possible. Since dynamic power is proportional to V_{dd}^2 , scaling to low-voltage operation is an attractive option for maintaining the power within acceptable limits. However, the on current, I_{on} , off current, I_{off} , threshold voltage, and V_{dd} are all tightly coupled through the switching slope (SS), which is fundamentally limited to $\text{SS} \geq 60$

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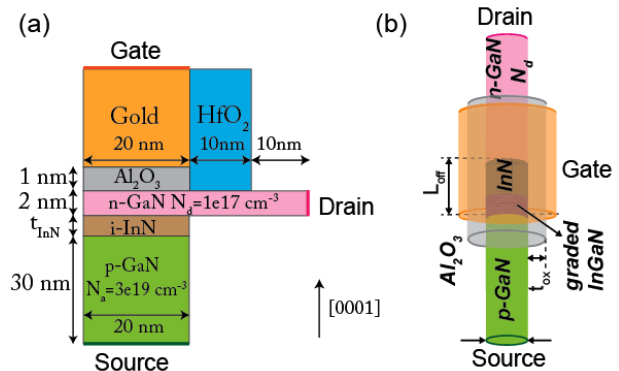


Figure 1. Candidate device structures for III-N TFETs. (a) in-line TFET, (b) nanowire TFET.

mV/decade at room temperature due to the Fermi tails in carrier distributions. This imposes strict limits on the minimum V_{dd} that can be used for any MOSFET; for example, if an $I_{\text{on}}/I_{\text{off}}$ ratio of 10^4 is required for noise margins and immunity, then $V_{\text{dd}} \geq 0.24$ V; in practice, higher V_{dd} would be required if operation above threshold (for which the effective SS is much larger than 60 mV/decade) is needed to obtain performance goals (e.g., to increase I_{on} to reduce latency).

This challenge has motivated extensive work on tunneling FETs (TFETs), which promise to enable realization of $\text{SS} < 60$ mV/decade. Extensive work on devices in Si, Ge, and narrow band gap III-V materials has been performed to pursue this goal (see e.g. [1-3] and references therein). These materials face fundamental challenges, however. With the group-IV materials, the on-current has been limited due to inefficient interband tunneling in indirect semiconductors, while for narrow-gap III-V's, the small band gaps lead to ambipolar conduction (degrading the off current) and limited SS. As an alternative that has not been widely explored, III-N heterostructures using polarization engineering to facilitate interband tunneling are potentially attractive. The candidate materials—GaN, InN, and associated alloys—are direct-gap materials, with wider band gaps than conventional materials used for TFETs. The additional design freedom afforded by polarization in these wurtzite materials provides the ability to engineer effective tunneling barriers with appreciable transmission in the on-state, while also exhibiting low off-state leakage.

In addition to potential for logic, TFETs are a promising device technology for analog and microwave/millimeter-wave applications as well. The steep SS of these devices leads to a fundamentally different g_m/I profile, and makes

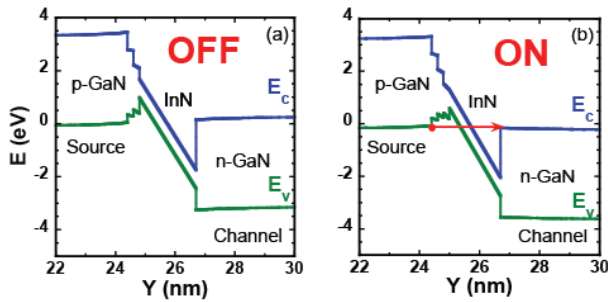


Figure 2. Computed band diagram along the channel for device in Fig. 1(b) in off- and on-state conditions [13].

TFETs extremely attractive for low-power analog and wireless applications [4]. In addition, the nonlinear characteristics of these devices are very well suited for high-sensitivity microwave/millimeter-wave detection for remote sensing and imaging applications [5-6]. We discuss here the device design, performance projections, and experimental status of efforts to demonstrate III-N TFETs with SS below the thermionic limit for applications in low-power logic and beyond.

II. DEVICE OPERATION

Figure 1 shows two candidate device structures for realizing TFETs in the GaN/InGaN material system; an in-line TFET [7] is illustrated in Fig. 1(a), while a nanowire version is shown in Fig. 1(b). The fundamental principles of operation of these devices are very similar to that of other TFET implementations: interband tunneling between the p-type source and n-type channel, with the barrier modulated by a gate. A key distinction between this material system and other typical semiconductor systems is the possibility of polarization engineering. Due to the lack of inversion symmetry in wurtzite III-Ns, the polarization discontinuity between materials at heterointerfaces (arising from both spontaneous as well as piezoelectric contributions) leads to the formation of an atomically-sharp layer of fixed charge [8]. This allows extremely high internal electric fields (exceeding 10 MV/cm) to be obtained even at modest externally-applied voltages, making high tunneling probabilities possible even in wide band gap materials such as GaN. Thus the primary challenges in designing a TFET in the III-N material system are to design a heterostructure using polarization engineering to enhance interband tunneling, while simultaneously ensuring that the electrostatics of the device are favorable for efficient gate control of the tunneling window. Figure 2 shows representative calculated band diagrams in the off- and on-states for the device structure shown in Fig. 1(b); similar principles apply also for the nanowire version shown in Fig. 1(a). As can be seen, the polarization dipole at the GaN/InGaN interfaces leads to very high electric fields in the InGaN, and by engineering the polarization discontinuity in conjunction with the thickness and composition of the InGaN interlayer, despite the large bandgap of GaN a “staggered gap” alignment between the p-type source and n-type channel can be achieved, as needed for achieving normally-off operation and high I_{on} in TFETs.

III. PERFORMANCE PROJECTIONS

The performance potential of these devices has been explored by physics-based simulation. Two distinct approaches to simulation have been pursued in order to ensure that the relevant physics are fully captured; device simulation has been performed using both commercially-available TCAD tools (Synopsys Sentaurus) [9] based on drift-diffusion simulation with a WKB-based nonlocal tunneling model as well as atomistic nonequilibrium Green’s function (NEGF) simulator (NEMO5) [10-11]. Details of the simulations and material parameters can be found in [12-13].

For the in-line TFET geometry in Fig. 1(a), simulations by TCAD and NEGF formalisms are shown in Fig. 3(a) for a GaN/InN/GaN heterojunction device [12]. From these simulations, for a 20 nm gate length device and $V_{dd}=0.5$ V, an on-current density of $\sim 75 \mu\text{A}/\mu\text{m}$ is obtained from TCAD, while NEGF projects an I_{on} of $195 \mu\text{A}/\mu\text{m}$. In addition, a SS of 12-15 mV/decade is predicted by both simulation approaches. The disparity between the two simulation projections arises from the different physics in the two simulations; the TCAD model includes a simplistic treatment of interband tunneling, but rigorously treats extrinsic access resistances. In contrast, the NEGF simulation more rigorously captures the coherent tunneling phenomena, but due to its heavy computational requirements does not include extrinsic access components. Thus the NEGF simulation provides a “ballistic limit” for device performance, while TCAD provides an indication of the role of access resistances in these devices. In both cases, steep SS as required for voltage scaling is projected. While InN is shown as the interlayer in these results, the device concept has also been explored for lower In composition interlayers as well (since growth of high In-composition interlayers by MBE or MOCVD is challenging).

As an alternative to the in-line geometry, the nanowire geometry illustrated in Fig. 1(b) has also been explored. This approach benefits from a more conventional device layout and fabrication sequence, as well as favorable electrostatic scaling. Fig. 3(b) shows the projected transfer characteristics as obtained from TCAD and NEGF for a representative III-N nanowire TFET. As with the in-line geometry, SS well below 60 mV/decade is projected (16-20 mV/decade for nanowire diameters of 32 nm and below), and with on-currents of $\sim 50 \mu\text{A}/\mu\text{m}$ projected by TCAD and $\sim 90 \mu\text{A}/\mu\text{m}$ from NEGF simulations. An extensive evaluation of device

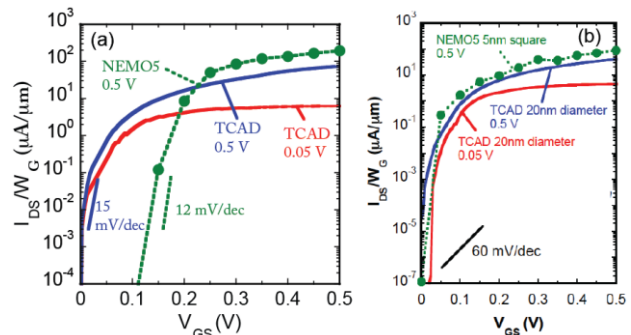


Figure 3. Projected transfer characteristics for (a) in-line TFET and (b) nanowire TFET.

design parameters and the trade-space among them is reported in [13].

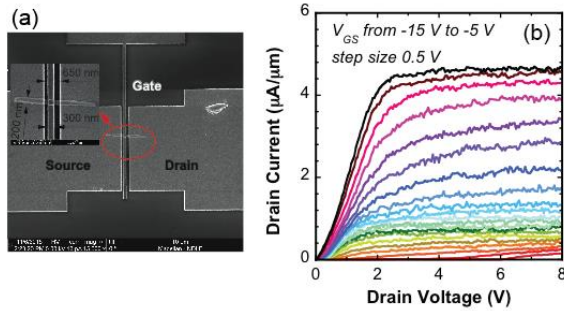


Figure 4. (a) SEM image and (b) common-source transfer characteristics of typical GaN nanowire FET [16].

IV. EXPERIMENTAL RESULTS

While TFETs based on III-Ns have not yet been demonstrated experimentally, progress towards toward this goal has been achieved. To date, n-GaN/InGaN/p-GaN heterostructure backward tunnel diodes have been achieved on both MBE- and MOCVD-grown materials with a range of InGaN compositions in the InGaN interlayer [14-15]. In these devices, the reverse current is higher than the forward current as expected for a tunnel diode, and the trends in current density are consistent with expectations from theory [15]. Reverse current densities for devices with 25% In composition interlayers exhibit reverse current densities in excess of 1 kA/cm^2 . The temperature dependence has also been evaluated experimentally, with very weak temperature dependence observed for reverse bias (as expected for interband tunneling) and a much stronger dependence in forward bias (consistent with thermionic emission) [15]. In addition, selective growth of nanowires on N-polar GaN substrates has been demonstrated, with wire diameters of approximately 50 nm.

In addition to tunnel diode demonstrations that establish the required material growth capabilities, fabrication of scaled devices has been developed. Nanowire MISFETs using MBE-grown n-type GaN nanowires have been demonstrated [16], with performance very close to that expected from numerical simulation. Figure 4 shows a micrograph and measured characteristics of a typical device. While the device in Fig. 4 is an n-channel MISFET and not a TFET, this demonstrates the key fabrication and material synthesis challenges are being addressed, highlighting a path towards realization of III-N TFETs.

V. CONCLUSION

GaN-based heterostructure devices have been explored for use in low-power logic and other applications. Simulations suggest that steep switching slopes well below the thermionic limit are possible with on-current densities suitable for practical applications. Polarization engineering in III-N heterostructures has enabled the experimental demonstration of the appreciable interband tunneling current densities required for TFET implementation.

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