First Demonstration of Strained AlN/GaN/AlN Quantum Well FETs on SiC

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Introduction

Ultra-thin body pseudomorphic GaN-on-Insulator Quantum Well FETs with MBE-regrown contacts have recently been realized as a fundamentally new strategy to create GaN CMOS-like technology that can support scaling down to ~10 nm, similar to UTBSOI [1]. The demonstration vehicle [2] used AlN-on-Sapphire templates, which have a large lattice mismatch with thick AlN layers, and very poor thermal conductivity. SiC has become the substrate of choice for GaN HEMT technology because of the availability of large size wafers and high thermal conductivity. The small lattice mismatch with AlN (~1%) makes SiC an exciting choice as a natural substrate [3] for AlN/GaN/AlN quantum well FETs. Most high-performance GaN electronics is built on SiC substrates. In this work, we demonstrate GaN quantum well FETs SiC substrates for the first time.

Experimental

The quantum well heterostructures in this work were grown in a Veeco Gen-930 plasma-assisted MBE system. Fig. 1(a) shows the layers of the heterostructure of the GaN Quantum Well FET schematically. A series of 3 structures with different GaN QW thicknesses (20/25/30 nm) were grown. The semi-insulating 6H SiC substrates were solvent cleaned, treated with buffered HF, baked at 200°C for 7 hrs and then 450°C for 1.5 hrs before high temperature MBE growth at 2.2 nm/min. A 40 nm N-rich AlN nucleation layer was first grown on SiC, followed by a slightly metal rich growth of ~250 nm AlN. Before the growth of the GaN quantum well layer, all excess Al was consumed by N_2; this crucial step was ensured by using a RHEED intensity modulation marker. The GaN quantum well was deposited under metal-rich conditions. The AlN barrier layer was grown using migration enhanced epitaxy (MEE) to ensure a smooth surface followed by a GaN passivation cap layer to protect the AlN barrier from oxidation. Because it is difficult to make low-resistance ohmic contacts to the 2DEG in the quantum well through the extreme wide bandgap AlN barrier, a mesa etch was performed and n+ GaN source and drain regions were regrown by MBE [Fig. 1(b)]. Ti/Au metal stacks were deposited for ohmic contact to the n+ GaN, and Pd/Au was deposited for gate metal.

Device Results

Fig. 1(c) shows the simulated energy band diagram for the formation of 2DEG channel for the 30 nm GaN QW structure. The measured Hall-effect transport properties at 300K and 77K are shown in Fig. 1(c). For different t_{QW}, the highest mobility of 515 cm^2/V-s achieved for 30 nm GaN QW at 300K on SiC, higher than the value reported in [2] for similar GaN quantum wells on AlN-on-Sapphire templates. The measured mobility is likely not of the 2DEG alone, and is affected by the formation of a parallel 2DHG at the bottom GaN/AlN interface. The 2DEG charge density >$2.5x10^{13}cm^{-2}$ is also higher than reported in [2]. The cross sectional HAADF-STEM image on the t_{QW}=25 nm sample [Fig. 2(a)-2(c)] GaN quantum well structure shows sharp AlN/GaN heterojunctions with the desired thicknesses for various layers. No alloying was observed between GaN and AlN. Fig. 2(d) shows the XRD ω-2θ scans for the FET structure with t_{QW} = 30 nm. Existence of SiC, AlN and GaN are clearly seen in the XRD spectra. The measured XRD spectra was fitted with a commercial software and it was found that the GaN QW was partially strained. Electrical characteristics of the 30 nm processed GaN quantum well FET are shown in Fig. 3. For a L_g=2μm gate length device with L_{gd}=1μm and L_{gs}=1μm, the linear and semi-log transfer curves in Fig. 3(a,b) show a I_d(sat)~0.5A/mm at V_{gs}~1V. The peak extrinsic transconductance is ~150 mS/mm with a ~4 orders on-off ratio. The family of I_d-V_{ds} DC output characteristics is shown in Fig. 3(c) showing current saturation and good transistor behavior for the long-channel device. These numbers show the high promise of pseudomorphic AlN/GaN/AlN quantum well FETs on SiC.

Conclusion

This is the first demonstration of strained AlN/GaN/AlN quantum well FETs on SiC substrates. The device performance, though highly encouraging for the gate lengths used, can be significantly enhanced by scaling [4]. But significant improvements are expected by ensuring the absence of the 2D hole gas, and by exploring high temperature growth of thick AlN buffer layer on SiC. This can potentially reduce the generation of threading dislocations in the subsequent layers and enhance the FET performance, by improving the transport properties.

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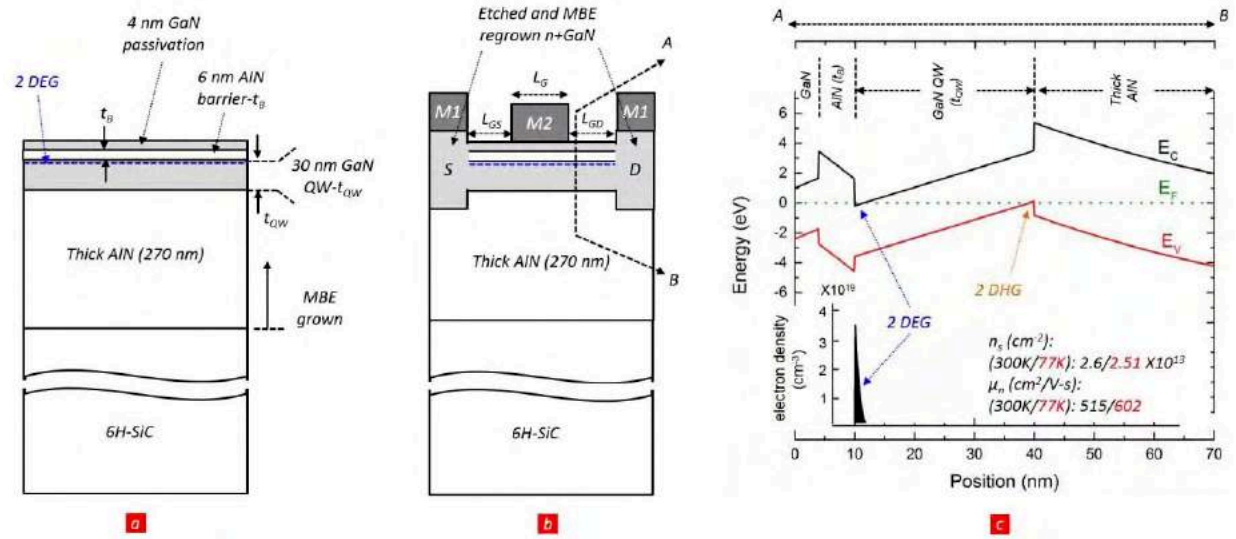

Fig. 1. a) Schematic of the strained AlN/GaN/AlN quantum well FET structure. b) Schematic of the processed device after MBE regrowth of n+ GaN source and drain regions, and ohmic and gate metal deposition (M1: Ti/Au, M2: Pd/Au). c) Energy band diagram of the QW showing the 2DEG channel at the top AlN/GaN hetero-interface, with the measured Hall-effect transport data in the inset.

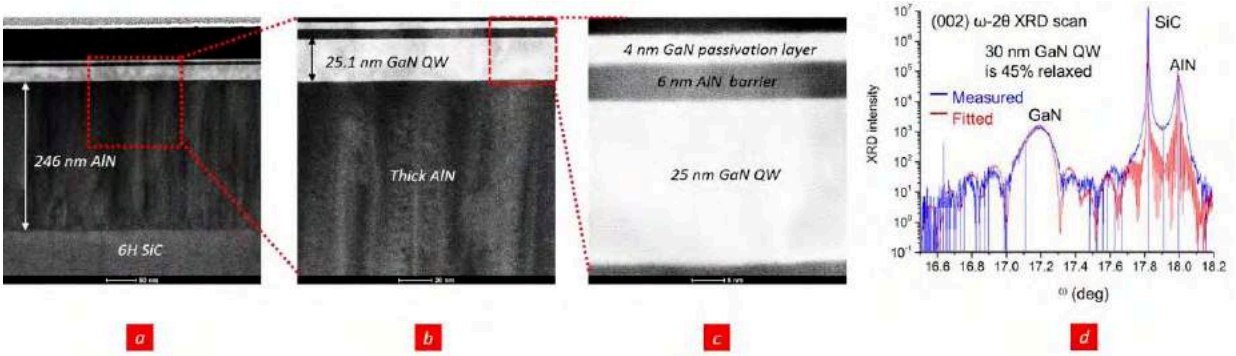

Fig. 2. Structural characterization of the strained GaN quantum well FETs. a-c) Z-contrast STEM analysis for a 25 nm GaN QW FET structure confirming abrupt hetero-interfaces between GaN and AlN. d) X-Ray diffraction spectra for 30 nm GaN QW sample showing the measured (blue) and theoretically calculated (red) curves that let us infer the thicknesses of the AlN and GaN layers. The GaN Quantum Well is found to be compressively strained as expected.

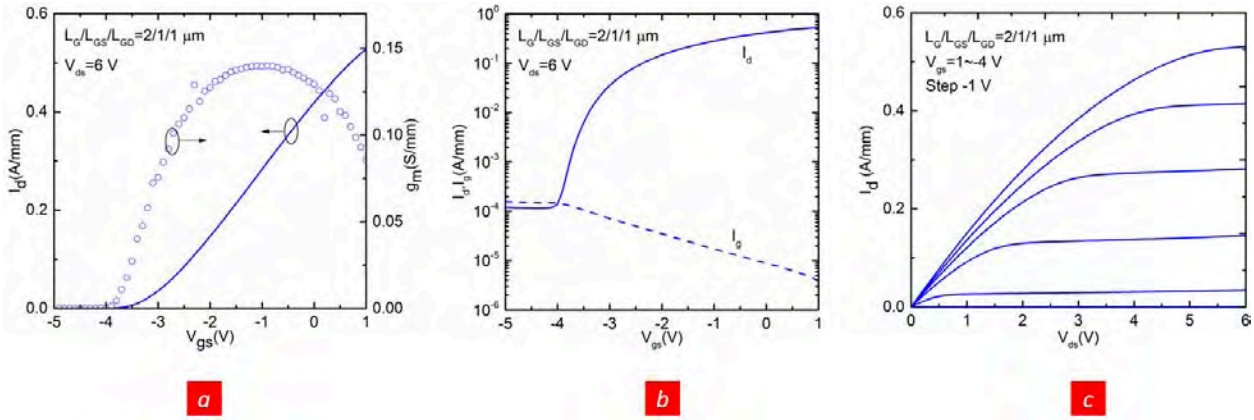

Fig. 3. Transistor characteristics for the 30 nm GaN strained quantum well FET with MBE regrown contacts. a) transfer curve at V_{ds}=6V b) semi-log transfer curve showing ~4 orders on-off ratio, and c) DC output characteristics.