

Fermi Level Tunability of A Novel 2D Crystal: Tin Diselenide (SnSe₂)

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Tin Diselenide (SnSe₂) is a two-dimensional layered crystal commonly found in octahedral coordination (1T phase). It has been reported to have a high electron affinity of around 5.1 eV and a bandgap of 1 eV [1-2], which can form staggered band alignment with tungsten diselenide (WSe₂) in Thin-TFETs [3]. However, its lack of gate modulation remains a mystery [4]. In this work, we investigate the Fermi level tunability of SnSe₂ by counter doping using a polymer electrolyte, PEO:CsClO₄. This counter doping technique increases the on/off ratio of SnSe₂ field effect transistor (FET) from 2 times to 50 times, a record high value. Meanwhile, a device model of SnSe₂ FET with ion doping and subgap density of states (DOS) has been proposed to fit the experimental data. The extracted effective number of acceptor-like subgap states is as high as $4.16 \times 10^{19} \text{ cm}^{-3}$ (in comparison with near $5 \times 10^{17} \text{ cm}^{-3}$ extracted for amorphous thin-film transistors [5]). This can explain the weak Fermi level tunability of SnSe₂ and direct future material development towards TFETs.

Device fabrication: SnSe₂ (from *2D Semiconductors*) flakes were exfoliated by scotch tape onto a 285 nm SiO₂ / p-type Si substrate. The presence of SnSe₂ was confirmed by Raman spectroscopy and the flake thickness is 5 nm determined by atomic force microscopy (AFM). Contacts (5 nm Ti/ 100 nm Au) were patterned by e-beam lithography (EBL). Before and after drop-casting PEO:CsClO₄, DC measurements were performed by a Keithley 4200-SCS parameter analyzer. A customized field probe with a flat metal plate was used to bias the electrolyte. The flat probe was placed above the PEO:CsClO₄ surface, leaving an air gap of several micrometers. Because of the air gap, a large field probe voltage of $V_{FP} = -50 \text{ V}$ was required to move the negative ions (ClO₄⁻) closer to SnSe₂, counter-doping the n⁺ SnSe₂ channel. The device schematic structure and the optical image of the device are shown in **Fig.1a** and **Fig.1b**.

Results and discussion: SnSe₂/Ti/Au contact resistance is less than $3 \text{ k}\Omega \cdot \mu\text{m}$ by four probe measurement (**Fig.1c**). **Figure 1d** shows the SnSe₂ FET's transfer characteristics when sweeping the back gate voltage (V_{BG}) before and after applying PEO:CsClO₄. Without the electrolyte, the on/off ratio is around 2 times when V_{BG} is swept from -30 V to 30 V . This low on/off ratio is attributed to a high unintentional n-type doping level in SnSe₂, which pushes its Fermi level into the conduction band where the DOS is high. To pull the Fermi level near/below the conduction band edge for improving tunability, p-type counter doping is implemented by electrostatically driving negative ions (ClO₄⁻) to the surface of n⁺ SnSe₂. With electrolyte and $V_{FP} = -50 \text{ V}$, **Figure 1d** shows that the overall current density is lowered, and more importantly, the on/off ratio is increased to 50 times. Even without applying V_{FP} , the electrolyte partially neutralizes charge in the channel due to a finite V_{DS} applied (1 V). Therefore, as shown in **Fig.1d**, the on/off ratio increases from 2 to 10 times with electrolyte at $V_{FP} = 0$. However, at a field probe voltage of 0 V, ions tend to be randomly distributed in electrolyte and move under the influence of V_{DS} and V_{BG} . The I_D - V_{DS} curves with and without electrolyte are shown in **Fig.2a-b**. In light of the low on/off ratio, we hypothesized that further turning off the device is impeded by a high subgap DOS. To verify the hypothesis, we introduce an empirical exponential subgap DOS [5] (**Fig.2c**). Under the long gradual channel approximation, the 1D Poisson equation is used to calculate the free carrier concentration in the channel (electrons in conduction band; and electrons in the subgap states are considered to be localized), which in turn is used to calculate the drain current. The device structures used in simulation are shown in **Fig.3a**, and the ClO₄⁻ ions near the SnSe₂ channel are modeled by a sheet of fixed negative charges located at 1 nm above the SnSe₂ surface [6]. Model fitting of the experimental data renders a donor concentration of $2 \times 10^{19} \text{ cm}^{-3}$ in SnSe₂, a fixed negative charge density of $2 \times 10^{13} \text{ cm}^{-2}$ in the electrolyte, and the parameters of the acceptor-like subgap DOS are shown in **Fig.2c**. The effective number of subgap states is estimated to be as high as $4.2 \times 10^{19} \text{ cm}^{-3}$ ($N_{TA} \times kT$). The band diagrams in **Fig.3c** illustrate how ion counter doping acts like a highly effective back gate, and how band bending in SnSe₂ changes when V_{BG} is changed from -30 V to 30 V . **Figure 3d** shows that if a sufficiently high back-gate voltage can be applied, the SnSe₂ FET can be turned off according to our model. Since subgap states induce undesired tunneling in the subthreshold region of a TFET, it is necessary to eliminate them to ensure proper operation of TFETs.

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References:

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SnSe₂ Band Structure Parameters Used in Simulation:

$E_G = 1 \text{ eV}$
 Electron affinity = 5.1 eV
 $m_C^* = 0.3 m_0$
 $m_V^* = 0.4 m_0$

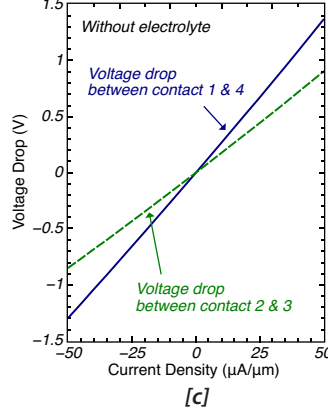
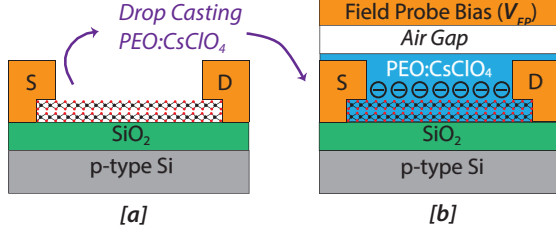


Figure 1: [a] Schematic structure of SnSe₂ back gated FET and SnSe₂ band structure parameter used in simulations; [b] Schematic structure of SnSe₂ FET with electrolyte and the device picture after fabrication; [c] I-V curves of four-probe measurement; [d] I_D vs. V_{BG} curve without electrolyte, and I_D vs. V_{BG} curves with electrolyte at zero field probe bias (i.e. $V_{FP} = 0$) and $V_{FP} = -50 \text{ V}$.

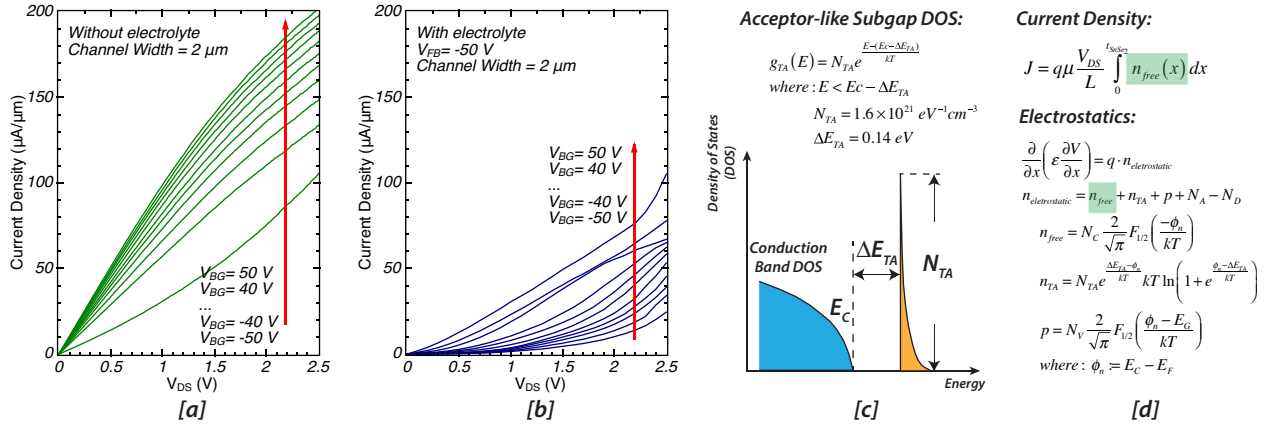


Figure 2: [a] I_D vs. V_{DS} curves without electrolyte; [b] I_D vs. V_{DS} curves with electrolyte and $V_{FP} = -50 \text{ V}$; [c] Sketch of the empirical exponential subgap DOS, and its fitting parameters; [d] Electrostatics and transport equations used in the simulations.

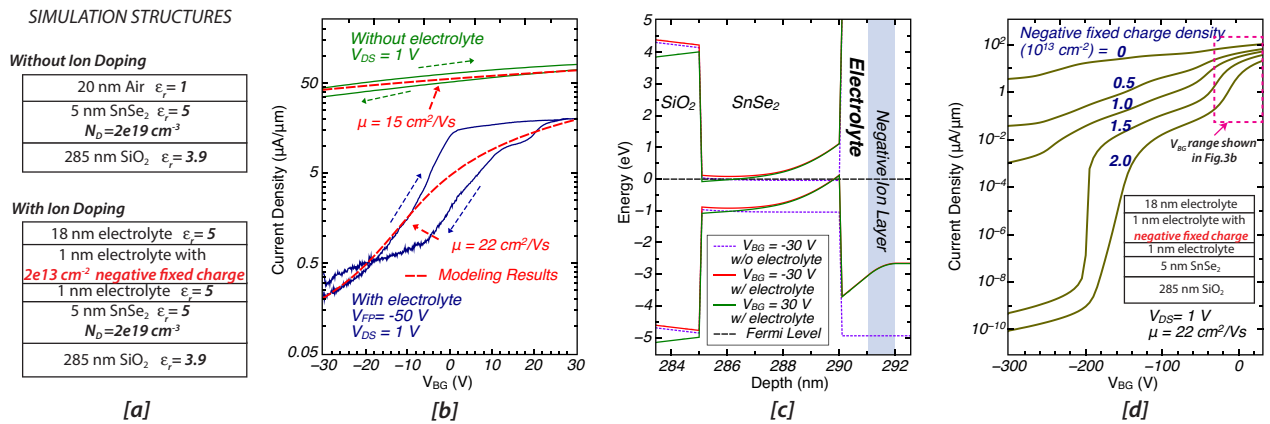


Figure 3: [a] The model structures for 1D Poisson simulations; [b] fitting models and experimental data of I_D vs. V_{BG} curves with and without electrolyte; [c] Band diagrams at $V_{BG} = -30 \text{ V}$ with and without electrolyte, and band diagram at $V_{BG} = 30 \text{ V}$ with electrolyte; [d] Simulated I_D vs. V_{DS} curves with different negative fixed charge densities in electrolyte, V_{BG} range is artificially extended down to -300 V to show the possible turn-off scenario, under the assumption that back gate oxide has no leakage regardless of the strength of the electrical field inside it.