GaN Nanowire MISFETs for Low-Power Applications

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Abstract

Gallium nitride (GaN) nanowire metal-insulator-semiconductor field-effect transistors (MISFETs) have been demonstrated experimentally. The large bandgap and high electron mobility of GaN, in addition to the 1-dimensional wrap-gate geometry, make GaN nanowire MISFETs promising for both low-power logic as well as RF applications. The fabricated GaN nanowire MISFETs exhibit an off-current (I_{OFF}) below 0.2 pA/μm, an on-off ratio (I_{ON}/I_{OFF}) above 10^8, and a subthreshold slope (SS) of 265 mV/decade. The GaN nanowire MISFET performance can be improved by the optimization of the nanowire growth and gate oxide deposition processing, as well as more aggressive device scaling.

Introduction

As complementary metal–oxide–semiconductor (CMOS) field-effect transistor (FET) scaling approaches the end of Moore's law roadmap, it is essential to have alternative device designs to achieve higher integration level and lower power consumption in integrated circuit (IC) [1-2]. At the same time, however, with the projected emergence of the Internet of Things (IoT) and ubiquitous low-power sensors and network nodes, high-speed device technologies capable of operating at very low power levels are also needed. Those real world needs have given rise to a recent expansion in nanowire FET research [2-3]. Nanowire FETs have many advantages over the conventional planar and fin-based MOSFETs. First, the 1-dimensional (1D) cylindrical geometry enables the possibility of using a wrap-around gate to improve the gate electrostatic control and mitigate the short channel effects in ultra-scaled devices. Second, small-diameter nanowires hold the promise for FETs to operate in the quantum capacitance regime at low power levels [4]. Group IV and compound semiconductor III-V nanowires have been used to fabricate FETs, showing promising DC and RF performance [2-3].

Gallium nitride (GaN)-based FETs have been widely used in power amplifiers and switches. The superior properties of GaN, such as its wide bandgap, high electron mobility, and the ability to form heterojunctions, make GaN well-suited for high-power and high-frequency applications [5-6]. The wide bandgap of GaN also suppresses the off-current (I_{OFF}), improves the on-off ratio (I_{ON}/I_{OFF}) and makes GaN FETs promising for use in harsh temperature environments required by emerging low-power and high-frequency applications, such as remote or distributed sensor networks [7-9]. GaN nanowire FETs have been demonstrated in both lateral and vertical geometries [10-11]. In this work, we report a lateral GaN nanowire metal-insulator-semiconductor FET (MISFET) for low-power applications that achieves an I_{OFF} below 0.2 pA/μm, an I_{ON}/I_{OFF} above 10^8, and a subthreshold slope (SS) of 265 mV/dec.

Device Fabrication

The GaN nanowires used to fabricate the MISFETs reported here were grown catalyst-free by plasma-assisted molecular beam epitaxy (MBE) on Lumilog freestanding N-polar n-type GaN substrates. As shown schematically in Fig. 1(a), the nanowires were formed by selective-area growth. A 5 nm-thick titanium film evaporated on the substrate was patterned with electron beam lithography (EBL) and BCl_3-based inductively coupled plasma-reactive ion etching (ICP-RIE) to form nucleation sites. The patterned substrate was intended to give accurate control of wire diameter, location, and density during the nanowire growth. To minimize the plasma damage to the GaN substrate during the dry etch, a chamber pressure of 3 mTorr, ICP power of 300 W and RIE power of 11 W (DC bias of 40 V) were used.

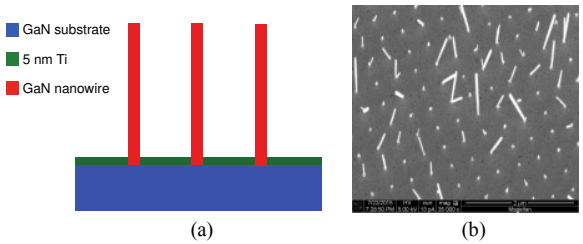

Figure 1. GaN nanowire growth on patterned free-standing N-polar GaN substrate (a) cross-sectional schematic (b) SEM image.

The patterned substrates were mounted on silicon carrier wafers with thermal paste for loading into the MBE. GaN nanowires were grown by MBE in a nitrogen-rich regime at

920 °C with a gallium flux of 7.2x10^{-8} Torr and a nitrogen plasma RF power of 400 W. The nanowires were uniformly doped at ~10^{18} cm^{-3} with silicon during the growth. Fig. 1(b) shows an SEM image of selectively grown nanowires on the patterned substrate. Although some aspects of the growth are not fully controlled (e.g. non-uniform growth rate in lateral and vertical directions, and different tilting angles for the nanowire growths), the process did yield many nanowires suitable for device processing. To better control the growth and improve the growth uniformity, improvements such as paste-free mounting as well as exploration of surfactants and growth window optimization need to be investigated in the future.

Fig. 2(a) illustrates the device fabrication flow. To fabricate the nanowire MISFETs, the nanowires were removed from the GaN substrates by ultrasonic agitation in isopropyl alcohol (IPA) and dispersed onto a host substrate, an oxide-coated silicon substrate (10 Ω-cm resistivity silicon wafer coated with 285 nm SiO_2 deposited by plasma-enhanced atomic layer deposition (PEALD)). Prior to the nanowire transfer, Ti/Au alignment markers were defined on the host substrate to help locate the randomly distributed nanowires after transfer as illustrated in Fig. 2(b). To start the device fabrication, source and drain contacts were defined by EBL and electron-beam evaporation of Ti/Au. A relatively thick gate oxide consisting of 23 nm of Al_2O_3 was then deposited on the sample by thermal ALD, and a Ti/Au "Ω-gate" wrap-around contact was defined on top of the Al_2O_3. Fig. 2(c) shows SEM images of a completed device, which has a source-drain distance of 650 nm, a gate length of 300 nm, and a nanowire diameter of 200 nm.

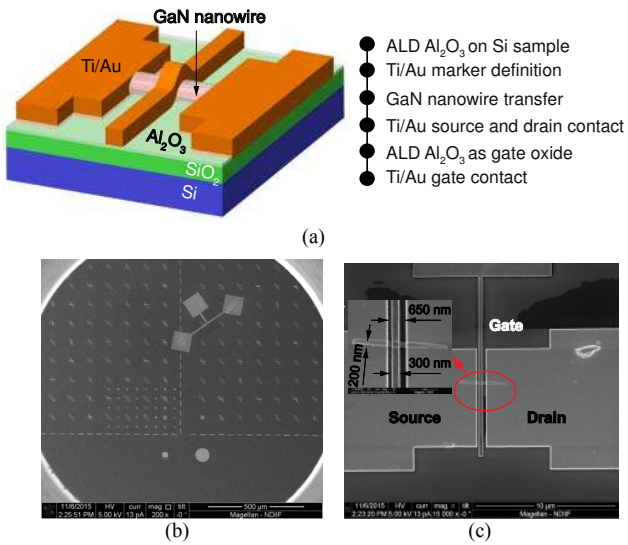

Fig.2. GaN nanowire MISFET (a) schematic diagram and process flow; (b) SEM image of alignment markers and device on the host substrate; (c) SEM image of a completed device (inset): detailed view of the active channel region.

Device Characterization

Fig. 3(a) and (b) show the measured transfer characteristics of a fabricated nanowire MISFET, which shows normally-on depletion mode (D-mode) operation with a threshold voltage (V_{th}) around -13 V, as expected for the combination of a large-diameter heavily-doped wire in conjunction with the thick gate oxide used here. The current densities reported here are normalized with respect to nanowire diameter (a "layout centric" normalization). The nanowire FETs show an I_{OFF} smaller than 0.2 pA/μm (corresponding to an absolute current of ~10 fA, the noise floor of the Agilent 4156C semiconductor analyzer used for the measurement), an on-current (I_{ON}) of ~ 5 μA/μm, and an on-off ratio exceeding 10^8 (limited by the measurement noise floor). The gate leakage current is also well below the measurement noise floor, suggesting negligible tunneling current through the thick gate dielectric. The relatively large gate equivalent oxide thickness (EOT) of 9.4 nm also limits the SS behavior, showing a modest value of 265 mV/dec at 1 V drain bias in Fig. 3(a). The thick nanowire body (~200 nm diameter) and high channel doping concentration (~10^{18} cm^{-3} doping level) also contribute to the modest SS. At a drain bias of 5 V, the peak transconductance (g_m) is extracted to be 2.2 μS/μm, as shown in Fig. 3(b).

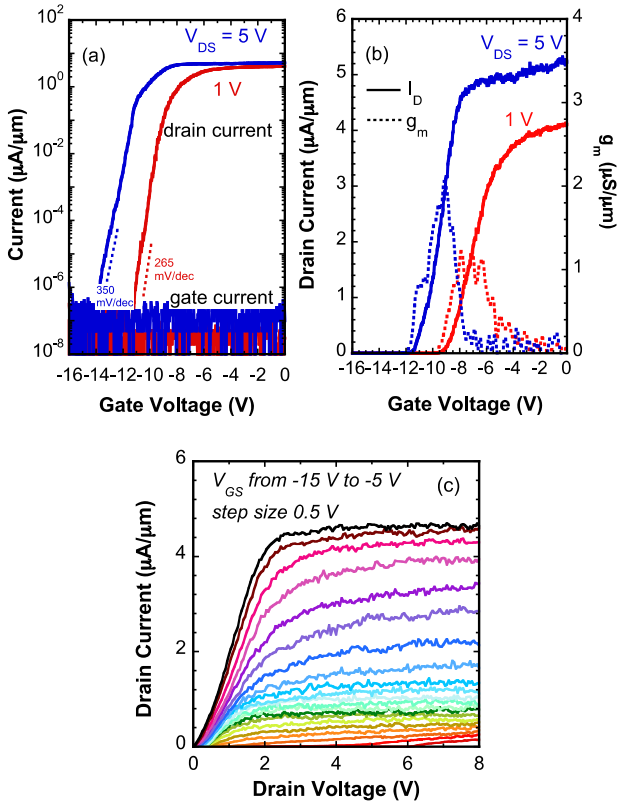

Fig.3. GaN nanowire MISFET transfer characteristics in (a) log scale (b) linear scale (with transconductance) and (c) common-source output characteristics.

Fig. 3(c) illustrates the device common-source output characteristics, which show typical ohmic and saturation behavior. A drain voltage offset of ~0.6 V can be observed, which is caused by the Schottky barriers from the unannealed Ti/Au source and drain contacts. The imperfect contacts also limit the I_{ON}. Good saturation can be observed for those devices. To improve the device DC characteristics, it is essential to scale the EOT and body thickness and lower the channel doping (to achieve a steeper SS), while improving the ohmic contact with different metal stacks and surface treatment strategies to improve I_{ON} and transconductance.

ANALYSIS

To analyze the device non-idealities, Synopsys Sentaurus TCAD was used to simulate the structure shown in Fig. 4(a) [12]. The simulated structure was based on the measured device dimensions, with an ideal gate-all-around geometry and defect-free oxide-semiconductor interface. The source and drain contacts were simulated as Schottky contacts with a barrier height of 0.6 eV, as extracted from the common-source output characteristics. The 200 nm-diameter nanowire was uniformly doped at 1.5×10^{18} cm^{-3}. The resulting transfer characteristics in Fig. 4(b) show a V_{th} and I_{ON} close to the experimental data, with a sharp turn-on behavior and an SS of ~ 90 mV/decade.

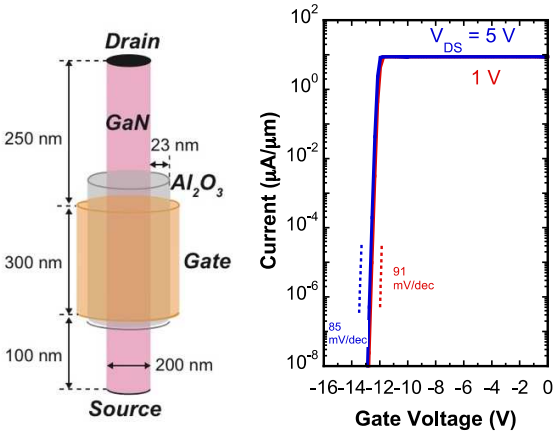

Fig.4. Device schematic and simulated transfer characteristics obtained from TCAD for GaN nanowire MISFETs of the same geometry as the experimentally demonstrated devices.

The discrepancy between the calculated and the experimental SS can be mainly attributed to the interface traps at the oxide-semiconductor interface, which compromises the gate modulation efficiency. The interface trap density (D_{it}) can be extracted by comparing the measured SS to the calculated SS through the following relation [13]:

$$SS_{meas} = SS_{cal}\frac{C_{ox} + C_D + D_{it}q^2}{C_{ox} + C_D}$$

Using this formula, the D_{it} is estimated to be $\sim 7.8\times10^{12}$ cm^{-2}. To mitigate the interface trap effect on gate efficiency, improved surface treatment techniques (e.g. [14]) are being investigated, while strategies to improve gate electrostatic control (i.e. reducing gate oxide thickness and nanowire diameter) will also be investigated to minimize the effects of interface charges.

Despite the limitations of this first generation of devices, the extremely low I_{OFF} and high I_{ON}/I_{OFF} in GaN nanowire MISFETs make them promising candidates for future low-power applications, with potential for integration with silicon and other device technologies. Ongoing work is focused on optimizing nanowire growth, improving the contact resistance, scaling the EOT and body thickness, and controlling the oxide-semiconductor interface quality to enhance I_{ON} , g_m and SS.

CONCLUSIONS

In this paper, the fabrication and characterization of GaN nanowire MISFETs has been demonstrated experimentally. Typical fabricated devices show low I_{OFF}, large I_{ON}/I_{OFF} and a modest SS. To improve the device performance, in terms of I_{ON}, g_m and SS, future work will be focused on optimizing the nanowire growth, contacts, oxide-semiconductor interface quality, and device scaling to shorter gate lengths.

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