Two-dimensional Heterojunction Interlayer Tunnel FET (Thin-TFET): From Theory to Applications

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***Abstract*—**We review the conception and development of two-dimensional heterojunction interlayer field effect transistor (Thin-TFET), where a steep subthreshold swing (SS) and a high on-current are estimated theoretically. The Thin-TFET has been experimentally demonstrated using $WSe_2/SnSe_2$ stacked heterostructures, where the SS is mostly likely limited by the interfacial trap density of states and the parasitic MOSFET. Due to its vertical stacking structure, Thin-TFET intrinsically has a smaller gate-drain capacitance compared to the conventional lateral pin-TFET. In turn, this results in mitigated Miller Effect in Thin-TFET thus reducing dynamic energy dissipation in circuits.

I. Introduction

Extending the road beyond CMOS, Tunnel Field Effect Transistors (TFETs) promise sub-60 mV/dec sub-threshold swing (SS) to triumph over MOSFETs in performance. Around 2011, various groups including ours independently arrived at a TFET structure based on a pair of electron and hole layers for optimized performance [1-5] though deriving from slightly different considerations of a TFET, which has great resemblance to the green transistor proposed in 2008 [6] and the gate-normal-TFET and ITFET proposed around 2013 [7]. In 2011 our group also reported the first experimental demonstrations of such a TFET based on III-Vs [1,2].

To obtain sub-60 mV/dec SS values, TFETs require a strong gate control over the channel, which in turn demands ultra-thin body or nanowire channel structures. However in 3D materials, size induced quantization enlarges the bandgap and impedes realization of near broken gap alignment between the source and channel in ultrascaled TFETs [8,9], which is desired to achieve high on-current in TFETs. Layered 2D crystals offer a native thickness of about 0.6 nm with a variety of bandgaps and band-alignments. Ideally, 2D crystals posses a sharp turn on of density of states at the band edges and have no surface dangling bonds thus potentially enabling a low interfacial density of state, which are highly desired for achieving a sharp SS. Motivated by the need for ultrascaled TFETs and our previous studies on heterojunction TFETs with type-I, II and III band alignments [1,2,9], we proposed the Two-dimensional Heterojunction Interlayer Tunneling FET (Thin-TFET) based on 2D layered materials. This paper reviews our effort on the modeling of Thin-TFETs, the recent experimental demonstration using $WSe_2/SnSe_2$ stacked heterostructures, and the discovery of the mitigated Miller effect in Thin-TFETs compared to pin-TFETs.

II. Modeling Approach

A. Device Structure and Working Principle

The Thin-TFET device structure is shown in Fig. 1, where the bottom and top 2D semiconductors act as the source and the drain, respectively. A van der Waals (vdW) gap separates the top and bottom 2D semiconductors. The device working principle can be explained as follows: take the p-type Thin-TFET as example, when the conduction band edge of the bottom 2D semiconductor E_{CB} is higher than the valance band edge of the top 2D semiconductor E_{VT} (Fig. 2), tunneling from the bottom layer is inhibited and the device is nominally off. When a negative top gate voltage pulls E_{VT} above E_{CB} (Fig. 3(a)), a tunneling window is opened thus current can flow.

B. The Eletrostatics and Interlayer Tunneling

The band alignment along the direction perpendicular to the 2D semiconductors is calculated using a 1D Poisson's equation with the effective mass approximation [10]. The interlayer tunneling current density is formulated by the transfer-Hamiltonian method [10], expressed as:

$$J_T = \frac{g_v e |M_{B0}|^2 A}{4\pi^3 \hbar} e^{-2\kappa T_{vdW}} \int_{\mathbf{k}_T} \int_{\mathbf{k}_B} d\mathbf{k}_T \, d\mathbf{k}_B S_F(q) S_E(E_B - E_T)(f_B - f_T) \quad (1)$$

where κ is the decay constant of the wave-function in the vdW gap, T_{vdW} is the thickness of the vdW gap, $\mathbf{k}_{T(B)}$, $\mathbf{E}_{T(B)}$, and $f_{T(B)}$ are the wavevector, the energy and Fermi occupation function in the top (bottom) 2D semiconductor and M_{B0} is the tunneling matrix element, which is estimated from the experimentally measured interlayer charge transfer time. (1) assumes that in the tunneling process electrons interact with a random scattering potential with a spectrum $S_F(q) = \pi L_C^2 / (1 + q^2 L_C^2/2)^{3/2}$, where $q=|k_T-k_B|$ and L_C is the correlation length. The scattering relaxes the momentum conservation. The energy broadening in the 2D semiconductors is described by $S_E(E) = \exp(-E^2/\sigma^2) / (\sqrt{\pi\sigma^2})$, where σ is the energy broadening parameter. The simulated I-V curves are shown in Fig. 3 (b-c), promising desired SS and high on-current.

III. Experiments

We first investigated a vdW heterojunction tunnel diode composed of black phosphorus (BP) and $SnSe_2$ [11] since these two layered-semiconductors possess a broken-gap (type-III) energy band offset. The presence of a thin insulting barrier

between p^+BP and $n^+$$SnSe_2$ enabled the observation of a prominent negative differential resistance (NDR) region in the forward-bias current-voltage characteristics, with a peak to valley ratio of 1.8 at 300 K and 2.8 at 80 K.

Following these efforts, we constructed Thin-TFETs composed of WSe_2 and $n^+$$SnSe_2$ vdW heterojunctions. The representative transfer I_d-V_g curve measured over the heterojunction is shown in Fig. 4(b), where the left branch is due to interband tunneling from the valence band (VB) of WSe_2 to the conduction band (CB) of $SnSe_2$ and the right branch is a result of carrier drift from WSe_2 CB to $SnSe_2$ CB. When WSe_2 is p-doped by the gate, it is consistently observed that the tunneling branch (reverse bias) exhibits a smaller SS than the MOSFET branch (forward bias), see Fig 4 (c). This is an indication that the dominant mechanism responsible for the reverse-biased current is interband tunneling between the layers. The I_d-V_{ds} family curves measured on our Thin-TFETs exhibit current saturation, see Fig. 5(a).

In today's Thin-TFETs, the SS is often degraded due to 1) the presence of interface traps at channel and dielectric interfaces, consistent with the SS often higher than 90 mV/dec in our WSe_2 MOSFETs; 2) the parasitic lateral WSe_2 MOSFET. In Fig. 5, we compare the I_d-V_g transfer curves and corresponding SS with and without the lateral MOSFET, of an experimentally measured device. It is seen that the lateral parasitic MOSFET could raise the SS by at least 20 mV/dec.

IV. Mitigated Miller Effect

Most TFET designs fall into two categories in terms of device structure: lateral (pin-)TFETs with tunneling direction perpendicular to the gate electric field and vertical TFETs with tunneling and gate electric field direction aligned. Layered-materials based pin-TFET is the latest breed of the lateral TFET, and its vertical counterpart is Thin-TFET. It has been reported that the pin-TFET has a much larger gate-drain capacitance (C_{GD}) compared to MOSFET, therefore exacerbated Miller effects [12]. A large Miller capacitance leads to large voltage overshoot/undershoot and longer switching time in the transient response of a circuit. In this section, we show that the C_{GD} in a Thin-TFET is significantly reduced, about half of that in a pin-TFET.

C. Charge Partition

In an n-type pin-TFET (see Fig. 6), the 100/0 drain/source charge partition gives a much larger C_{GD} than a MOSFET [12]. In an n-type Thin-TFET, under the gate there is channel but also the heavily doped p^+source. For an efficient top gate control of the band alignment between the top layer (channel, i-region) and bottom layer (source, p^+region) in a Thin-TFET, the top channel layer has to have a low carrier concentration to avoid screening out the electric field from the top gate, while the bottom layer has to have a very high carrier concentration to terminate the electric field. Since most of the electric field from the top gate terminates at the source beneath the gate, the change of the gate terminal charge is mainly reflected in the source instead of the drain. Therefore, *a Thin-TFET intrinsically has a smaller C_{GD} than a pin-TFET.*

D. Modeling of C_{GD} and Transient Response

The analytical expressions of C_{GD} and gate efficiency for Thin-TFETs and pin-TFETs are shown in Fig.7. The C_S term in the C_{GD} expression for Thin-TFET arises from the vertical gate-channel-source region, which helps to reduce C_{GD} of Thin-TFETs. Unlike a double-gated pin-TFET, a Thin-TFET is effectively gated from the top only, thus the band edge of the bottom layer moves in the same direction as the band edge of the top layer. The gate efficiency of a Thin-TFET, measured by the change in tunneling window with respect to the change in gate voltage, is lower than that of a pin-TFET. C_{GD} in Thin-TFETs and pin-TFETs has been modeled by a charge-based capacitance model using 2D Poisson simulations (Fig. 7). To evaluate the impact of C_{GD} in TFETs based circuits, the transient response of a complementary TFET inverter is simulated. As expected, the Thin-TFET inverter has a smaller voltage overshoot/undershoot, and less dynamic energy dissipation thanks to its smaller C_{GD}.

V. Conclusion

Simulations suggest that Thin-TFETs can achieve desired SS and high on-current. Performance limiters have been identified in the ongoing experimental work. The vertical structure of Thin-TFETs has an intrinsically smaller Miller effect, making Thin-TFETs more attractive in ICs.

Acknowledgment

This work was supported in part by the Center for Low Energy Systems Technology (LEAST), one of the six SRC STARnet Centers, sponsored by MARCO and DARPA. The authors are grateful for discussions with Profs. A. Seabaugh, R. Feenstra, S. Fullerton and A. Kummel.

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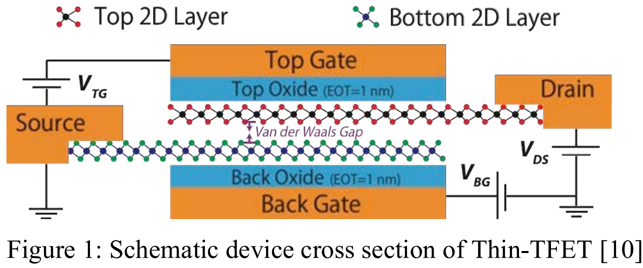

Figure 1: Schematic device cross section of Thin-TFET [10]

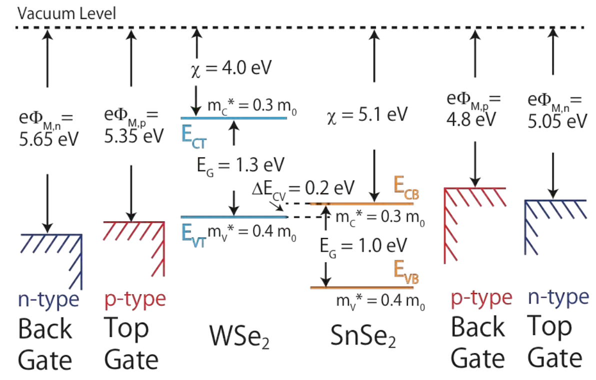

Figure 2: An example to realize both *n*-type and *p*-type Thin-TFETs using one pair of 2-D semiconductors (2H-WSe_2 and 1T-$SnSe_2$) with a near broken gap band alignment [10].

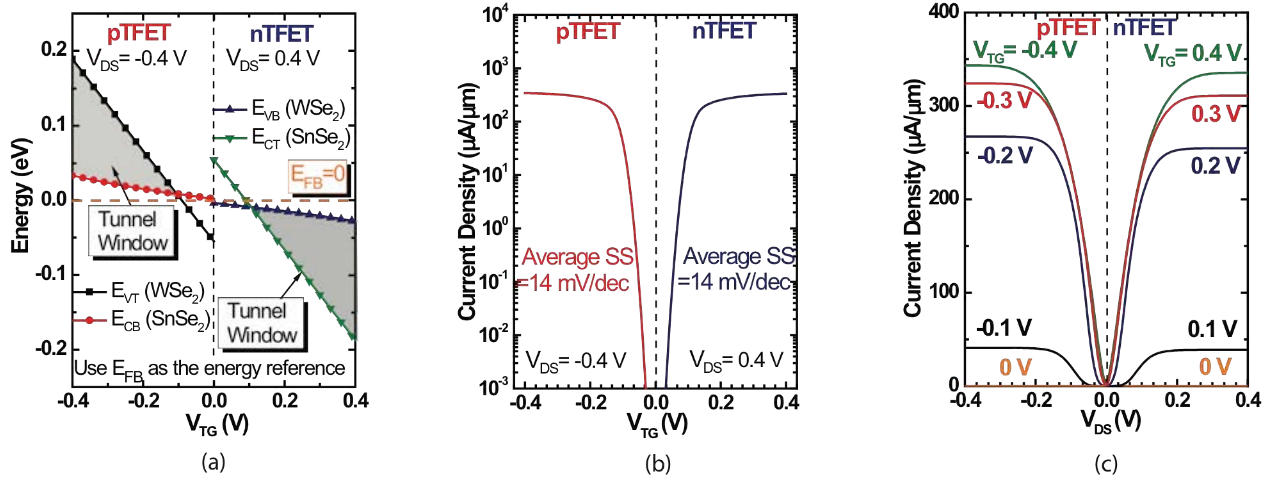

Figure 3: For the *n*-type and *p*-type Thin-TFETs shown in Fig. 2. (a) Band alignment versus V_{TG} . (b) Current density versus V_{TG} , the average SS is calculated from 10^{-3} µA/µm to 10 µA/µm. (c) Current density versus V_{DS} at various V_{TG} [10].

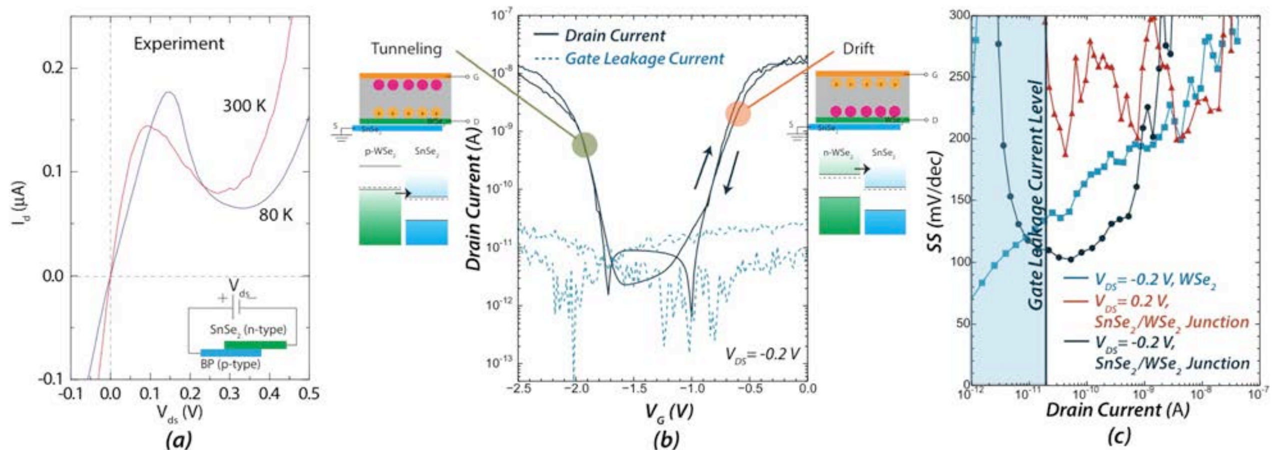

Figure 4: Experiments. (a) I_D-V_{DS} curves at 80 and 300 K for the BP/$SnSe_2$ vdW Esaki tunnel diode [11]; (b) Typical I_D-V_G curve at V_{DS}=-0.2 V for the WSe_2/$SnSe_2$ Thin-TFET. At more negative V_G, the transport mechanism is tunneling, while at less negative V_G, the transport mechanism is primarily thermionic emission and recombination; (c) Corresponding SS-I_D curves for the WSe_2/$SnSe_2$ Thin-TFET at V_{DS}=-0.2 V and V_{DS}=0.2 V, and for the parasitic WSe_2 MOSFET at V_{DS}=-0.2 V, SS values of the tunneling branch of the WSe_2/$SnSe_2$ Thin-TFET are significantly smaller than the other two. With improved device design and fabrication, <60 mV/dec is observed in our Thin-TFETs (not shown).

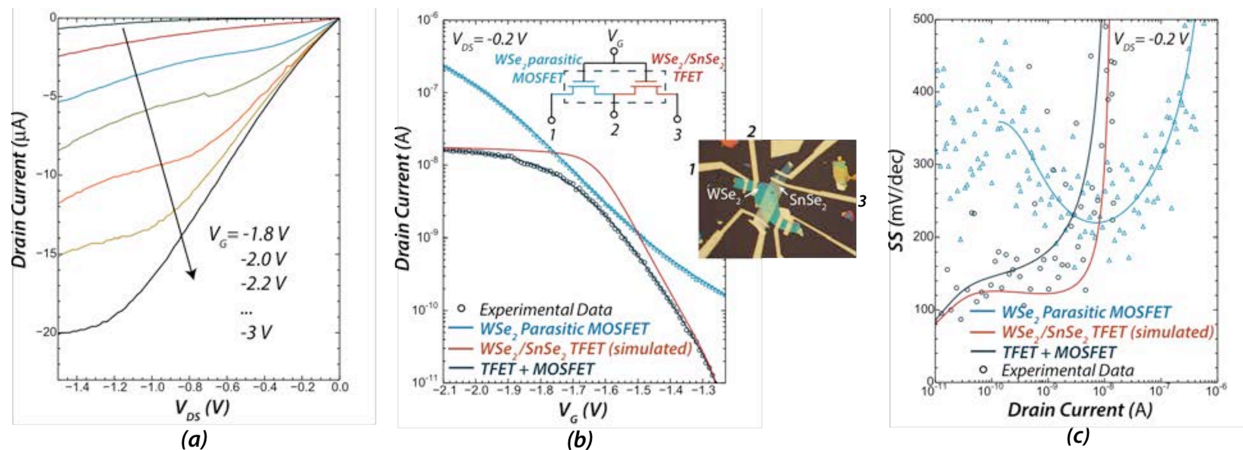

Figure 5: Experiments. (a) I_D–V_{DS} curves of the $WSe_2/SnSe_2$ Thin-TFET; (b) I_D–V_G curves of the measured WSe_2 parasitic MOSFET, the $WSe_2/SnSe_2$ Thin-TFET (TFET + MOSFET), and the intrinsic $WSe_2/SnSe_2$ TFET, the insets show the optical image of the device and the equivalent circuit with the parasitic MOSFET; (c) the corresponding SS curves for the parasitic MOSFET, the $WSe_2/SnSe_2$ Thin-TFET (TFET + MOSFET), and the intrinsic TFET.

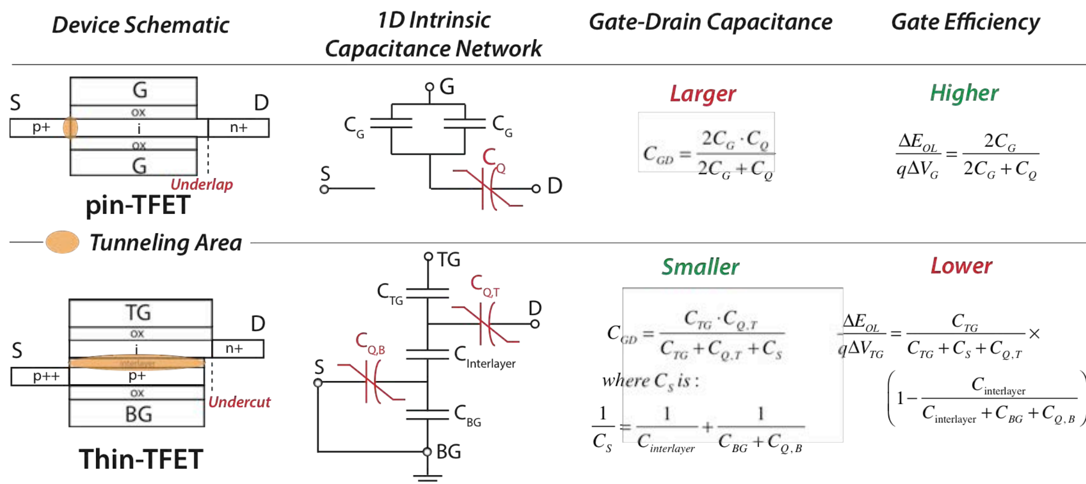

Figure 6: Comparison between pin-TFET and Thin-TFET: (Column 1) Device schematics with the tunneling area highlighted. Thin-TFET has a larger tunneling area, which can potentially render a higher tunnel current; (Column 2) 1D intrinsic capacitance networks; (Column 3 & 4) analytical expressions for C_{GD} and gate efficiency.

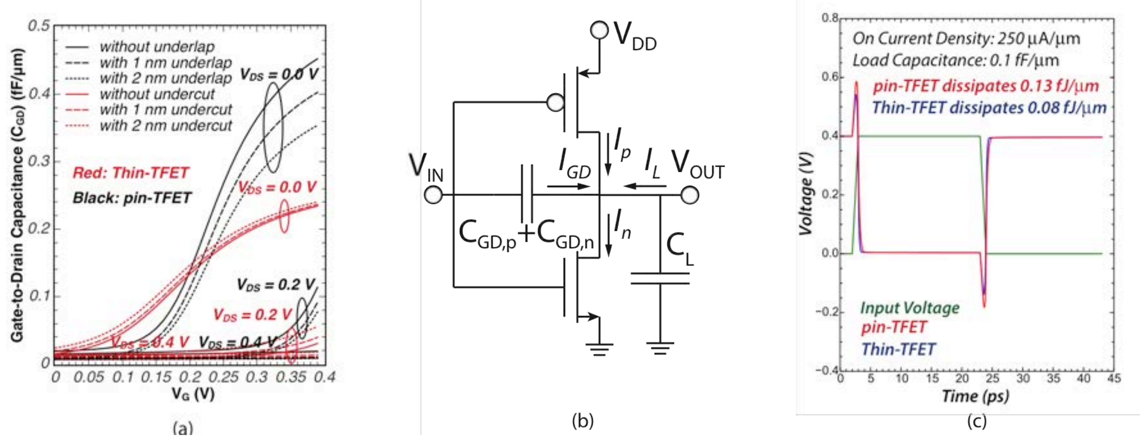

Figure 7: (a) C_{GD} versus the gate voltage (V_G) at different drain voltages (V_{DS}) for Thin-TFETs with various undercut lengths and pin-TFETs with various underlap lengths; (b) schematic of a complementary inverter based on TFETs; (c) time-dependent output voltage of the Thin-TFET inverter and the pin-TFET inverter.