GaN Vertical Nanowire and Fin Power MISFETs

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Introduction: GaN vertical power devices have many advantage over lateral device in device scaling, reliability and thermal management, etc. Traditional power transistors employ p-type pockets to achieve E-mode, RESURF and avalanche capabilities. However, this topology in GaN vertical power transistors has been challenging to implement [1] due to the difficulty to achieve selective area doping without compromising breakdown: p-type pockets in n-type regions or vice versa. The GaN UMOS-FETs or trench MOSFETs can be realized using epitaxial p-layers, however, suffer from low channel mobility in the inversion channel [2, 3]. Using n-type GaN only, depletion mode vertical MISFETs can be achieved with attractive current densities and breakdown voltages [4]. To get normally-off operation, Fin or nanowire (NW) pillars are necessary geometries. Compared with Fins, GaN nanowires have added advantages including superior electrostatic control and possibility for low-cost growth on foreign substrates [5, 6]. In this work, we report the first experimental demonstration of NW-MISFETs on bulk GaN substrates and compare them with Fin-MISFETs with the state-of-the-art performance fabricated on the same sample. The benefit of better electrostatic gate control in nanowire MISFETs are highlighted.

Device Epitaxy and Fabrication: The GaN epi structure is grown on bulk GaN substrates by MOCVD, consisting of a 7 μm n-GaN drift layer with a net donor concentration of ~6×10^{15} cm^{-3} (Fig. 1). The NWs and Fins are formed by a top-down approach: dry etch followed by a hot TMAH wet etch to form vertical side walls, first reported by Kodama et al. [2]. Images of fabricated NWs are shown in Fig. 2. The key device fabrication steps after the NW/Fin formation are shown in Fig. 3.

Results: The output characteristics of the Fin-MISFET are shown in Fig. 4. An on-current of 14 kA/cm^2 and R_{on} of 0.4 m$\Omega\cdot cm^2$ are extracted, which are on a par with the state-of-the art values reported in [4]. Fig. 5 shows the transfer characteristics of a Fin-MISFET with a single pillar and a NW-MISFET with 120 pillars. Due to the non-uniformity in NW fabrication, the off-state leakage of the NW-MISFET is higher than the single-pillar Fin device. The off-state characteristics of the Fin-MISFET under different gate-bias is shown in Fig. 6. Under more negative gate-bias, the breakdown voltage of the same device increases, reaching a highest value 513 V under V_{gs}=-15 V where the device undergoes a hard breakdown. This behavior is attributed to the drain induced barrier lowering (DIBL) effect. Due to the all-around gate geometry in NW-MISFETs, the electrostatic control of the channel is better. Thus, the NW-MISFET promises a higher and more stable breakdown voltage thanks to the suppressed DIBL effect. In addition, the NW geometry allows for a higher V_{th} than Fins of the same width (diameter for NWs). Using an abrupt depletion edge approximation, an analytical expression for the threshold voltage is derived for NWs:

$$V_{th} = V_{fb} - \frac{eN_d d_{NW}^2}{4\varepsilon_s} - \frac{eN_d d_{NW}^2}{2\varepsilon_{ox}} \cdot \ln\frac{d_{NW} + d_{ox}}{d_{NW}}$$

Fig. 7 shows the comparison of the calculated V_{th} of the Fin- and NW- MISFETs. When the Fin width (W_{Fin}) and the NW diameter (d_{NW}) are the same, V_{th} is always higher for NW-MISFETs, regardless of the insulator interface charge density. Due to the limited device yield, we are not able to get a good fit and a comprehensive comparison of the V_{th} between the two device geometries experimentally; nonetheless, this work represents the first attempt to use NWs on bulk GaN to curb DIBL-impacted breakdown behavior in vertical GaN power transistors.

Conclusion: Vertical NW-MISFETs on bulk GaN for power electronics have been fabricated and compared with the vertical GaN Fin-MISFETs with the state-of-the-art performance simultaneously fabricated on the same sample. DIBL effect is observed in the off-state characteristics, indicating the importance of gate-control in such devices. With the all-around gate geometry, the NW-MISFET has better electrostatic control, which promises higher BV and V_{th}. The added possibility of low-cost, bottom-up realization on foreign substrate makes GaN vertical NW-MISFET an attractive candidate for the new generation, high performance power devices.

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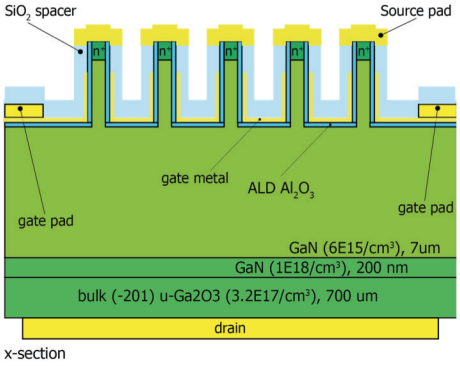

Fig. 1. Schematic of NW/Fin MISFETs.

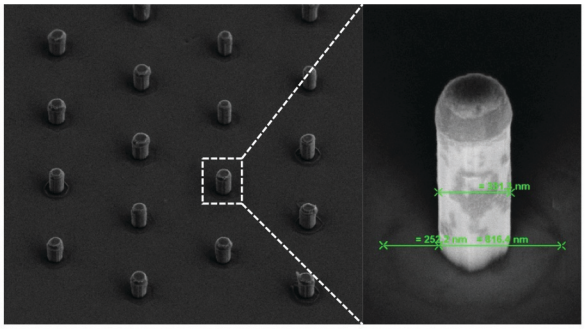

Fig. 2. SEM images of the GaN-on-GaN nanowires after dry etch and hot TMAH wet etch.

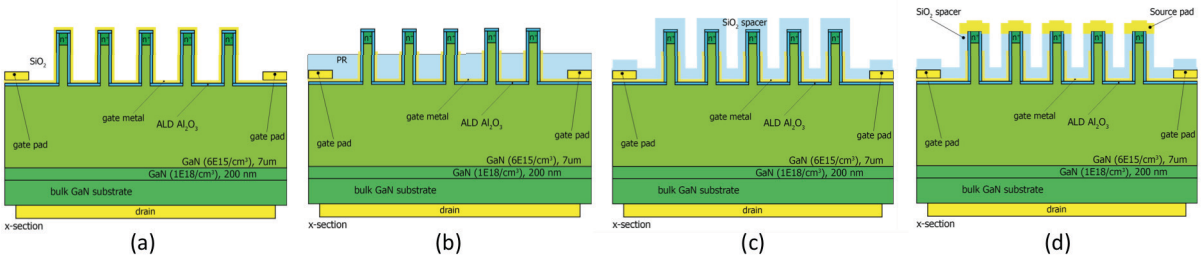

Fig. 3. Schematic of the key process steps after forming NWs/Fins. (a) ALD Al_2O_3 dielectric deposition and Cr gate sputtering after NW/Fin formation. (b) Photoresist (PR) planarization and thinning followed by gate metal etch. (c) SiO_2 spacer deposition and 2nd PR planarization. (d) Source pad metallization.

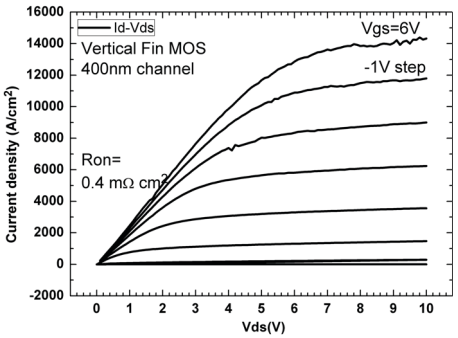

Fig. 4. Output characteristics of the vertical Fin-MISFETs.

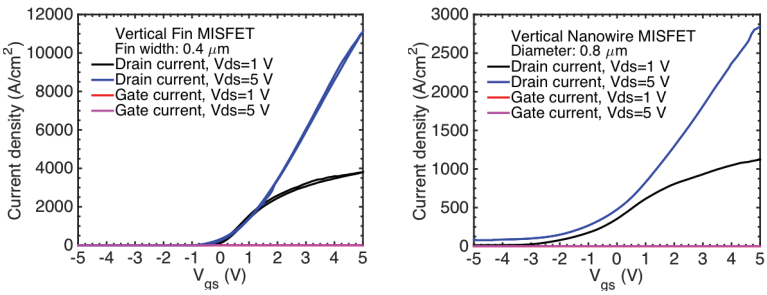

Fig. 5. Transfer I-V of the (a) Fin-MISFET, (b) nanowire-MISFET.

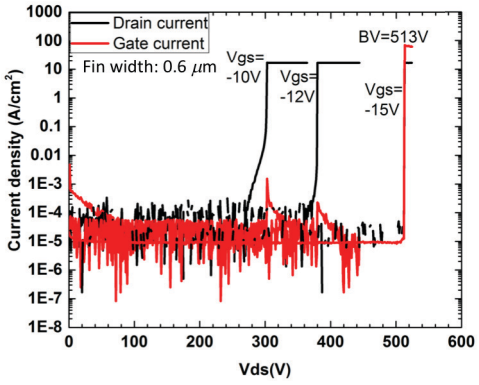

Fig. 6. Off-state characteristics of Fin-MISFETs under different gate bias.

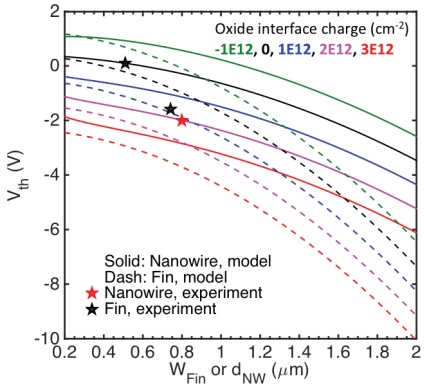

Fig. 7. Calculated V_{th} of the fabricated Fin- and NW-MISFETs, assuming a gate dielectric thickness of 50 nm and a doping concentration of $6x10^{15}$ cm^{-3}.

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