

Vertical Fin Ga₂O₃ Power Field-Effect Transistors with On/Off Ratio >10⁹

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Introduction. Recently, Ga₂O₃ has become an attractive material for both power electronic and optoelectronic device applications since large-size electronic-grade Ga₂O₃ substrates can be readily produced by melt-grown methods. Furthermore, high quality epitaxy and n-type doping schemes have been demonstrated [1, 2]. Due to its ultra-wide band gap (~4.5-4.9 eV), Ga₂O₃ is estimated to have a critical breakdown field >6 MV/cm, comparing favorably with ~3 MV/cm in SiC and ~4 MV/cm in GaN. This allows devices capable of handling large switching voltages. Devices such as lateral channel MOSFETs, MESFETs [3], MISFETs [4], nano-membrane FETs [5] and lateral FinFETs [6], vertical Schottky Barrier Diodes (SBDs) [7, 8], and deep-UV solar-blind photodetectors [9] have all been demonstrated using Ga₂O₃. Here, we report the first Ga₂O₃ vertical power transistors with a breakdown voltage (BV) of 185 V.

Device structure and fabrication. The devices are fabricated on commercially available unintentionally doped (UID) (-201) Ga₂O₃ substrates. First, Si ion implantation is applied to the top surface of the substrate, followed by an activation annealing, to facilitate ohmic contact formation [1]. Then, a metal hard mask is patterned using electron beam lithography (EBL) to define the fin channel with a fin width ranging from 200-400 nm. Subsequently, the vertical fins are formed using a BCl₃/Ar based dry etch [10], resulting a fin-pillar height of ~1 μm. A 50 nm Al₂O₃ gate dielectric is deposited using atomic layer deposition (ALD). The gate contact is then deposited, followed by a photoresist planarization and thinning process. A SiO₂ spacer layer is used to isolate the gate and source contacts. Finally, the source pad contacts are deposited and the devices are isolated. The gate length is estimated to be ~500 nm. **Fig. 1** shows the device schematic.

Results and discussion. MOS capacitor structures fabricated on the same sample are used to extract the net doping concentration in the UID Ga₂O₃ substrate, which is found to be ~10¹⁷ cm⁻³ extracted from the C-V measurements, as shown in **Fig. 2**. In **Fig. 3**, the family of I_d-V_{ds} and the transfer curve of I_d-V_{gs} are shown for a FinFET with a fin width of 400 nm. The output current density reaches >1 kA/cm², however, clearly exhibiting room for improvement if the ohmic contacts are improved. A high current on/off ratio >10⁹ is observed in the transfer I-V. The device also suffers from severe short channel effects due to the unfavorable electrostatic control: ~400 nm fin width, ~500 nm gate length and a channel doping concentration of 10¹⁷ cm⁻³; as a result, the drain current does not saturate well at high V_{ds}. The electrostatic control is much improved in the 200 nm wide devices (not shown). Thanks to the mitigated drain induced barrier lowering (DIBL) effects, a BV of >185 V was measured on devices with a fin width of 200 nm. A comparison between the drain and gate current (**Fig. 3d**) reveals that the breakdown in these devices is likely limited by the field crowding near the bottom of the fin; implementation of field plates should help improve BV, and further improvement is expected with a lower channel doping concentration.

Conclusions Vertical FinFET topology is an attractive option to realize Ga₂O₃ power switches due to the lack of p-type Ga₂O₃. Here we demonstrate promising results for the first time.

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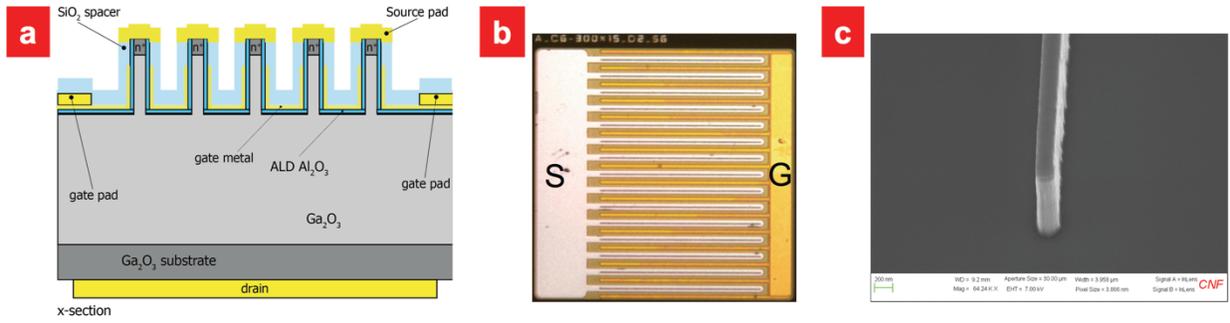


Fig. 1. Ga₂O₃ vertical Fin-FET power transistors. (a) Schematic cross section, (b) optical image of a finished device (top view), and (c) scanning electron microscopy image of a Ga₂O₃ fin on (-201) UID Ga₂O₃ substrate after dry etch.

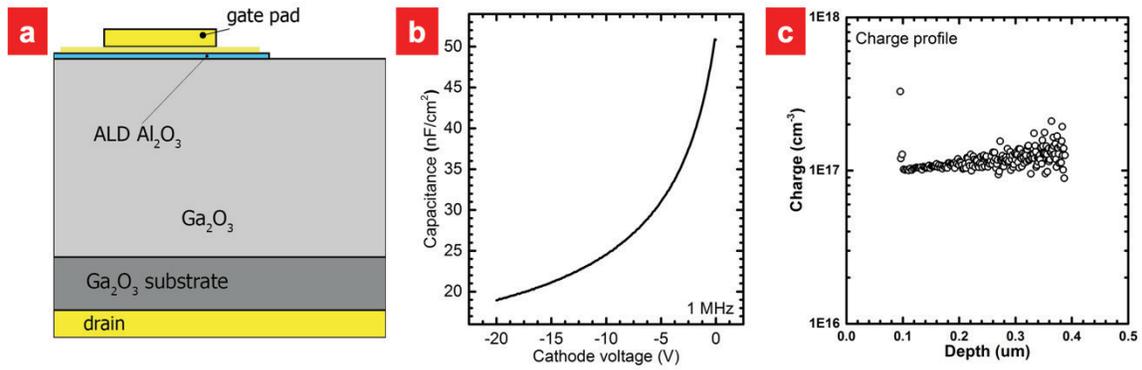


Fig. 2. (a) Ga₂O₃ MOS capacitor test structure, (b) C-V and (c) extracted net doping concentration profile in Ga₂O₃.

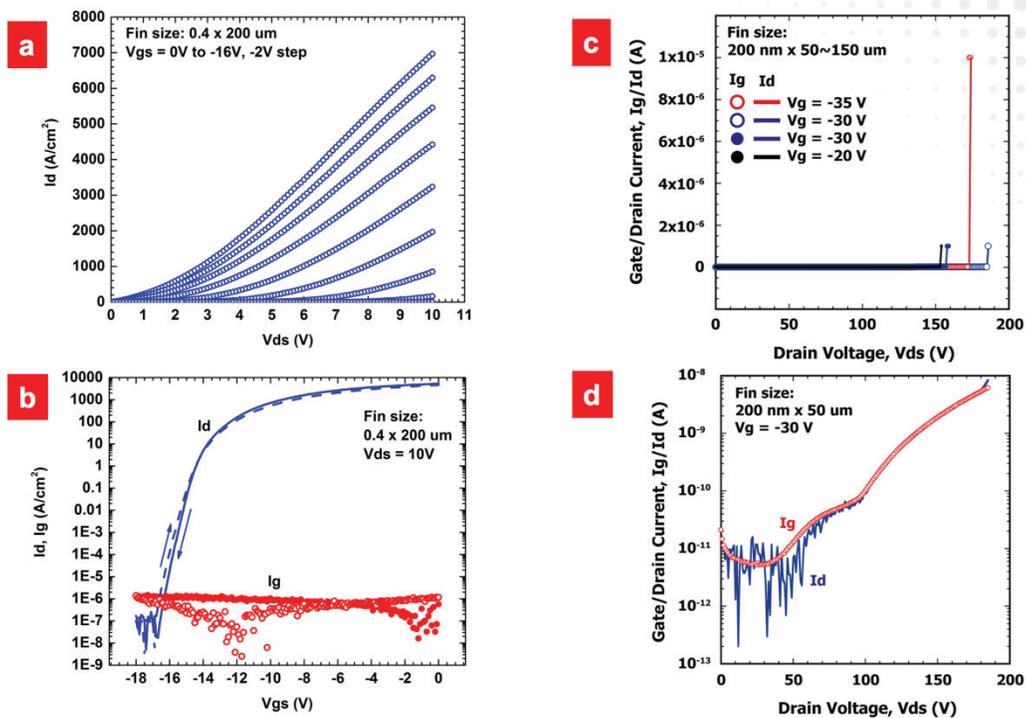


Fig. 3. Vertical Ga₂O₃ Fin-FET I-V characteristics, showing an on/off ratio >10⁹ and BV >185 V.