600 V GaN vertical V-trench MOSFET with MBE regrown channel

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Introduction: GaN vertical power transistors have gained increasing interest in recent years due to the advantages over lateral transistors in high voltage/high current applications. To date, two major topologies have been studied most: gate-on-epi-surface (GoE) and gate-on-sidewall (GoS). The GoE devices include CAVET [1] and VDMOSFET-like transistors [2, 3]. The GoS devices include U-MOS or trench-MOSFETs with inversion channel [4, 5] or regrown AlGaN/GaN semi-polar channel [6], as well as depletion-mode MISFET [7]. The vertical MISFET is the simplest to fabricate, however, it does not have avalanche capabilities inherently besides being difficult to achieve sufficiently large V_{th}. It is easier for trench MOSFETs to achieve normally-off operation, high breakdown voltage (BV) and small footprint. However, it is challenging to achieve high mobility in the inversion channel. In contrast, CAVETs, VDMOS-like transistors and PolarMOS [3] utilize high mobility AlGaN/GaN channel to achieve low R_{on}, but the channel regrowth posts challenges in achieving low off-state leakage in un-gated regrowth interface. Recently, a novel design based on trench MOSFET is realized by MOCVD regrowth of a thin GaN interlayer [8]. Low R_{on} and high BV is achieved in the gated regrown channel. Similar to the other MOCVD regrown devices, the buried Mg-doped p-GaN needs to be re-activated by exposing the p-GaN surface during high temperature anneal. This leads to high thermal budget and poses limitations on device geometry. Furthermore, any incomplete activation of buried p-GaN leads to reduced BV. In this work, we design a V-shaped trench MOSFET with MBE regrown UID GaN channel. ~600 V breakdown voltage with normally-off operation is demonstrated without the need for re-activation of the buried p-GaN. *To our knowledge, this is the highest BV achieved in GaN vertical transistors with MBE regrown channel.*

Experimental process: The starting epitaxial structure is similar with our previous high voltage p-n diodes grown by MOCVD [9] (Fig. 1). The schematic of the device is shown in Fig. 2, which consists of a MBE regrown UID GaN channel covering the sidewall of the V-shaped trench. The conformal gate ensures field-control of the regrown channel as well as the possible charge typically present at the regrowth interface. Smooth surface morphology of the regrown GaN at the trench bottom is observed with clear atomic steps (Fig. 3). The fabrication steps are shown in Fig. 4. A tapered trench is etched using our low damage Cl-based ICP recipe with SiO_2 as mask. The sidewall angle is measured to be 43°. In order to reduce impurity concentration at the etched surface, a combination of UV-ozone cleaning and HF+HCl wet etch is performed before loading into the MBE chamber, where 50 nm UID GaN is regrown. A patterned n^+-GaN regrowth is then performed for ohmic contact purpose. Since MBE chamber has no hydrogen-containing reactants, the buried p-GaN remains activated. The 30 nm Al_2O_3 gate dielectric is deposited by ALD.

Results: The transfer curve of a single finger device at V_{ds} = 10 V is shown in Fig. 6. On-off ratio of 10^9 and normally-off operation with a threshold voltage of ~16 V is achieved. The output characteristics in Fig. 7 show good saturation behavior and an on-current of ~18 A/cm^2 (normalized by the trench area) at V_{gs} = 25 V. R_{on} is determined from the linear region to be 0.3 $\Omega \cdot$ cm^2. The relatively poor R_{on} and I_{on} is determined to be limited by the lateral portion of the regrown channel from gated-TLM measurement (Fig. 5). We found the sheet resistance of the lateral regrown channel to be ~2 M$\Omega/\square$ at V_{gs} = 25 V. Since the lateral channel length $L_{g,lateral}$ is 3 ~ 4 μm in the measured device, R_{on} is dominated by the lateral channel. The high resistivity of the lateral regrown channel is likely due to the carrier compensation by Mg diffusion from the p-GaN underneath [10]. A thicker UID channel or growing a thin n^+-GaN counter layer before the channel regrowth could improve the channel conductivity dramatically and is being investigated. The off-state characteristics in shown in Fig. 8. Low drain leakage and a breakdown voltage of 596 V is measured with V_{gs} = −15 V, indicating good quality of the regrowth p-n junction interface.

Conclusion: Record high 600 V BV is achieved among GaN vertical transistors with MBE regrown channel. No additional activation annealing of the buried p-GaN is needed, allowing for lower thermal budget and more flexible device geometry than MOCVD regrowth. The device R_{on} and I_{on} is limited by the lateral channel, which can be dramatically boosted by reducing the Mg compensation using a thicker lateral channel or an n^+ counter layer.

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[1] S. Chowdhury, et al., IEEE-EDL, vol. 29, p. 543, (2008).
[2] H. Nie et al., IEEE-EDL, vol. 35, p. 939, (2014).
[3] H. Xing et al., DRC, p. 51, (2015).
[4] T. Oka et al., Appl. Phys. Exp., vol. 8, p. 054101, (2015).
[5] R. Li et al., IEEE-EDL, vol. 37, p. 1466, (2016).
[6] D. Shibata et al., IEEE-IEDM, pp. 10-1, (2016).
[7] M. Sun et al., IEEE-EDL, vol. 38, p. 509, (2017).
[8] C. Gupta et al., IEEE-EDL, vol. 38, p. 353, (2017).
[9] Z. Hu et al., Appl. Phys. Lett., vol. 107, p. 243501, (2015).
[10] H. Xing et al., Jap. J. Appl. Phys., vol. 42, p. 50, (2003).

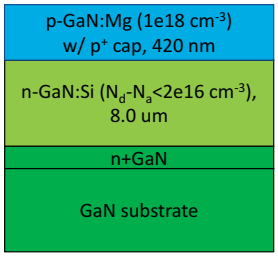

Fig. 1: Epitaxial structure grown by MOCVD.

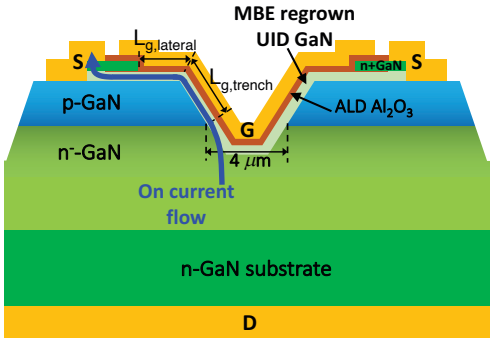

Fig. 2: Schematic device structure of the GaN V-trench MOSFET. The total gate length over the regrown channel: $L_{g,tot} = L_{g,lateral} + L_{g,trench}$.

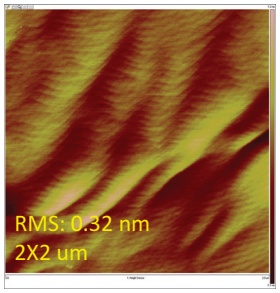

Fig. 3: AFM surface morphology of the MBE regrown GaN at the trench bottom.

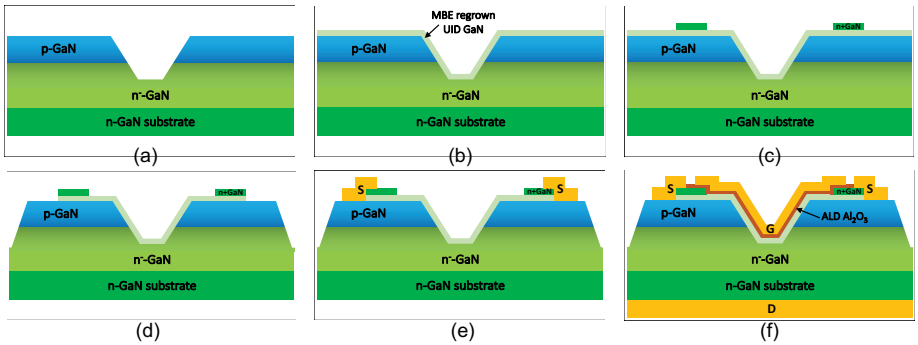

Fig. 4: GaN V-trench MOSFET fabrication process: (a) tapered trench etch; (b) MBE channel regrowth; (c) n^+-GaN patterned regrowth; (d) dry etch for p-GaN body contact and device isolation; (e) source ohmic contact (Ti/Au) and body contact (Pd/Au) metallization; (f) ALD of 30 nm Al_2O_3 gate dielectric, followed by gate (Ni/Au) and drain (Ti/Au) electrode metallization.

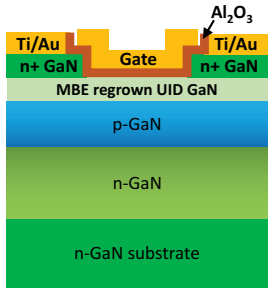

Fig. 5: Schematic cross-section of the gated TLM structure for the lateral regrown channel.

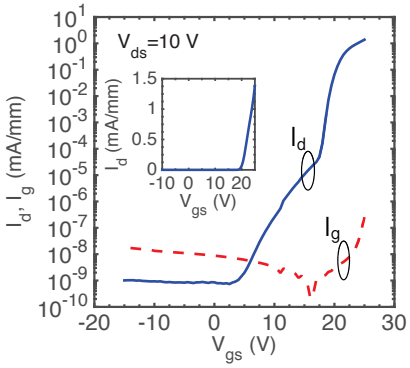

Fig. 6: Transfer I-V of a single finger GaN V-trench MOSFET at $V_{ds} = 10$ V.

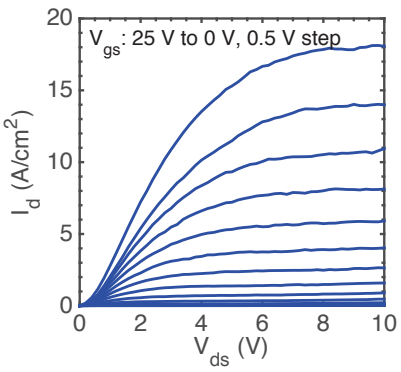

Fig. 7: Output characteristics. Current is normalized by the total trench area (4×50 μm).

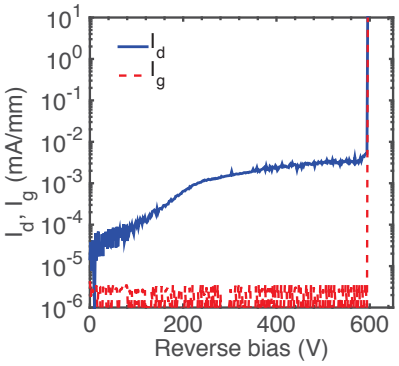

Fig. 8: Off-state characteristics at $V_{gs} = -15$ V.

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