Wide-bandgap Gallium Nitride p-channel MISFETs with enhanced performance at high temperature

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Overview

Wide-bandgap materials, particularly Gallium Nitride, have emerged as the platform underlying many of the most promising technologies in the high-power and high-frequency domain. However, GaN p-channel devices lag far behind their popular n-channel counterparts, due to lower mobilities as well as difficulties in doping and forming ohmic contacts. There is a strong need for wide-bandgap p-channel FETs – this missing piece would enable energy-efficient, high-voltage CMOS electronics, a critical technique for on-chip power conditioning and management.

Researchers have produced p-channel FETs from several epitaxial III-Nitride structures, including AlGaN/GaN [1], GaN/AlN [2], AlInGaN/GaN [3, 4] and InGaN/GaN [5]. As part of a comparison of potential pFET candidates, we have grown, fabricated, and characterized a series of Gallium Nitride p-channel metal-insulator-semiconductor field-effect transistors (p-MISFETs) on Silicon Carbide. To the author's knowledge, these are the first p-MISFETS – that is, p-channel devices relying only on three-dimensional space charge rather than a two-dimensional hole gas – reported in Gallium Nitride. Such devices provide both a baseline against which p-channel HFET structures can be compared and an independent path toward an effective high-voltage pFET solution.

Experiment

Mg-doped p-GaN epilayers were grown by Plasma-Assisted Molecular Beam Epitaxy in a Veeco GENxplore system under metal-rich conditions. The epitaxial structure includes a 100 nm nominally undoped buffer, followed by 200 nm of moderately p-doped GaN and 10 nm of a heavily p-doped GaN contact layer. After device mesa isolation, Pd ohmic contacts are deposited at source and drain and used as a mask to ICP etch the p+ GaN and a variable amount of the p-GaN channel. The device is then coated with 11 nm of ALD aluminum oxide dielectric before a Ti/Au gate is deposited. The resulting device structure is shown in Figure 1a & b. A representative band diagram is plotted in Figure 1c to show how the gate controls the channel charge via manipulation of the depletion width.

On the processed samples, TLM measurements demonstrated ohmic contacts with $R_c = 155\ \Omega \cdot \text{mm}$ ($\rho_c = 1.5 \times 10^{-3} \Omega \cdot \text{cm}^2$). Temperature-dependent Hall measurements were performed up to 460 K to characterize the Mg doping. Extraction of the doping density, compensation ratio, and "inherent" acceptor level (in the sense of [6]) are shown in Figure 1d. I-V characteristics were measured up to 400 K (see Figure 2), notably improving with increasing temperature. Room temperature on-currents of 1.8 mA/mm for a L_g=1.5um, L_{sd}=5.2um device are competitive with several of the 2DHG-based candidates [1, 5]. Device characteristics are well-described by an analytic long-channel incomplete-ionization MISFET model embedded in empirical contact resistances; comparisons between the model and experiment are shown for multiple temperatures in Figure 2 and for varied geometries in Figure 3. MISFET modelling parameters related to doping/compensation are consistent with the relations extracted from Hall measurements so that Figures 1d and 2 represent two different extractions of the same phenomena. Meanwhile Figure 3 demonstrates that the model suitably captures the geometrical dependencies of the pinch-off voltage and on-current.

Discussion

This analysis makes clear how the depth of the Mg acceptor level in GaN affects MISFET design, whereby the full concentration of uncompensated acceptors controls the electrostatics but the only the ionized acceptor concentration contributes holes to transport. By increasing the temperature, more acceptors are ionized, and carrier transport improves. The MISFET design concerns developed in this work naturally frame many of the trade-offs involved in heterostructure/modulation-doped approaches. Finally, given that current densities will increase with scaling and improved process control, these results indicate that attractive pFET device performance for high-voltage CMOS can be acheived on a GaN platform.

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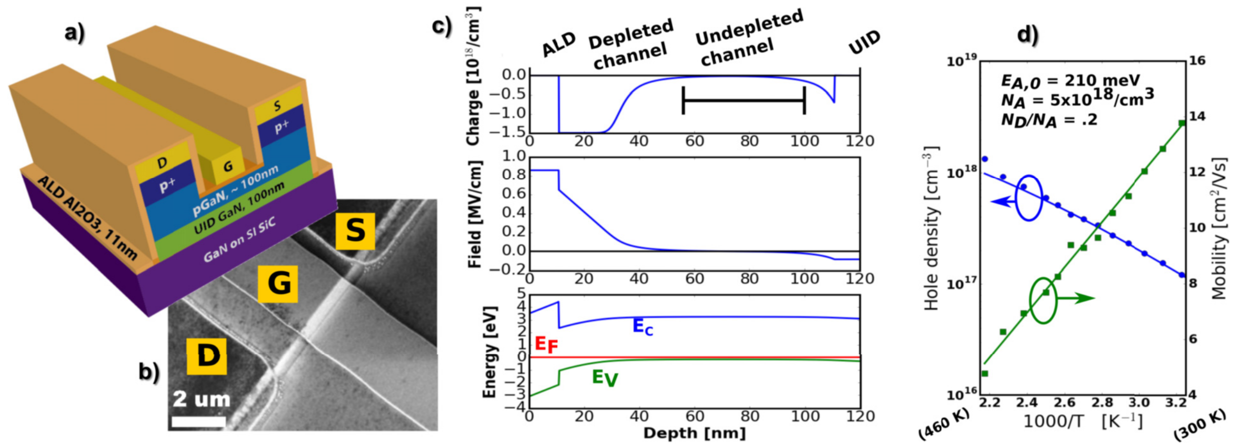

Fig. 1: (a) The MISFET structure is formed from a variably-recessed pGaN layer on UID GaN. (b) SEM of the processed device. (c) Equilibrium charge/field/band diagram (d) Hall measurements and model fits: hole density was modelled by Eq 1 and 3 of [6] (note that $E_{A,0} \neq E_A$). Mobility was linearly regressed to $\mu[\mathrm{cm}^2/\mathrm{Vs}] = -12.5 + 8124/T[\mathrm{K}]$.

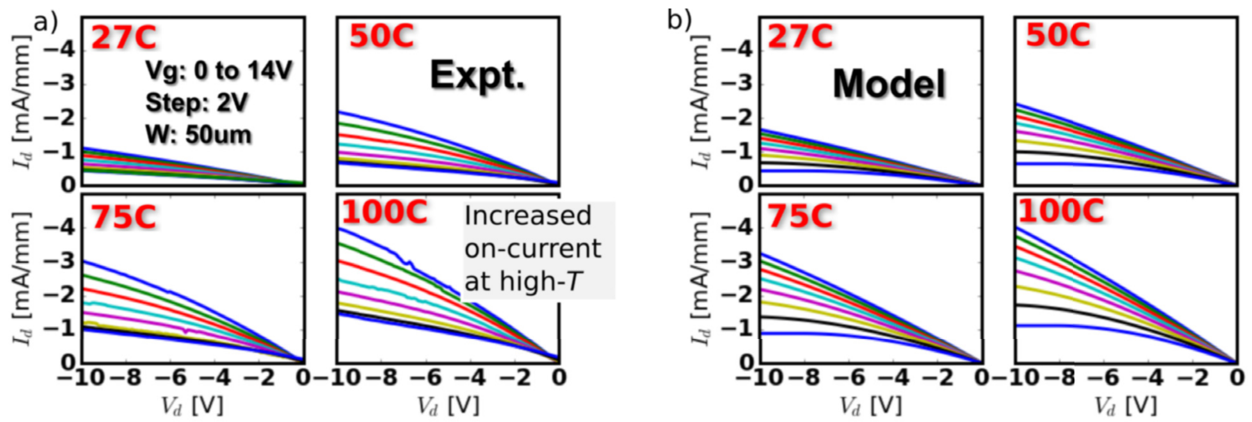

Fig. 2: (a) Measured and (b) modelled Id-Vd characteristics (solid lines) at higher temperatures show markedly improved device performance due to unfreezing of the Mg acceptors.

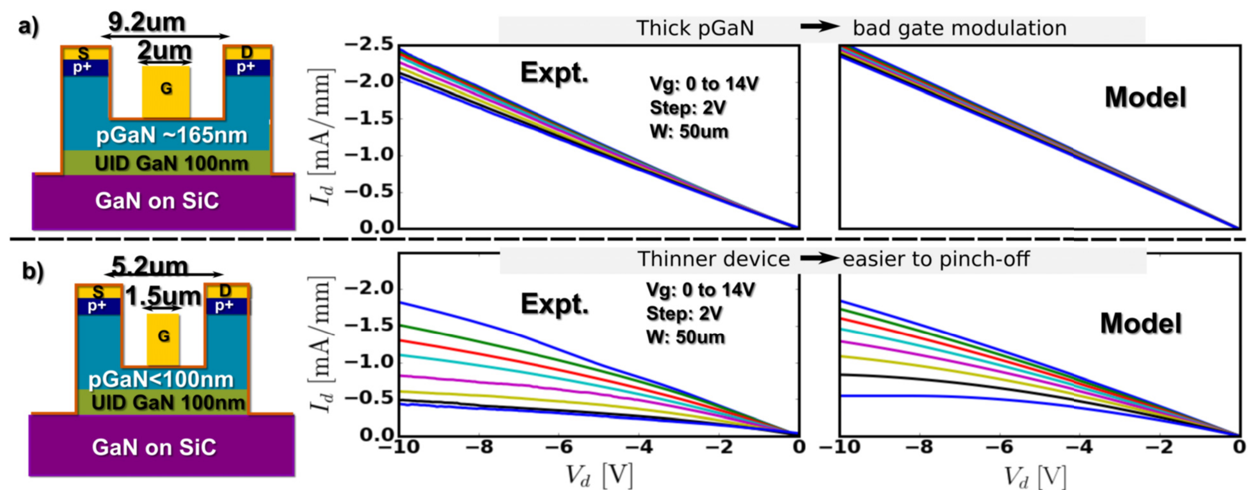

Fig. 3: Comparitive Id-Vd characteristics of two devices with different recessed pGaN thicknesses and gate lengths. Greater recess depth reduces the pinch-off voltage magnitude, improving gate control (but reducing on-current). Shorter gate length (and source-drain lengths) in the second device, tending to increase on-current, mitigate this reduction.

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