Realization of the First GaN Based Tunnel Field-Effect Transistor

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Tunnel field-effect transistors (TFETs) offer the means to surpass the subthreshold swing (SS) limit of 60 mV/dec that limits MOSFETs. While MOSFETs rely on modulating a potential barrier, which is subject to a Boltzmann tail in the density of states (DOS), interband tunneling in TFETs enables a sharp turn off of the DOS because the transport is no longer governed by an exponential tail of carriers. These devices have been investigated in Si & III-V material systems[1], achieving SS's as low as 20 mV/dec[2]. GaN is advantageous to these other material systems because its large bandgap is ideal for suppressing leakage current. Unfortunately impurity doping in GaN alone is not enough to achieve the internal fields required to promote interband tunneling**[Fig 1(a)]**. However, by taking advantage of the difference in polarization fields between InGaN and GaN, a device structure favoring interband tunneling can be made **[Fig 1(b)]**. Li et. al.[3] have theoretically predicted that a GaN heterojunction TFET could obtain an SS of 15 mV/dec and a peak current of $1x10^{-4}$ A/μm. For the work being presented, GaN TFETs were fabricated using a surrounding gate (SG) architecture utilizing both nanowires and fins formed from a top-down approach.

The devices were grown using plasma assisted MBE on bulk n-type metal polar GaN substrates. Separate effusion cells supplied the metal atoms (Ga, In) while a plasma source provided the active N. Growth began with a buried n^+/p tunnel contact to the p-GaN source layer, followed by 5nm of $In_xGa_{1-x}N$ (x: 25%), a UID GaN channel and an n-GaN drain. **[Fig 1(c)]** shows the resulting energy band diagram for the on and off state. Fabrication of the GaN nanowires was realized by a two-part dry-wet etch. After patterning, RIE-ICP was used to define the wire/fin height, followed by a wet etch in hot (90 °C) AZ400 which resulted in fins and wires with m-plane sidewalls. Al_2O_3 gate dielectric was conformally deposited through ALD. Gate metal (Cr) coverage was accomplished using sputtering, while source and drain contact pads were formed from e-beam evaporation **[Fig. 2 (a)]**. Contact to the p-GaN source was achieved through a backside tunnel contact utilizing the n^+-doped substrate.

Selective wet etch of the GaN pillars is possible due to the OH^- ions in the AZ400. For Ga-polar GaN, the the electronegativity of the c-plane insures that only the side walls are etched. The result is an etch rate of 12nm/min for sidewalls, allowing for wire diameters < 40nm. Due to its electropositivity, c-plane N-face GaN does not benefit from this selectivity, limiting this process to metal polar devices. Cross-sectional TEM **[Fig 2 (b)]** shows that the top down process results in devices that perfectly matched to **Fig 2 (a)** thanks to the wet etch.

Fig 3(a) shows the resulting transfer characteristic at room temperature for a GaN TFET. In this device, gate leakage is sufficiently suppressed, remaining >100x lower than the drain current in forward bias. From this plot, a SS of 109 mV/dec is calculated, which is maintained over 2 orders of drain current **[Fig 3(b)]**. One reason for these devices' inability to go below the 60 mV/dec limit is trap assisted tunneling. Prior work in III-V based TFETs proved this to be a common bottleneck[4]. **Fig 3(a)** also highlights two major advantages of using a wide bandgap material: low off state leakage current and the suppression of ambipolar current flow, which is a concern in most Si and III-V based TFETs. The family curves for the same device can be seen in both the linear **[Fig 4(a&c)]** and semilog plot **[Fig 4(b)]**. For the current regime dominated by interband tunneling ($V_{DS} > 0$ V, $V_{GS} > 0$ V), the drain current clearly saturates, a strong sign that the device is operating as an FET. Based on the stepped gate voltage steps, the threshold voltage is found to be ~0.4 V, which agrees with the I_DV_{GS} measurement. The measured current densities are far lower than the ~mA/μm range desirable for an attractive TFET, but not far from the theoretical predictions for this heterostructure and geometry, implying a clear model-driven path towards their improvement.

In conclusion, we have fabricated the world's first nanowire and fin based GaN TFET using a two-step dry-wet etch process. The lowest measured SS was 109 mV/dec at room temperature, with the device showing current saturation indicative of FET behavior. Trap assisted tunneling is the main candidate for the limited SS and will be explored with future temperature dependent IV measurements. The realization of TFETs in the III-N material system opens up an exciting new frontier of low power switching that is capable of operating at high frequencies while maintaining low leakage currents in the widest bandgap semiconductors taking advantage of polarization discontinuities.

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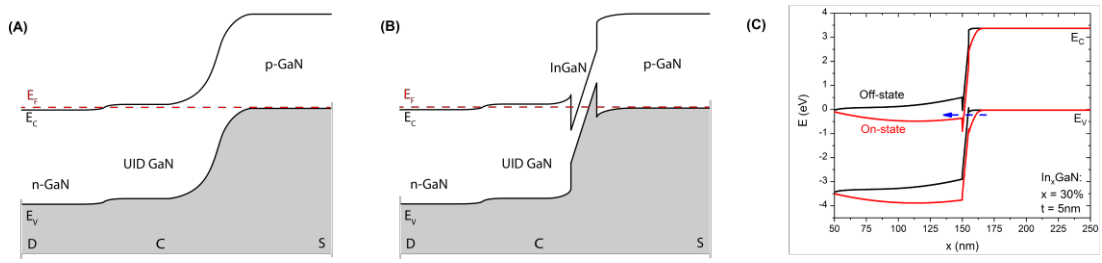

Fig. 1. (a) & (b) Energy band diagrams of GaN homo- and hetero- tunnel junctions respectively. Inclusion of InGaN reduces tunneling distance and increases the electric field. (c) Simulated energy band diagrams for the on and off state of a GaN heterojunction TFET

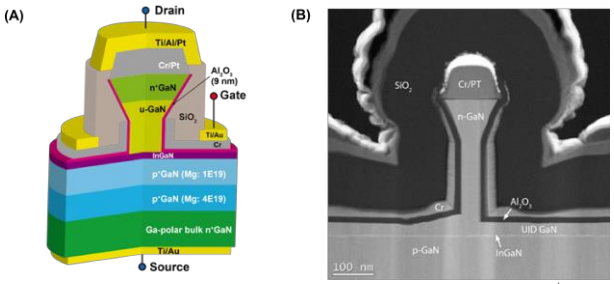

Fig. 2. (a) Schematic cross-section of the designed GaN TFET device. A buried n^+/p tunnel junction of large area is used to make a low-resistance ohmic contact to the buried p-type source layer. Cr/Pt metal is left over from the dry-wet process. (b) TEM cross-section image of the fabricated TFET. A golf-tee structure is formed due to Cr/Pt metal.

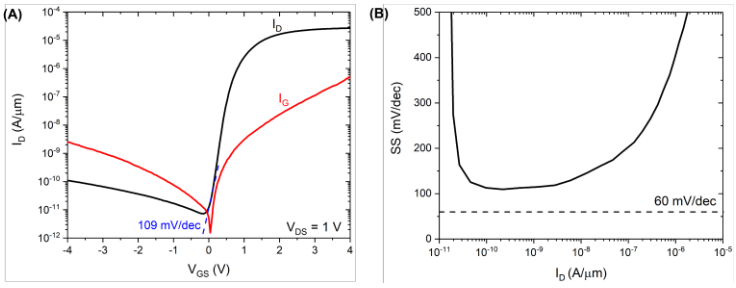

Fig. 3. (a) The measured transfer curve for 75nm wide GaN fin-TFET at 300 K. The minimum SS achieved is 109 mV/dec for an applied V_{DS} of 1 V. (b) The measured subthreshold swing versus drain current, extracted from Fig 3(a). While the SS is not below the thermal Boltzmann limit, the low SS is maintained over 2 orders of magnnitude.

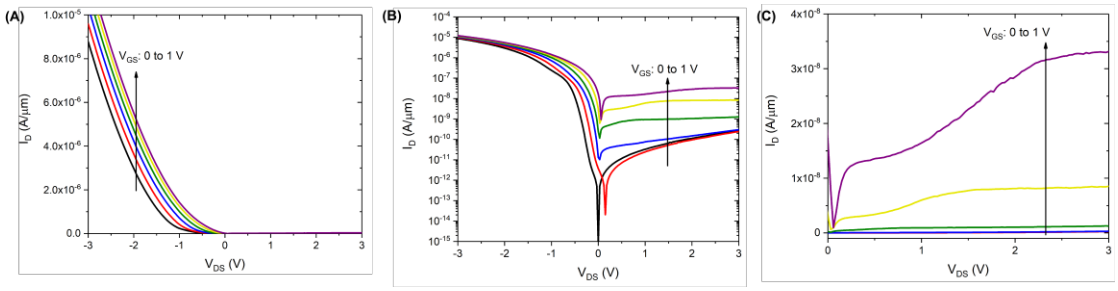

Fig. 4. Family curves for 75nm wide fin TFET. (a) The measured linear I_D-V_{DS} curves of the GaN TFET. While the current densities are much smaller than the desirable mA/μm range, it nevertheless is close to the theoretically predicted values for these heterostructures and device geometries. (b) Semilogarithmic plot of the same family curves. Because of the non-degenerate p-type doping of GaN, NDR characteristics are not observable in the reverse bias conditions, as is the case for InGaAs TFETs. (c) Close up, linear plot of the forward bias conditions. Due to tunneling, the drain current is 10x less than the thermally generated current in the reverse bias. Nevertheless, the drain current in the TFET mode saturates as desired.

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