

Breakdown mechanism in 1 kA/cm² and 960 V E-mode β -Ga₂O₃ vertical transistors

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A high current density of 1 kA/cm² is experimentally realized in enhancement-mode Ga₂O₃ vertical power metal-insulator field-effect transistors with fin-shaped channels. Comparative analysis shows that the more than doubled current density over the prior art arises from a larger transistor channel width; on the other hand, a wider channel also leads to a more severe drain-induced barrier lowering therefore premature transistor breakdown at zero gate-source bias. The observation of a higher current density in a wider channel confirms that charge trapping in the gate dielectric limits the effective field-effect mobility in these transistor channels, which is about 2× smaller than the electron mobility in the Ga₂O₃ drift layer. The tradeoff between output-current density and breakdown voltage also depends on the trap density. With minimal trap states, the output current density should remain high while breakdown voltage increases with decreasing fin-channel width. Published by AIP Publishing. <https://doi.org/10.1063/1.5038105>

Gallium oxide is one of the most important new semiconductor materials for high-power applications. With an experimentally reported critical electric field up to 5.2 MV/cm,^{1,2} an electron mobility of 100–150 cm²/V s (Refs. 3–5) and low-cost high-quality substrates⁶ and epitaxial layers,^{7–9} β -Ga₂O₃ promises high-voltage and high-power devices with performance at least comparable to those of SiC and GaN. Ga₂O₃ device technologies have advanced fast in the past 5 years and various lateral channel Ga₂O₃ transistors including nano-membrane field-effect transistors (FETs),^{10,11} FinFETs¹² and MOSFETs¹³ have been developed.

Vertical Ga₂O₃ power devices including power diodes and transistors have great potential in high-power applications. High-voltage Schottky Barrier Diodes (SBD)¹⁴ and heterojunction p-n diodes¹⁵ with breakdown voltage (*BV*) >1000 V have been demonstrated. The first three vertical Ga₂O₃ transistors were reported in 2017 albeit showing no pinchoff or low *BVs*.^{16–18} Very recently, we demonstrated the first kV vertical Ga₂O₃ transistors employing vertical fin-shaped channels (FinFETs); more importantly, these transistors are normally off, i.e., enhancement-mode (E-mode).¹⁹ E-mode operation is a desired feature for power transistors since it allows less complicated circuit designs and fail-safe operation under high voltages. Early successes in demonstrating E-mode Ga₂O₃ FETs are in lateral devices.^{11,12,20,21} On the other hand, the vertical-FinFET topology allows strong gate electrostatic control by double gating of the channel; the ungated access region between the gate and source thus the transistor source resistance can be minimized while employing a thick drift layer to sustain high voltages, which in turn enables high output currents and high breakdown

voltages simultaneously. Such features have been successfully proven in SiC²² and GaN.²³ However, the output current density in our recent demonstration in Ga₂O₃ is significantly lower than expected.

In this work, we investigate Ga₂O₃ vertical power FinFETs, i.e., vertical power metal-insulator FETs (MISFETs), with a wider fin channel of 0.44 μ m than our previous work (0.33 μ m).¹⁹ We analyze the tradeoff between the output current density and drain-induced barrier lowering (DIBL) thus premature breakdown in these devices, in particular, the impact on this tradeoff from the dielectric/channel interface states. DIBL, a type of short channel effects, has adverse impacts on threshold voltages (*V*_{th}) and high-frequency performance of ultra-scaled transistors.²⁴ High-power transistors usually do not suffer from high DIBL due to relatively large gate length to channel width aspect ratio; thus, device breakdown is induced by channel avalanche or gate leakage. However, under high operation voltages of hundreds to kilos of volts, *V*_{th} shifts may be significant, which could lead to *V*_{th} roll-off from E-mode to depletion-mode at high *V*_{ds}. As a result, some E-mode transistors achieve highest *BVs* under negative gate bias.^{25–27} In addition, power transistors usually have thick gate dielectrics for suppression of gate leakage currents. The dielectric/channel interface states may lead to extra DIBL that requires careful analysis.

The wafer structure contains a 10 μ m epitaxial layer with a target Si concentration of 2×10^{16} cm⁻³ grown by halide vapor phase epitaxy (HVPE) on n-type bulk β -Ga₂O₃ (001) substrates (*n* $\sim 2 \times 10^{18}$ cm⁻³). The schematic device structure is shown in Fig. 1. Key components of the device include n+ ion-implanted top-source and back-drain contacts using Si as donors, a vertical fin-shaped FET channel defined

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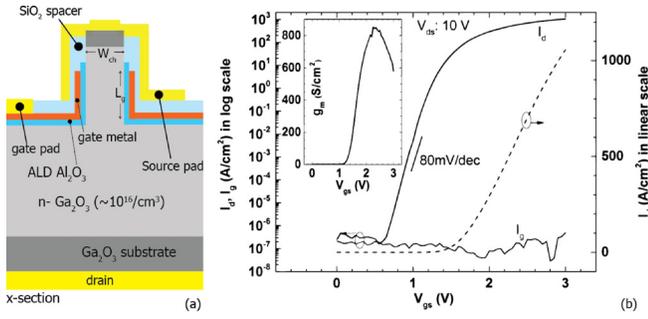


FIG. 1. (a) Schematic cross sections of a Ga_2O_3 vertical power FinFET or MISFET. (b) $I_d/I_g - V_{gs}$ transfer characteristics of a vertical Ga_2O_3 power FinFET in the semi-log and linear scale, along with the extracted subthreshold slope. Inset: transconductance at $V_{ds} = 10$ V.

by dry etching, a 30 nm thick Al_2O_3 gate dielectric deposited by atomic layer deposition (ALD), a 50 nm thick sputtered Cr gate metal, and a 200 nm SiO_2 spacer separating the source and gate electrodes. The details of device fabrication can be found in Ref. 17. Devices with a channel width (W_{ch}) of both 0.44 μm and 0.33 μm were fabricated, and the vertical gate length (L_g) for all devices is 0.80 μm , as confirmed by measurements using scanning electron microscope (SEM).

C-V measurements on vertical MIS capacitor structures reveal a charge concentration $N_d - N_a$ of $1.2 \times 10^{16} \text{ cm}^{-3}$ in the top $\sim 1 \mu\text{m}$ and a gradual transition to $\sim 1 \times 10^{15} \text{ cm}^{-3}$ in the deeper epitaxial region.¹⁹ Devices with a W_{ch} of 0.33 μm show characteristics similar to what were reported in Ref. 19. For the vertical power FinFETs with $W_{ch} = 0.44 \mu\text{m}$, the $I_d - V_{gs}$ transfer curves in linear and semi-log scales are shown in Fig. 1(b). A high current on/off ratio of $\sim 10^9$ and an on-current of $> 1 \text{ kA/cm}^2$ (normalized to the area of the source contact) is measured, which is $\sim 2.5 \times$ of that in the 0.33 μm devices.¹⁹ The subthreshold slope (SS) is extracted as $\sim 80 \text{ mV/dec}$ near the drain current of 1 mA/cm^2 . Since the SS of a MOSFET is written as²⁸

$$SS = \frac{kT}{q} \ln 10 \cdot \left(1 + \frac{C_d + qD_{it}}{C_{ox}} \right), \quad (1)$$

where k is the Boltzmann constant, T is the temperature, q is the elementary charge, C_d is the depletion capacitance of the channel (in the sub-threshold region, $C_d \sim 0$ in double-gated junctionless MISFETs including FinFETs), C_{ox} is the capacitance per unit area associated with the gate dielectric, and D_{it} the interface state density. We can thus estimate D_{it} to be $> 6 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. This value is comparable to a few other reports on interface state extraction using Ga_2O_3 MOS capacitors.^{29,30} V_{th} extracted by linear extrapolation of the drain current is $\sim 1.6 \text{ V}$. Alternatively, if we use a criterion of $I_d = 1 \text{ mA/cm}^2$, V_{th} is determined as $\sim 0.94 \text{ V}$ at $V_{ds} = 10 \text{ V}$. For the rest of the discussion, we choose to use the latter V_{th} criterion for convenience of the DIBL analysis. The peak g_m at $V_{gs} = 2.25 \text{ V}$ and $V_{ds} = 10 \text{ V}$ is $\sim 850 \text{ S/cm}^2$.

The family of $I_d - V_{ds}$ curves of the same vertical FinFET is shown in Fig. 2. The drain current density reaches $\sim 750 \text{ A/cm}^2$ with a V_{gs} of 3 V and a V_{ds} of 10 V. This magnitude of I_d is lower than that in the transfer $I - V$ due to device self-heating and D_{it} . The differential on-resistance R_{on} calculated near $V_{ds} = 0 \text{ V}$ is $\sim 7 \text{ m}\Omega \text{ cm}^2$. The transistor shows a

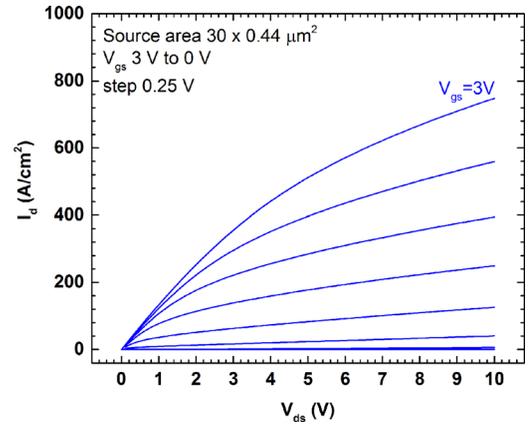


FIG. 2. $I_d - V_{ds}$ characteristics of a vertical Ga_2O_3 power FinFET with a 0.44 μm wide channel. The measured device is the same as that in Fig. 1.

noticeable output conductance since an aspect ratio $2L_g/W_{ch}$ of ~ 3.6 is not high enough to completely suppress the DIBL effects. In Fig. 3, the transfer $I - V$ of the same device is shown at varied V_{ds} biases. In order to minimize the effect from D_{it} , V_{gs} is swept from 0 V to 3 V with the same sweeping rate in all three curves. The DIBL effect, defined as $\text{DIBL} = \Delta V_{gs} / \Delta V_{ds}$, is measured to be 18 mV/V near the current density of 1 mA/cm^2 .

Figure 4 shows the off-state $I_d/I_g - V_{ds}$ characteristics of representative FinFETs with the same L_g/W_{ch} dimensions. At $V_{gs} = 0 \text{ V}$, a BV of $\sim 560 \text{ V}$ is measured. A soft breakdown behavior of the drain current appears at $V_{ds} > 380 \text{ V}$ while the gate current stays low at the instrumentation limit. This suggests that the transistor breakdown at $V_{gs} = 0 \text{ V}$ is limited by DIBL. To further probe this hypothesis, another set of devices were measured under negative gate bias. At $V_{gs} = -1 \text{ V}$, much higher BV s of up to $\sim 960 \text{ V}$ are observed; moreover, both gate and drain currents increase abruptly and simultaneously at breakdown, which is destructive. These observations exclude the likelihood of avalanche breakdown at $V_{gs} = 0 \text{ V}$, thus confirming DIBL is the dominant mechanism.

For double-gated junctionless MISFETs (i.e., FinFETs) with symmetric source and drain where L_g is the distance

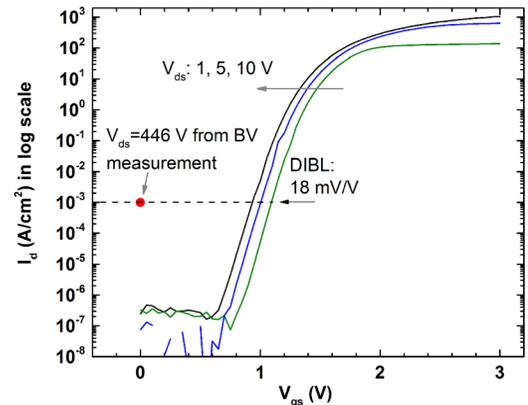


FIG. 3. $I_d - V_{gs}$ transfer characteristics of a vertical Ga_2O_3 power FinFET in the semi-log scale measured at 1, 5, and 10 V, along with the extracted DIBL ($\Delta V_{gs} / \Delta V_{ds}$) at a drain current of 1 mA/cm^2 . The measured device is the same as that in Figs. 1 and 2. The solid symbol denotes the V_{ds} value measured at $V_{gs} = 0 \text{ V}$ and $I_d = 1 \text{ mA/cm}^2$ from the breakdown measurement (see Fig. 4).

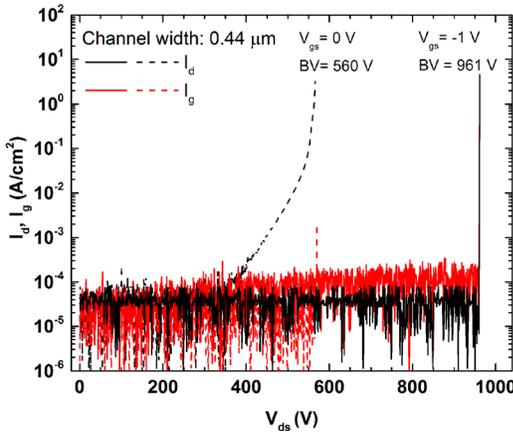


FIG. 4. Representative three-terminal off-state (at $V_{gs} = 0$ V and -1 V) $I_d/I_g - V_{ds}$ characteristics and breakdown voltages of Ga_2O_3 vertical power FinFETs with $0.44 \mu\text{m}$ wide channels. The same device as in Fig. 3 was used for the measurement at $V_{gs} = 0$ V. Another representative device was used for the measurement at $V_{gs} = -1$ V.

between the source and drain, which are often found in logic applications, we can derive the dependence of the V_{th} shift on channel geometry and V_{ds} based on the framework in Ref. 31 as

$$\Delta V_{th} \sim -2e^{-L_g/\lambda} \left[V_{ds} + e^{L_g/2\lambda} \sqrt{\phi_{\min}(\phi_{\min} - V_{ds})} \right], \quad (2)$$

where $\lambda = \sqrt{W_{ch}t_{ox}\epsilon_s/(2\epsilon_{ox}) + W_{ch}^2/8}$ for the depletion mode operation, and ϕ_{\min} is the minimum central channel potential with respect to the source, determined from 2-D numerical device simulation to be about -0.3 V in the device shown in this work. When the channel thickness W_{ch} is much larger than the oxide thickness t_{ox} , it can be seen that the DIBL effect diminishes exponentially with an increasing L_g/W_{ch} ratio. For a fixed L_g , an increment in either oxide thickness or channel width leads to a worse DIBL. Therefore, the aspect ratio $2L_g/W_{ch}$ can be roughly applied to determine the degree of DIBL. In high voltage transistors, the thick n-drift layer sustains most of the voltage drop, thus effectively screening the gated channel from the high voltage on the drain. Therefore, the DIBL effects are expected to weaken compared to the FinFETs for logic applications, and Eq. (2) no longer gives accurate predictions on DIBL effects. Due to the complexity associated with the thick drift region, edge termination near the gate as well as the interface states, 2-dimensional simulations using Sentaurus are employed for the quantitative analysis of DIBL in these vertical Ga_2O_3 power FinFETs.

In Fig. 5, simulated DIBL as a function of V_{ds} and D_{it} using the experimentally determined values of L_g , W_{ch} , and N_d are shown together with the experimental data. In the simulation, uniformly distributed interface states across the energy band gap are assumed, with the charge neutrality level near the mid-gap. All DIBL values are calculated at a drain current level of 1 mA/cm^2 . It is observed that DIBL decreases and the accumulated V_{th} shift increases (see Fig. 6) non-linearly [in contrast to the linear prediction in Eq. (2)] with the increase in V_{ds} due to the screening effect of the thick drift layer. The existence of interface states indeed exacerbates DIBL effects, and the experimental data compare favorably with the simulated results assuming

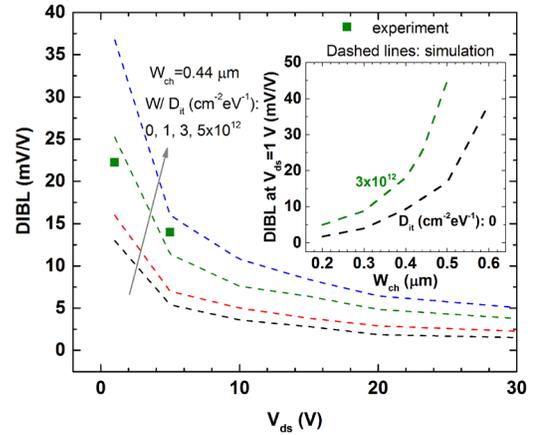


FIG. 5. DIBL with increasing V_{ds} . All DIBL values are calculated at a drain current level of 1 mA/cm^2 . Dashed lines are extracted from 2-dimensional device simulations using Sentaurus assuming various interface state densities. Solid symbols are experimental data. Inset: simulated DIBL at $V_{ds} = 1$ V as a function of W_{ch} , with (red) and without (black) interface states. DIBL is calculated by $\text{DIBL} = \Delta V_{gs}/\Delta V_{ds}$ at $I_d = 1 \text{ mA/cm}^2$.

$D_{it} \sim 3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. The inset shows the DIBL at $V_{ds} = 1$ V as a function of the channel width W_{ch} with the same gate length. It is worth mentioning that with this level of D_{it} , the DIBL values are almost doubled compared to the case without interface states. The impact of $D_{it} \sim 3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ on DIBL is equivalent to an increase in channel width from $0.44 \mu\text{m}$ to $\sim 0.55 \mu\text{m}$.

Figure 6 shows the simulated V_{th} shift as a function of V_{ds} and without the impact of interface states. For each curve in this figure, the net V_{th} shift $\Delta V_{th}(V_{ds})$ is defined as $V_{gs}(V_{ds}) - V_{gs}(V_{ds} = 1 \text{ V})$ at $I_d = 1 \text{ mA/cm}^2$. From Fig. 3, the experiment data at 1 V, 5 V, and 10 V are extracted from $V_{gs} = 1.093$ V, 1.004 V, and 0.935 V at $I_d = 1 \text{ mA/cm}^2$; from Fig. 4, we observe $V_{ds} \sim 446$ V at $V_{gs} = 0$ V and $I_d = 1 \text{ mA/cm}^2$ thus the net V_{th} shift can be calculated to be -1.093 V at $V_{ds} \sim 446$ V. The comparison between the simulations and experimental results indicate the presence of D_{it} with a value of $\sim 3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ under the bias conditions considered here, and that the breakdown mechanism in these devices is dominated by DIBL effects exacerbated by D_{it} . Based on the simulation, it is expected that a MISFET with the same

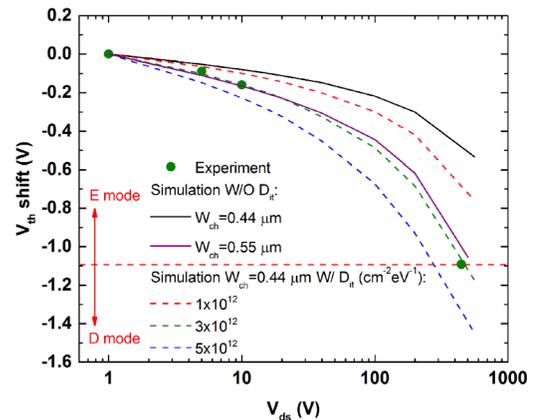


FIG. 6. V_{th} shifts as a result of increased V_{ds} . Dashed lines are simulation results assuming various interface state densities. Solid lines are simulations without interface states. Solid symbols are experimental data. These transistors have a V_{th} at 1 mA/cm^2 of ~ 1.1 V near $V_{ds} \sim 0$ V. The V_{th} shift is calculated by $\Delta V_{th}(V_{ds}) = V_{gs}(V_{ds}) - V_{gs}(V_{ds} = 1 \text{ V})$ at $I_d = 1 \text{ mA/cm}^2$.

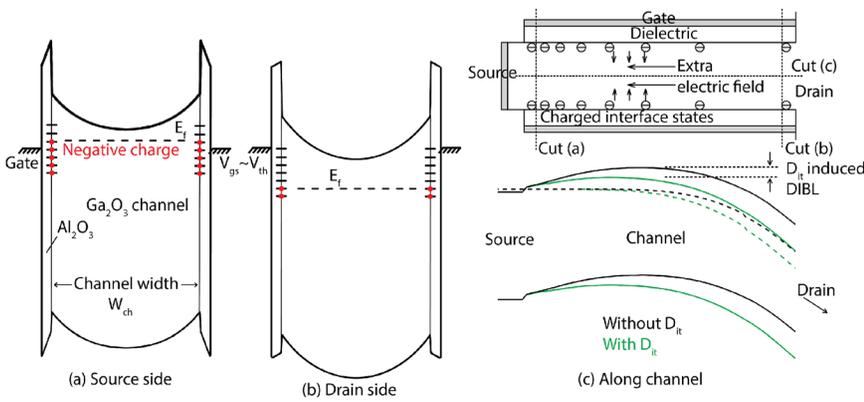


FIG. 7. Schematic band diagram illustrating the impact of gate dielectric interface states on DIBL, with cross-section of (a) source side cut normal to the channel, (b) drain side cut normal to the channel, and (c) center cut along the channel direction comparing the barrier height with (green) and without (black) interface states.

geometry but an optimized interface treatment would have a DIBL-limited BV beyond 1 kV. In addition, it is observed that the V_{th} shift curve for devices with a W_{ch} of $0.55 \mu\text{m}$ and zero interface states roughly aligns with the curve for devices with a W_{ch} of $0.44 \mu\text{m}$ and a D_{it} of $3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ at all voltages. This further confirms that the existence of interface states is equivalent to a wider channel in terms of their impact on DIBL. The simulation also indicates that though DIBL is reduced at higher V_{ds} , the V_{th} shift (integration of DIBL with respect to V_{ds}) shows no trend of saturation, thus remaining a challenge for high voltage transistor operations.

The impact of the interface states on DIBL is illustrated in the band diagrams in Fig. 7 and intuitively explained in the following. Under a fixed V_{gs} bias, on the source side [Fig. 7(a)], the electron quasi-Fermi ($E_{fn(s)}$) level is determined by the source ohmic contact. All the acceptor-like dielectric/channel interface states below the energy E_{fn} are occupied by electrons, hence negatively charged, which is believed to be true in our devices. The built-in potential is expected to be $\phi_{ms} \sim 0.5 \text{ V}$ between the n-type Ga_2O_3 and Cr gate; however, the measured V_{th} is found to be 1.6 V ; thus, we infer that a negative sheet charge Q_{it} of $-2 \times 10^{12} \text{ cm}^{-2}$ is present at the $\text{Al}_2\text{O}_3/\text{Ga}_2\text{O}_3$ interface at V_{th} . Since this Q_{it} exceeds the total donor density in the channel ($\sim 2.6 \times 10^{11} \text{ cm}^{-2}$), the electric field in the gate oxide points in the opposite direction from that in the channel. Under a high voltage from the drain, the channel closer to the drain [Fig. 7(b)] has a higher potential; therefore, $E_{fn(d)}$ is at a lower energy level with respect to the conduction band. This causes fewer interface states to be occupied near the drain end, thus lowering the negative interface charge density. This results in two effects that exacerbate DIBL: (1) less negative charge on the dielectric/channel interface reduces the energy barrier in the channel; (2) a gradient in the interface charge density exists from the source end to the drain end, which generates an extra electric field parallel to current flow. Since this electric field points from the drain to the source, it lowers the barrier height in the channel (c), hence leading to a stronger DIBL effect. In a long channel FET with a larger L_g/W_{ch} aspect ratio, the gradient of the interface charge density is smaller near the center of the channel; thus, the impact of D_{it} on DIBL is weakened. The same trend is also observed in the inset of Fig. 5.

Transistor analysis reveals that the existence of dielectric/channel interface states and charge trapping reduces the gate modulation efficiency and prevents the device from

operating in the accumulation mode. The presence of trap states is confirmed in this experiment in that transistors with narrower channels show lower maximum output current densities and higher on-resistances than those with wider channels at the same gate overdrive voltage. Using a dielectric/channel interface state density of $D_{it} \sim 3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, it is estimated that $\sim 50\%$ of the $0.44\text{-}\mu\text{m}$ wide fin-shaped channel is depleted even at a gate voltage of 3 V . The effective electron field effect mobility in the channel is about $30 \text{ cm}^2/\text{V s}$, $\sim 2\times$ smaller than the estimated electron mobility in the HVPE Ga_2O_3 drift layer, which is in turn extracted from the on-resistance of Schottky barrier diodes on the same wafer. A mobility of $60 \text{ cm}^2/\text{V s}$ in HVPE Ga_2O_3 with a net dopant concentration $N_D - N_A$ in the range of $10^{15} - 10^{16} \text{ cm}^{-3}$ is lower than $\sim 150 \text{ cm}^2/\text{V s}$ reported in bulk Ga_2O_3 .³ It is likely due to the presence of compensating centers, which merits further investigations. Given a large gate length ($\gg 1 \mu\text{m}$) is quite challenging to achieve in these vertical power FinFETs, reducing dielectric/channel interface D_{it} and charge trapping is key to mitigate the tradeoff between on-resistance (i.e., output currents) and DIBL for kV switches.

In conclusion, E-mode vertical Ga_2O_3 FinFETs with an output current higher than 1 kA/cm^2 and a BV near kV are analyzed in this work. A combination of high BV and low R_{on} leads to a Baliga's figure of merit of 125 MW/cm^2 , significantly advancing the state-of-the-art Ga_2O_3 power

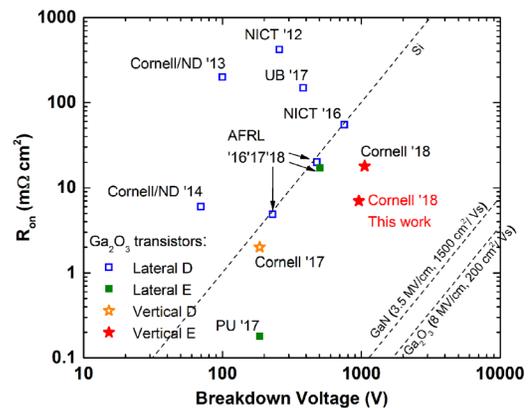


FIG. 8. On-resistance and breakdown voltage values of the state-of-the-art Ga_2O_3 lateral and vertical power transistors. To calculate R_{on} , the active device area excluding ohmic contacts and metal pads have been used, i.e., channel width \times source-drain distance for lateral devices and the source area on top of the fin-channel for vertical devices. References used in the figure: ND '13,³⁴ '14,¹⁰ NICT '12,³⁵ '16,¹³ AFRL '16,¹ '17,³³ '18,²¹ UB '17,³² PU '17,¹¹ Cornell '17,¹⁷ '18.¹⁹

transistors as shown in Fig. 8. Device simulation and analysis show that a relatively low density of dielectric/channel interface states of $\sim 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ leads to nearly doubled DIBL effects in transistors with a $L_g/(W_{ch}/2)$ of 0.8/0.22 μm , which in turn limits the device breakdown as measured in experiments. These trap states also lead to low field-effect mobility in the channel. To this end, it is key to improve the dielectric interface quality; moreover, field plates should be applied to delay premature gate-edge breakdown once the DIBL effects are minimized. The device analysis in this work provides valuable insights on Ga₂O₃ high-power transistor design and processing in general.

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