Enhancement-Mode Ga_2O_3 Vertical Transistors With Breakdown Voltage >1 kV

Zongyang Hu, Kazuki Nomoto, *Member, IEEE*, Wenshen Li, Nicholas Tanen, Kohei Sasaki, Akito Kuramata, Tohru Nakamura, *Fellow, IEEE*, Debdeep Jena, *Senior Member, IEEE*, and Huili Grace Xing, *Senior Member, IEEE*

***Abstract*—High-voltage vertical Ga_2O_3 MISFETs are developed employing halide vapor phase epitaxial (HVPE) layers on bulk Ga_2O_3 (001) substrates. The low charge concentration of $\sim 10^{16}$ cm^{-3} in the n-drift region allows three terminal breakdown voltages to reach up to 1057 V without field plates. The devices operate in the enhancement mode (E-mode) with a threshold voltage of ~1.2–2.2 V, a current on/off ratio of $\sim 10^8$, an on resistance of ~13–18 mΩ·cm^2, and an output current of >300 A/cm^2. This is the first report of high-voltage vertical Ga_2O_3 transistors with E-mode operation, a significant milestone toward realizing Ga_2O_3 based power electronics.**

***Index Terms*—β-Ga_2O_3, HVPE, breakdown voltage, MISFET, MOSFET, FinFET, enhancement mode, vertical transistor, power electronics.**

I. Introduction

GALLIUM oxides has emerged as a new semiconductor material forhigh-power applications in recent years. As the most stable form monoclinic β-Ga_2O_3 has been reported with a wide bandgap up to 4.9 eV [1], a high expected breakdown electric field up to 8 MV/cm [2] and a decent intrinsic electron mobility limit of 250 cm^2/Vs [3], which enables high-voltage and high-power operation. The experimentally reported critical electric field up to 5.2 MV/cm [4], [5] already exceeds that of SiC and GaN [6], and electron mobility of 100-150 cm^2/Vs has been achieved in both bulk substrates [7] as well as epitaxial layers [8]. In addition, low-cost, large area single-crystal substrates [9] allow high-quality epitaxial layers to be developed using various methods.

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Z. Hu, K. Nomoto, and W. Li are with the School of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14853 USA (e-mail: zh249@cornell.edu).

N. Tanen is with the Department of Materials Science and Engineering, Cornell University, Ithaca, NY 14853 USA.

K. Sasaki and A. Kuramata are with Novel Crystal Technology, Inc., Sayama 350-1328, Japan.

T. Nakamura is with the Center for Micro-Nano Technology, Hosei University, Tokyo 184-0003, Japan.

D. Jena and H. G. Xing are with the Department of Materials Science and Engineering, School of Electrical and Computer Engineering, Kavli Institute at Cornell for Nanoscale Science, Cornell University, Ithaca, NY 14853 USA (e-mail: grace.xing@cornell.edu).

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There have been a few reports on high-performance Ga_2O_3 devices in the past few years. Following the first demonstration of Ga_2O_3-nanomembrane field-effect transistors (FETs) [10], this device platform has reached a high current density of 600 mA/mm [11]. Both lateral FinFETs [12] to attain enhancement-mode (E-mode) operation as well as vertical FinFET [13] to attain high areal current density have also been demonstrated. Other reported methods to achieve E-mode transistor operation include using very thin heavily-doped nano-membranes [11], recessed-gate [14], vertical moderately-doped Fins [12] and FETs with unintentionally doped channels and ion-implanted source and drain [15]. Lateral Ga_2O_3 MOSFETs on semi-insulating bulk substrates with field plates [16] are reported to show a breakdown voltage as high as 750 V. Vertical Schottky diodes on n-type bulk substrates [17] and halide vapor phase epitaxial (HVPE) structures [18] are also developed, showing the potential of high-voltage Ga_2O_3 devices.

The past year witnessed first few demonstrations of vertical Ga_2O_3 power transistors. Wong *et al.* [19] reported vertical MOSFETs with a buried current blocking layer (CBL) implanted with Mg; however, the devices showed limited gate modulation due to the difficulty in activating p-type dopants in Ga_2O_3. Simultaneously, our group reported the first vertical Ga_2O_3 Fin-based MISFETs or FinFETs with a current on/off ratio of 10^9 to overcome the difficulty in realizing p-type Ga_2O_3 [13]; however, the high charge concentration of 1×10^{17}cm^{-3} in the drift region led to depletion-mode operation and a relatively low breakdown voltage of 185 V. More recently, Sasaki *et al.* reported depletion-mode vertical trench MISFETs employing lightly-doped HVPE drift layers with decent gate modulation. However, a relatively small ratio of gate-length over channel-width (1-μm/2-μm) led to a high output conductance and a low operation voltage [20]. In this work, we demonstrate the first high-voltage vertical Ga_2O_3 MISFETs or FinFETs with E-mode operation and a breakdown voltage over 1 kV. These devices are referred as MISFETs to distinguish them from the conventional p-n junction based MOSFETs since there are no p-regions in these MISFETs.

II. Device Fabrication

The epitaxial layers were grown by HVPE on n-type bulk Ga_2O_3 (001) substrates (n = 2×10^{18} cm^3). The 10-μm thick

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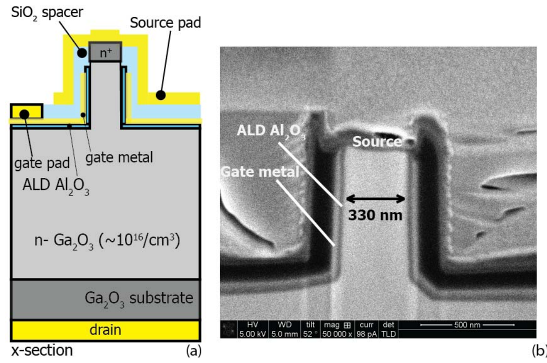

Fig. 1. (a) Schematic cross-section of a Ga_2O_3 vertical power MISFET. (b) 52° SEM cross-section image of a completed Ga_2O_3 vertical Fin-MISFET showing a 330 nm wide and 795 nm long channel.

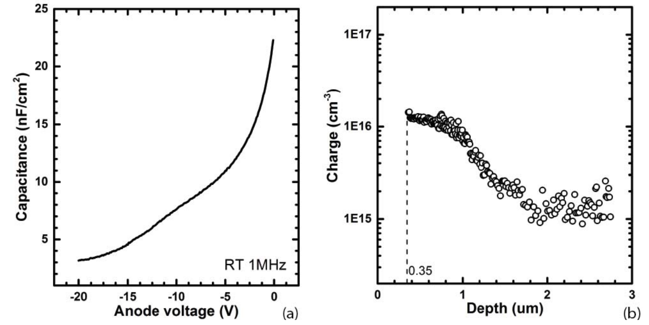

Fig. 2. (a) C-V characteristics of a vertical MOS capacitor on the etched HVPE Ga_2O_3 drift layer. (b) Net charge concentration as a function of depth in the n-Ga_2O_3 drift layer extracted from the C-V data in (a).

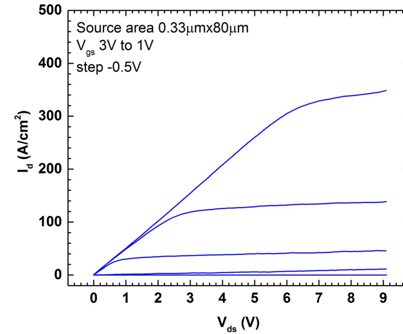

Fig. 3. Representative I_d-V_{ds} characteristics of a Ga_2O_3 vertical power MISFET, taken under pulsed conditions: a pulse width of 6 μs and a duty cycle of 0.06%.

n-Ga_2O_3 epitaxial layer is doped with Si with a target doping concentration of $<2 \times 10^{16}$ cm^{-3}. Device fabrication started with Si ion implantation with a box profile of 5×10^{19} cm^{-3} in the top 50 nm of the drift layer, followed by an activation annealing in N_2 at 1000 °C and 1 atm for 30 min to reduce the contact resistance. Pt metal masks were then patterned by electron beam lithography and deposited by electron beam evaporation on the sample surface to define position and size of the FET channels. Vertical Fin-channels were etched in an inductively coupled plasma (ICP) system [13], [21] with a target width/height of 0.3/1.0 um, respectively. Then, a 30 nm Al_2O_3 was deposited in an atomic layer deposition (ALD) system at 300 °C as the gate dielectric, immediately followed by a 50 nm thick Cr sputtered as the gate metal. The gate pads were deposited a few microns away from the channel for the convenience of electrical measurements. A photoresist planarization process was used to selectively etch away the gate metal/dielectric on top of the n+Ga_2O_3 source. Then, a 200 nm SiO_2 was deposited by plasma-enhanced chemical vapor deposition (PECVD) and a second planarization process was used to etch away the SiO_2 on top of the n+ source. The remaining SiO_2 in the device structure serves as the isolation spacer between the gate metal and the source metal. Finally, source ohmic contacts were formed by depositing Ti/Al/Pt, and device isolation was realized by etching away SiO_2 and Cr between active devices. The schematic cross section of a completed device with a single-finger channel is shown in Fig. 1(a), and a 52° cross-section image of a completed device taken in a focused ion beam (FIB) scanning electron microscopy (SEM) system is shown in Fig. 1(b). The channel width is measured to be 330 nm and the vertical gate length is 795 nm excluding the rounded corners at the bottom of the etched channel.

III. Results and Discussion

The net charge concentration (N_D-N_A) in the n-Ga_2O_3 drift layer is estimated using capacitance–voltage (C–V) measurements on the vertical Cr/Al_2O_3/Ga_2O_3 MOS capacitors in the regions between transistors, which were defined in the same step with the gate pads. The results are shown in Fig. 2, where the net doping concentration is found to decrease from $\sim 1.2 \times 10^{16}$ cm^{-3} at ~0.35 um below the etched Ga_2O_3 surface to $\sim 1 \times 10^{15}$ cm^{-3} at >2 um below the etched Ga_2O_3 surface. This range of the net charge concentration is consistent with the profile desired to achieve E-mode operation and high breakdown voltage. In this analysis, the following parameters have been used: a depletion depth of 0.35 μm under zero bias in Ga_2O_3 with a dielectric constant ε_s of 10, an Al_2O_3 thickness of 30 nm with a dielectric constant of 9.1 and no interface charges at the Al_2O_3/Ga_2O_3 interface. Due to complexity, it is beyond the scope of this study to achieve a comprehensive understanding of doping and compensation mechanisms in lightly-doped Ga_2O_3 as well as distribution of interface charges between ALD dielectric and etched Ga_2O_3 surface.

Figure 3 shows the representative I_d-V_{ds} family curves of a fabricated vertical Ga_2O_3 MOSFET with a source area of 0.33 μm×80 μm. In order to minimize the effects from device self-heating and interface trap states, the I_d-V_{ds} curves were measured under pulsed conditions. At V_{gs} of 3 V and V_{ds} of 10 V, the drain current reaches ~350 A/cm^2 with an associated differential on-resistance of ~18 mΩ.cm^2, normalized to the area of the n+Ga_2O_3 source. Non-uniformity due to doping across the wafer and partly device processing leads to variations in device performance, including the drain current density ranging from 300 to 500 A/cm^2, the on-resistance in the range of 13–18 mΩ.cm^2 and the threshold voltage (V_{th}) in the range of 1.2–2.2 V though the devices were designed to have the same geometry.

All the vertical Ga_2O_3 MISFETs exhibit E-mode, i.e. normally-off, operation. The representative I_d-V_{gs} transfer

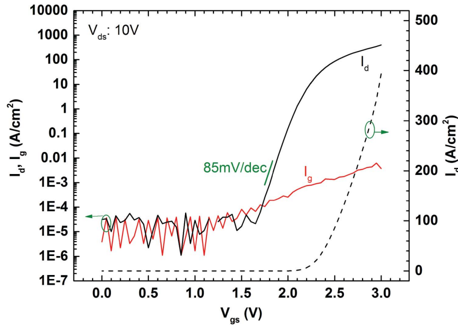

Fig. 4. Representative I_d/I_g-V_{gs} transfer characteristics in the semi-log and linear scale, along with the extracted subthreshold slope.

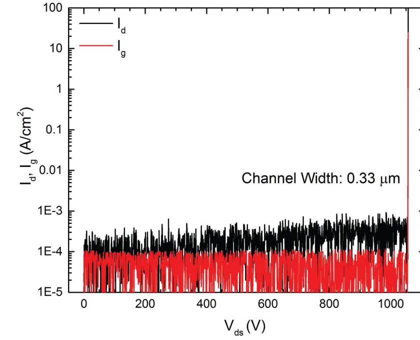

Fig. 5. Representative three-terminal off-state (at V_{gs} = 0 V) I_d/I_g-V_{ds} characteristics and breakdown voltage of Ga_2O_3 vertical power MISFETs.

characteristics of these devices are shown in Fig. 4. The V_{th} defined by linear extrapolation of the drain current at the peak transconductance is ~2.2 V. At $V_{ds} = 10$ V, the drain current on/off ratio is about 8 orders of magnitude, while the off-state leakage current is limited by the measurement system. The sub-threshold slope is measured to be ~85 mV/dec near a current density of 1 mA/cm^2 and the hysteresis is less than 0.2 V.

Given that the transport properties of these lightly-doped HVPE-grown β-Ga_2O_3 and the subsequently formed MOS junctions are yet to be fully characterized, we attempt to gain preliminary understanding on the V_{th} and carrier mobility in the vertical channel of these vertical MISFETs by using the *C-V* measurements of the MOS capacitors shown in Fig. 2. Assuming the quality of the MOS junction in the vertical fin-shaped channel is the same as that of the MOS junctions in the planar surface, and the net charge concentration in the vertical channel is uniform at $N_d \sim 1.2 \times 10^{16}$ cm^{-3}, E-mode operation is expected since the 330-nm wide channel is fully depleted at $V_{gs} = 0$ V. V_{th} can be estimated by summing up two voltage components: 1) the voltage drop difference $V_{th,Ga2O3}$in the n-Ga_2O_3 channel, when reducing the depletion depth in Ga_2O_3 from 350 nm to 165 nm (half of the fin width), expressed as

$$V_{th,Ga_2O_3} = \frac{1}{2}\frac{qN_dW_1^2}{\varepsilon_s} - \frac{1}{2}\frac{qN_dW_2^2}{\varepsilon_s},$$

in which $W_1 = 350$ nm and $W_2 = 165$ nm, and 2) the associated voltage drop difference $V_{th,Al2O3}$ across the Al_2O_3 gate oxide:

$$V_{th,Al_2O_3} = \frac{qN_d(W_1 - W_2)t_{ox}}{\varepsilon_{ox}},$$

in which $t_{ox} = 30$ nm and $\varepsilon_{ox} = 9.1\varepsilon_0$. Assuming the same parameters shown in the earlier section, $V_{th,Ga2O3}$ ~1.03 V and $V_{th,Al2O3}$ ~0.13 V are calculated, thus leading to an estimated V_{th} ~1.2 V. This estimated value falls in the range of the measured V_{th}. However, we believe these devices suffer from interfacial states near the Al_2O_3/Ga_2O_3 interface, which can shift V_{th} as well as reduce gate efficiency. Assuming the vertical channel is solely responsible for the observed R_{on} of 18 mΩ.cm^2 and also assuming it is achieved under the flatband condition, we can estimate the *apparent electron field-effect mobility* in the vertical channel to be ~3 cm^2/Vs. This value is significantly lower than the previously reported electron Hall mobility in β-Ga_2O_3, which could be attributed to the effects of the source ohmic contact resistance, the drain ohmic contact resistance, traps near the Al_2O_3/Ga_2O_3 interfaces, and possibly compensating dopants in the lightly doped n-Ga_2O_3. Unfortunately, all these parasitic parameters cannot be reliably determined in the current device geometry and are thus left for future investigation.

The off-state leakage currents and 3-terminal breakdown voltages in these vertical power MISFETs are measured at $V_{gs} = 0$ V. The representative results are plotted in Fig. 5: both the drain and gate leakage currents remain low, near the detection limit of the measurement instrument, before the hard breakdown near 1057 V. Assuming a 1-dimensional electric field distribution in the drift region, the peak electric field under the gate pad is estimated to be ~1.44 MV/cm, which is far below the expected breakdown electric field of β-Ga_2O_3. However, 2-dimensional device simulations reveal that the electric field peaks near the outer edges of the gate pads as well as the bottom corners of the vertical Ga_2O_3channel at much higher values than 1.44 MV/cm. In fact, examination of the devices after breakdown shows visible damage near the outer edges of the gate pads. For the same reason, the three-terminal BV demonstrated in this work is slightly lower compared to the two-terminal BVs in heterojunction p-Cu_2O/n-Ga_2O_3 diode fabricated on similar HVPE-Ga_2O_3 epitaxial layers and substrates [22]. Therefore, we expect that higher breakdown voltages be achieved by implementing field plates or ion implantation edge termination techniques, similar to what has been achieved in GaN vertical power devices [6], [23]–[25].

IV. Conclusion

β-Ga_2O_3 vertical power MISFETs based on HVPE epitaxial drift layers on bulk Ga_2O_3 substrates are demonstrated in this work. Breakdown voltages higher than 1000 V, on/off ratios of 10^8, and enhancement mode operation are simultaneously achieved. As the first demonstration of high performance Ga_2O_3 vertical transistors, this work shows that Ga_2O_3 vertical devices have great potential in high-power applications.

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