1230 V β-Ga_2O_3 trench Schottky barrier diodes with an ultra-low leakage current of <1 $\mu A/cm^2$

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β-Ga_2O_3 vertical trench Schottky barrier diodes (SBDs) are realized, demonstrating superior reverse blocking characteristics than the co-fabricated regular SBDs. Taking advantage of the reduced surface field effect offered by the trench metal-insulator-semiconductor structure, the reverse leakage current in the trench SBDs is significantly suppressed. The devices have a higher breakdown voltage of 1232 V without optimized field management techniques, while having a specific on-resistance ($R_{on,sp}$) of 15 mΩ cm^2. An ultra-low leakage current density of <1 $\mu A/cm^2$ is achieved before breakdown, the lowest among all reported Ga_2O_3 Schottky barrier diodes. Fast electron trapping and slow de-trapping near the Al_2O_3/Ga_2O_3 interface are observed by repeated C-V measurements, which show an interface state ledge and positive shifts of flat-band voltages with increasing voltage stress. By comparison between pulsed and DC measurements, the device self-heating effect and the trapping effect are uncoupled. It is found that the trapping effect at the trench sidewall affects the on-resistance of the trench SBDs, even under pulsed conditions. With reduced trapping effect and better field management technique, the trench SBDs could further harvest the promising material properties of β-Ga_2O_3. *Published by AIP Publishing.*
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β-Ga_2O_3 has become an attractive material for the development of electronic devices that benefit from the high expected critical electric field of ~8 MV/cm,[1] as a result of its wide bandgap (~4.5 eV),[2] as well as the decent electron mobility of ~200 cm^2/V s at room temperature.[3–5] Such devices include power electronic devices[6–22] and scaled RF power amplifiers,[23–25] especially in a high temperature harsh environment.[26] On top of the attractive material properties, the availability of melt-growth methods to mass-produce single crystal bulk substrates[27] provides important benefits towards low cost as well as the fast development of device technologies and epitaxial growth.

The attractiveness of β-Ga_2O_3 for power electronic devices arises from its highly projected Baliga's figure-of-merit (FOM).[1] In recent years, fast progress on the performance of β-Ga_2O_3-based power devices has been made. A critical electric field of up to 5.2 MV/cm (Refs. 8 and 28) has been observed. With the help of the field-plate, lateral transistors with a breakdown voltage (BV) of 750 V[7] and Schottky barrier diodes with a BV over 1 kV (Refs. 16–19, 21, and 22) have been demonstrated. With the employment of a trench or vertical-fin structure, enhancement-mode transistors with over 1 kV breakdown voltage and decent on-resistance (R_{on}) have been realized.[12] As a result of such advancements, a FOM (BV^2/R_{on}) higher than Si has been achieved.

To further improve the FOM in Ga_2O_3 power devices, the electric field profile needs to be carefully managed to prevent premature breakdown due to field crowding. In addition, in the case of Schottky barrier diodes, reduced surface field (RESURF) techniques are necessary, since the high electric field at the Schottky contact will induce high reverse leakage current through thermionic field emission and image-force-induced barrier lowering effect. Among various RESURF techniques, a trench metal-insulator-semiconductor (MIS) structure[29] is desirable for β-Ga_2O_3 since it does not require a conductive p-type region, which is yet to be realized in Ga_2O_3. In early days, such vertical devices employing castellated surface structures were often termed as *trench* Schottky barrier diodes (SBDs)[29] or static induction transistors (SITs)[30] in Si, SiC, etc.; more recently, device names referring to trenches as *fins* were also adopted in GaN[31] and β-Ga_2O_3.[12,32] Thus, in this context, we will use trench and fin interchangeably.

The first demonstrations of Ga_2O_3 trench-MIS SBDs[20,21] have been very recently reported; however, the FOM is poorer than that of the regular SBDs limited by the device design coupled with the wafer quality. In this work, we report an ultra-low leakage current below 1 $\mu A/cm^2$ in the Ga_2O_3 trench SBDs as a definitive proof of the RESURF effect, as well as a state-of-the-art FOM, thanks to the improved epitaxial material with a uniform doping concentration of $\sim 2 \times 10^{16}$ cm^{-3}.

The schematic cross-section of the trench SBDs is shown in Fig. 1(a). The devices are fabricated on a (001) β-Ga_2O_3 n-type bulk substrate with a 10–μm n$^-$ epitaxial drift layer grown by halide phase vapor epitaxy (HVPE) with a net doping concentration of $\sim 2 \times 10^{16}$ cm^{-3}. Vertical fins with widths (W_{fin}) of 2, 3, and 4 μm and a height of 2 μm are designed. Between the fins is the trench region, where the

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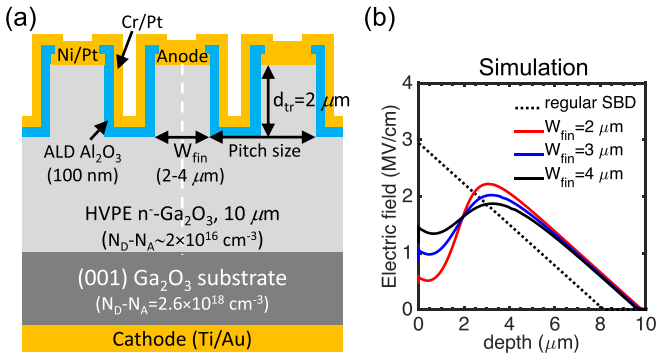


FIG. 1. (a) Schematic cross-section of the β-Ga_2O_3 trench Schottky barrier diodes. Fin widths (W_{fin}) of 2, 3, and 4 μm are designed, along with a trench depth (d_{tr}) of 2 μm. (b) Simulated electric field profile at a reverse bias of 1200 V along vertical cut lines at the center of the fins [see the dashed line in (a)]. The electric field profile in a regular SBD is shown in the dotted line for comparison.

MIS-junction is located. The fin area ratio over the entire device area (or W_{fin}/pitch size) for all fin widths is (60 ± 5)%. Figure 1(b) shows the simulated electric field profile at a reverse bias of 1200 V along a vertical cutline in the center of the fin [see the dashed line in Fig. 1(a)]. In comparison with the regular SBD, the electric field near the top surface is effectively reduced by the trench-MIS structure and the RESURF effect is more pronounced with a smaller fin width.

The fabrication process of the trench SBDs is illustrated in Fig. 2(a). First, reactive ion etch (RIE) based on BCl_3 and Ar[33] was performed on the backside of the wafer to facilitate ohmic contact. After that, Ti (50 nm)/Au (125 nm) was evaporated on the backside as the cathode contact followed by a rapid thermal anneal (RTA) for 1 min in a N_2 environment.[34] Next, Ni (20 nm)/Pt (120 nm) was deposited and patterned by a lift-off process on the top surface, serving as the Schottky

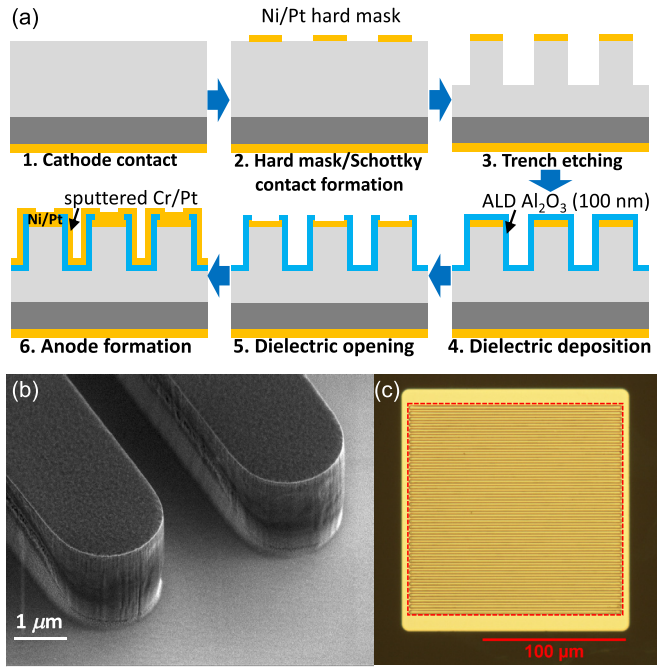


FIG. 2. (a) Fabrication process flow of the trench- or fin-SBDs. (b) 45° tilted SEM image of the etched fins with a fin width of 2 μm. (c) Optical graph of the top view of a fabricated device with a fin width of 2 μm. *The central anode area enclosed by the red dashed line is used for calculating current densities.*

contact as well as the hard mask for the subsequent etching for trench formation. Trenches with a depth of 2 μm were etched using RIE, resulting in fin channels oriented along the [010] direction. Figure 2(b) shows a scanning electron microscopy (SEM) image of the etched fin channels tilted at 45°. Near vertical fin sidewalls are observed. Subsequently, the etched surface was cleaned in HCl before the deposition of a 100-nm Al_2O_3 dielectric layer by atomic layer deposition (ALD). Next, the dielectric was opened by dry etching to expose the Ni/Pt Schottky contact, followed by a deposition of Cr (10 nm)/Pt (70 nm) over the sidewall by sputtering. Figure 2(c) shows a top-view optical image of a fabricated trench SBD with a fin width of 2-μm. The cross-section SEM image of the device is shown in the supplementary material.

Under the same fabrication process, regular SBDs with the same Ni/Pt Schottky contact on the original epitaxial surface were also formed. A net doping concentration (N_D-N_A) of $\sim 2 \times 10^{16}$ cm^{-3} is extracted from the regular SBDs from capacitance-voltage (C-V) measurements (see supplementary material). With an additional evaporation of Ni (20 nm) on the planar surface prior to the sputtering of Cr/Pt, MOS-capacitors with a Ni-based anode contact on the etched (001) surface were co-fabricated on the same sample. Figure 3 shows the high frequency C-V measurements on a MOS-capacitor. To investigate the charge trapping effect typically seen at the MOS interface, repeated sweeps were performed on the capacitor starting with a fixed reverse bias limit of −30 V and toward different forward bias limits (stress voltage), which was stepped up from 5 V to 30 V. At each stress voltage, 3 repeated dual-direction sweeps were performed. Figure 3(a) shows the first set of sweeps up to a stress voltage of 5 V. In comparison with the ideal C-V curve, the 1st upward sweep shows a positive flat-band voltage (V_{fb}) shift of 1.6 V as a result of an interface state ledge.[35] The ledge is due to the population of deep interface states with trapped electrons during the upward sweep. Assuming that the trapped charge is located close to the Al_2O_3/Ga_2O_3 interface, the sheet density of the trapped negative charge (N_{tr}) can be obtained by

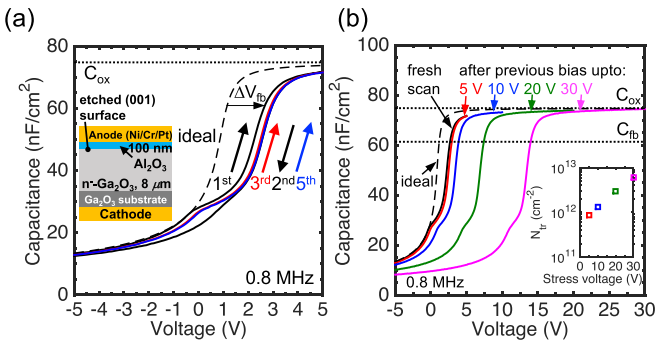


FIG. 3. High-frequency capacitance-voltage (C-V) measurements on a MOS-capacitor fabricated on the etched (001) surface. The device cross-section is shown in the inset of (a). Repeated C-V sweeps were performed with a fixed reverse bias limit of −30 V and a different forward bias limit (stress voltage), which was stepped up from 5 V to 30 V. At each stress voltage, 3 repeated dual-direction sweeps were performed starting from −30 V. (a) The set of sweeps up to 5 V. The ideal C-V curve in the absence of the trapping effect is shown in the dashed line. (b) The 3rd upward sweeps at each forward bias limit and the inset shows a plot of the extracted trapped charge density (N_{tr}) at each stress voltage. A probing frequency of 0.8 MHz and a sweep rate of 0.1 V/s were used for all sweeps. No hold time was employed.

$$N_{tr} = C_{ox} \cdot \Delta V_{fb}/e, \quad (1)$$

where C_{ox} is the dielectric capacitance, e the elemental charge and ΔV_{fb} the flat-band voltage shift. According to Eq. (1), a N_{tr} of $7.4 \times 10^{11}\,cm^{-2}$ is calculated based on the ΔV_{fb} of 1.6 V associated with the 1st upward sweep to 5 V. These trapped charges should be primarily due to the deep interface states. After the 1st sweep to 5 V, the V_{fb} is further shifted as indicated by the hysteresis. The V_{fb} shift is not recovered after the downward sweep back to deep depletion and stays nearly the same as indicated by the subsequent upward sweeps. On the other hand, the interface state ledge is nearly identical in subsequent upward sweeps. This indicates that the trapped charge associated with the ledge can be mostly de-trapped with the downward sweep but there are additional trapped charges that cannot be de-trapped, which suggests that trapping mechanisms other than the deep interface states may exist. Figure 3(b) shows the 3rd upward sweeps at each forward bias limits. The V_{fb} increases with increasing bias limit, suggesting an increasing N_{tr}. The V_{fb} shift does not recover until several days later. Inset shows the extracted N_{tr} based on the ΔV_{fb} referenced to the ideal C-V curve at each stress voltage. Notice that the interface state ledge is present in each upward sweep. It further suggests that the deep interface states associated with the C-V ledge is not the only trapping mechanism. In fact, such a charge trapping effect has been observed in several reports on Al_2O_3/β-Ga_2O_3 MOS capacitors,[36–39] and the traps inside the ALD Al_2O_3 dielectric have been identified as one of the major causes.[40] We thus speculate that the increasing trapping effect or N_{tr} with increasing voltage stress is likely associated with the traps in the dielectric. In addition, it is worth noting that N_{tr} after the voltage stress toward accumulation (30 V) is $\sim 5 \times 10^{12}\,cm^{-2}$, which is similar to the values reported in Refs. 36 and 38. As will be discussed later, the trapping effect is detrimental to the forward conduction of the trench SBDs.

The forward I-V characteristics of the trench SBDs is compared with that of the regular SBDs in Figs. 4 and 5. Both DC and pulsed measurements were performed on the devices. *For a fair comparison, the current density of the trench SBDs was calculated by the entire central area of the anode enclosed by the dashed line in Fig. 2(c).* Figure 4(a) shows the DC measurement results in a log-scale. The trench SBDs and the regular SBD have the same ideality factor of 1.08. The barrier height (ϕ_B) of the trench SBDs and the regular SBD is extracted to be 1.40 eV and 1.35 eV, respectively, using the thermionic emission model. The slightly higher barrier height/turn-on voltage in the trench SBDs was observed before both in trench SBDs[20] as well as in trench junction-barrier-Schottky-diodes,[41] which can be attributed to the increase of the effective barrier height due to the adjacent MOS junction or p-n junction.[41] Figure 4(b) shows the pulsed I-V measurements from 0 V to 5 V in a linear-scale. The pulsed I-V measurements were performed to mitigate primarily the self-heating effect, as will be discussed more in detail later. In comparison with the regular SBD, the trench SBDs have lower current density. This is due to the restricted conduction path as a result of the fin geometry. The current density for different fin widths is similar, and the finite variation is attributed to the slight difference in the fin area ratio, nonuniformity of the processing and the doping concentration in the wafer. Figure 4(c) shows the extracted specific differential on-resistance ($R_{on,sp}$) of the devices from the pulsed measurements. The trench SBDs have an $R_{on,sp}$ of $\sim$15 mΩ cm^2, while the regular SBD has an $R_{on,sp}$ of 6.6 mΩ cm^2.

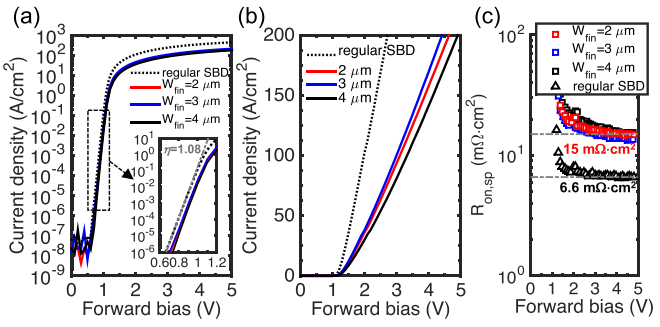
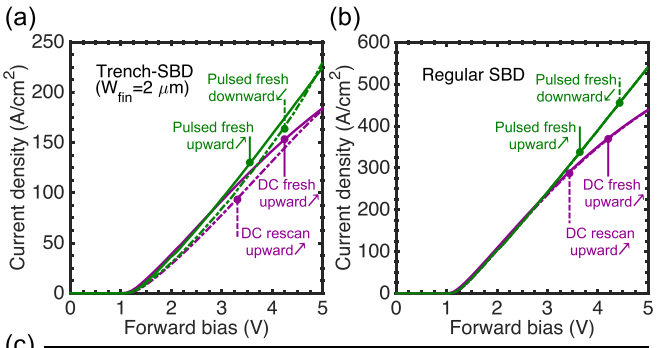


FIG. 4. Forward I-V characteristics of the trench SBDs in comparison with the regular SBD fabricated on the same wafer. (a) Measurements under DC conditions in a log scale. The inset shows the zoom-in plot of the exponential turn-on region. The ideality factor of the diodes is extracted to be ~1.08. (b) Measurements under pulsed conditions from 0 V to 5 V in a linear scale. The pulse width is 8.4 μs and the duty cycle is 0.84%. The quiescent voltage (V_Q) is 0 V. (c) Extracted differential specific on-resistance from pulsed I-V measurements.

The comparisons between the DC and pulsed measurements under different measurement conditions are shown in Fig. 5. In the trench SBD [Fig. 5(a)], notable differences are observed in three sets of comparisons: (i) pulsed vs. DC scan; (ii) pulsed scan upward vs. pulsed scan downward and (iii) DC fresh scan vs. DC re-scan. In the regular SBD [Fig. 5(b)], notable difference is observed only in: (i) pulsed vs. DC scan. These comparisons are summarized in the table in Fig. 5(c). In the comparison (i) for the regular SBD, a lower current is observed under the DC scan at a bias higher than 3 V compared with the pulsed scan. This is attributed to the device self-heating effect under DC measurements. For the trench SBD, the difference in comparison (i) is similar to that in the regular SBD and is primarily due to the self-heating effect. However, distinct from the regular SBD, it is also compounded by the trapping effect as indicated by comparisons (ii) and (iii). In comparison (ii) for the trench SBD, the self-heating effect is removed by the pulsed condition. As a result, the difference between the pulsed upward and downward scans on a fresh trench SBD should be due to the presence of trapping effect. Since no trapping effect is observed in the regular SBDs, the trapping must be located at the trench MIS structure. Although the crystal orientation of the fin sidewall is different from that of the (001) surface, we speculate that the similar trapping effect occurs as in the MOS-capacitors on the etched (001) surface. That is, when a positive voltage is applied at the anode of the trench SBD, negative charges start to get trapped near the sidewall interface. The negative sheet charge causes a depletion of the fin channel. Assuming an N_{tr} of $\sim 8 \times 10^{11}\,cm^{-2}$ at the trench sidewall similar to the value extracted in the MOS-cap after a 5-V stress, there will be an *extra* depletion width of ~170 nm at zero bias in the channel from each side due to the N_{tr}. The extra depletion width increases the channel resistance, thus lowering the measured current. Notice in comparison (ii) for the trench SBD, the downward pulsed scan measures a higher current initially at 5 V than the upward pulsed scan. This is because no charge trapping



(c)

Comparisons	Trench-SBD	SBD
	Observation (main cause)	Observation (main cause)
(i) Pulsed vs. DC	**Different** (self-heating)	**Different** (self-heating)
(ii) Pulsed ↗ vs. Pulsed ↙	**Different** (trapping effect)	**Near identical**
(iii) DC fresh ↗ vs. DC rescan ↗	**Different** (trapping effect)	**Near identical**

FIG. 5. Pulsed vs. DC I-V measurements (a) on a trench SBD with a fin width of 2 μm and (b) on a regular SBD. (c) Summary of the three sets of comparisons among different measurement conditions.

occurred before the 5-V current data were first acquired during the downward scan. In contrast, the downward pulsed scan measures *lower* current than the upward pulsed scan between 1.5 and 4.5 V. This is due to a more pronounced charge trapping effect within this biasing region under the downward scan as a result of the initial biasing at 5 V. Similarly, in comparison (iii) for the trench SBD, the lower current under the DC rescan is also due to the charge trapping after the device was biased at 5 V. Due to the asymmetry between the fast trapping process and the slow detrapping process, the pulsed measurement data for the trench SBD is still affected by the trapping effect and the extracted $R_{on,sp}$ under the pulsed condition is still *higher* than the ideal $R_{on,sp}$ determined by the intrinsic drift layer material property and the device geometry. The trapping effect could be reduced with a post deposition anneal (PDA) of the ALD dielectric[40,42] and with improved surface treatment on the etched Ga_2O_3 surface after the dry etch.

The representative reverse I-V characteristics of the trench SBDs in comparison with the regular SBD is shown in Fig. 6. In the regular SBD, the reverse leakage current increases quickly as the reverse bias is increased. The hard breakdown voltage is 734 V. In comparison, the trench SBDs have much lower leakage currents and higher BVs. In devices with a W_{fin} of 2 μm, the highest BV of 1232 V is observed,

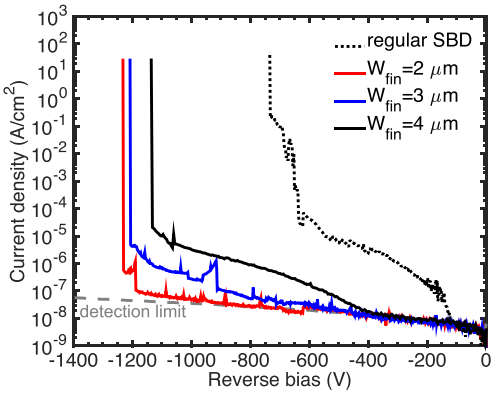


FIG. 6. Reverse bias I-V characteristics of the trench SBDs in comparison with the regular SBD.

together with an ultra-low leakage current density of less than 1 μA/cm^2 before breakdown, without other optimized field management techniques. For a bias lower than ~1000 V, the leakage current density is around the detection limit (<0.1 μA/cm^2), translating into a very low off-state power dissipation of <0.1 mW/cm^2. Higher leakage current and lower breakdown voltage is observed for wider fin widths, suggesting that a narrow fin width is preferable for a more pronounced RESURF effect and a higher breakdown voltage.

Figure 7(a) benchmarks the state-of-the-art β-Ga_2O_3 SBDs, using a reverse blocking voltage defined at 1 mA/cm^2, as typically used in commercial SBDs for a reasonable off-state power consumption. With such a definition, the FOM at 1 mA/cm^2 for a number of regular SBDs is worse than using the hard breakdown voltage, especially for the SBDs with breakdown voltages higher than 1 kV, due to their high leakage current under high surface fields. Although not having the highest FOM at 1 mA/cm^2 among all the reported SBDs, the 2-μm trench SBD from this work has a comparable FOM with the best SBDs, while achieving a notable improvement in the FOM compared with the previous trench SBD reports.[20,21] In comparison with our previous results,[21] the on-resistance is much reduced due to a more uniform doping profile with a moderate level (~2×10^{16} cm^{-3}) and less carrier compensation.

Figure 7(b) shows the leakage current density at 80% of the reported BV vs. the reported BV of β-Ga_2O_3 SBDs. It can be seen that the trench SBDs generally have lower leakage currents than the regular SBDs. The 2-μm trench SBDs

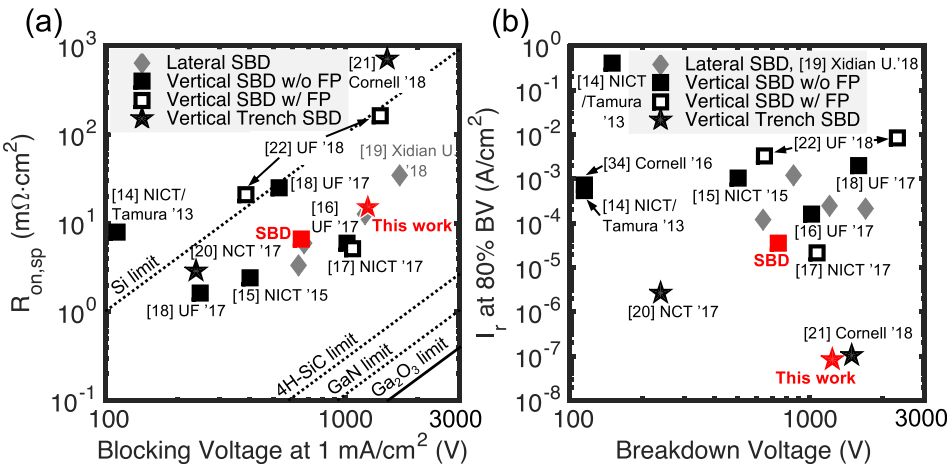


FIG. 7. Benchmark plots of the state-of-the-art β-Ga_2O_3 SBDs. (a) Differential specific on-resistance $R_{on,sp}$ (excluding the turn-on voltage) vs. the blocking voltage specified at a reverse leakage current density of 1 mA/cm^2. (b) Leakage current density at 80% of the reported BVs vs. the reported hard-breakdown voltage. The 2-μm trench SBD in this work has the lowest leakage current at 80% BV among all the reported SBDs.

in this work achieve the lowest leakage current density among the reported β-Ga_2O_3 SBDs. Note that a number of reported vertical SBDs use similar HVPE-grown drift layers with a net doping concentration around $2 \times 10^{16}\,cm^{-3}$.[15–17] As is expected, our regular SBD shows a comparable leakage level as those reports, suggesting that the observed advantage over the leakage current in our trench SBDs arises from the device structure itself.

In conclusion, β-Ga_2O_3 vertical trench SBDs with pronounced RESURF effects and state-of-the-art FOM are reported. Fast electron trapping and slow de-trapping are observed near the Al_2O_3/Ga_2O_3 interface from repeated C-V measurements. Comparing the forward I-V characteristics under DC versus pulsed conditions, it is found that device self-heating limits the DC current at >3 V and the trapping effect at the fin sidewall affects the measured on-resistance even under pulsed conditions. The trench SBD with a 2-μm fin width is found to have a breakdown voltage of 1232 V and an ultra-low leakage current of <1 $\mu A/cm^2$, the lowest reported value among the reported β-Ga_2O_3 Schottky barrier diodes. The FOM could be further improved toward the promised material limit of β-Ga_2O_3 with a reduced trapping effect and better field management.

See supplementary material for more information on the device cross-section, doping profile and dielectric quality.

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