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1.6 kV Vertical Ga_2O_3 FinFETs With Source-Connected Field Plates and Normally-off Operation

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Abstract*—High performance Ga_2O_3 vertical FinFETs with a breakdown voltage of 1.6 kV, a drain current density of 600 A/cm^2 have been demonstrated in this work. Fin-shaped channels with sub-micron widths lead to a high threshold voltage of 4 V, and also provide strong RESURF effects to reduce the drain leakage current and increase the breakdown voltage. A low leakage current of lower than 10^{-3} A/cm^2 is maintained until the hard breakdown of the transistor. In order to sustain high voltage, a source-connected field plate (FP) supported by a dielectric layer is implemented at the outer edge of the gate pad as the edge termination, which enabled a breakdown voltage almost 2 times as high as those without FP. Device simulation shows that the highest electric field peak appears at the FP edge, which suggests further improvement of the breakdown voltage is possible by optimizing the FP design or implementing additional edge terminations.

Keywords—Vertical transistor, Ga_2O_3, FinFET, normally-off, breakdown voltage, field plate

I. Introduction

In recent years, Ga_2O_3 has been identified as one of the most important semiconductors for power applications. In its most stable crystal structure, monoclinic β-Ga_2O_3 has an ultra wide bang gap of up to 4.9 eV, a high estimated breakdown electric field of 8 MV/cm [1] and a decent electron mobility of up to 250 cm^2/Vs [2], enabling high voltage, high current and stable device operations even under harsh environments. One of the most attractive aspects of Ga_2O_3 for both research and applications is the availability of large-area low dislocation density (~10^2 cm^{-2}) bulk Ga_2O_3 substrates through melt growth methods [3] [4]. This serves as the fundation for high quality epitaxial layers with electron mobility up to 150 cm^2/Vs [5] and > 10 μm thick n-type layers with controllable doping concentrations [6], which are excellent building blocks for power device development.

Similar to many other wide band gap semiconductors, Ga_2O_3 power devices are limited to unipolar conduction due to the lack of high conductivity p-type Ga_2O_3. To this end, MOS-based structures provide a RESURF (Reduced Surface Field) effect that enhances the breakdown voltages (BV), therefore Field plate (FP) Schottky Barrier Diodes (SBD) [7] and lateral MOSFETs [8] have shown high BV in excess of 1 kV. Furthermore, we have proposed and demonstrated vertical FinFETs [9] [10] and vertical trench SBDs [11] [12] with stronger RESURF effects near the channel region similar to those in p-n super junctions, and achieved record-high performance in vertical Ga_2O_3 devices well surpassing the Si unipolar limit. These vertical Ga_2O_3 power devices directly benefit from the high quality bulk substrates and Halide Vapor Phaze Epitaxy (HVPE), and have the potential to deliver higher power than the lateral power devices. In our recent development of the vertical FinFETs, both experiment and simulation suggest that electric field crowding near the edge of the gate pads could limit the BV of the transistor [13]. In this new generation of vertical FinFETs, we have designed a source-connected FP with perfect compatibility with our existing process flow. This modification significantly improves the BV of the transistors to > 1.6 kV, compared to BV ~870 V for those without FP on the same sample. FP together with a higher charge concentration in the drift layer also leads to a slightly reduced on-resistance thus improved Baliga's figure of merit (BFOM).

II. Experiment

The sample used in this work is a 10 μm n$^-$-Ga_2O_3 grown by HVPE method on a (001) Ga_2O_3 substrate. The process flow is decribed as the following: The source contact Cr/Pt is deposited on a layer of n$^+$-Ga_2O_3 formed by Si ion implantation on the top surface of the wafer. The channel of the transistor is defined by electron beam lithogratphy, and formed by dry etching in an ICP-RIE system and subsequent acid/base wet chemical treatments to remove the plasma damages. From the SEM images taken in **Fig. 1**, a typical fin geometry is about 1.3 μm tall and 480-560 nm wide from the source-end to the drain-end. The bottleneck structure shown

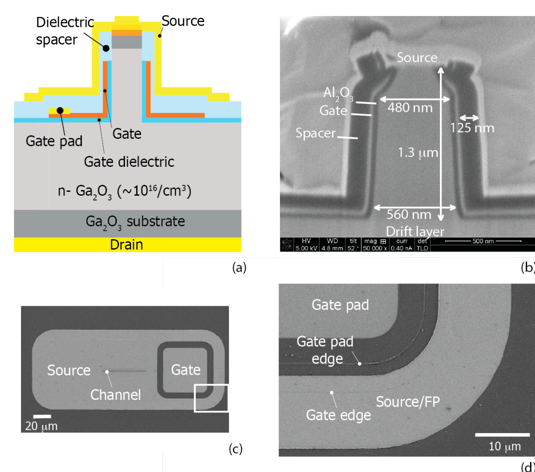

Fig. 1: (a) Schematic structure of a vertical Ga_2O_3 (001) FinFET with source-connected field plates, (b) an SEM cross section image, (c) SEM top-view image and (d) zoomed in image of the field plate region.

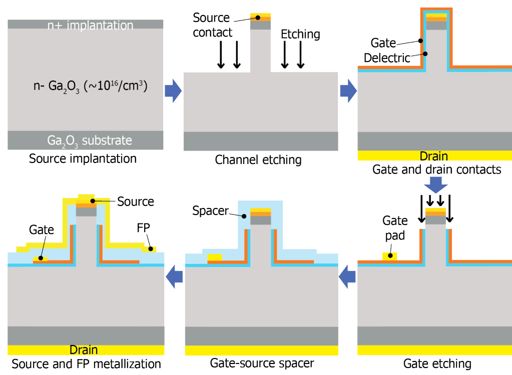

Fig. 2: Device fabrication process flow of vertical Ga_2O_3 FinFETs.

in Fig. 1(b) is likely a result of the wet chemical reaction. The drain ohmic contact is then metallized, followed by conformal depositions of a thin gate dielectric (Al_2O_3 by Atomic Layer Deposition (ALD)) and a gate metal (Cr) layer to form MOS structures on both sidewalls of the fin channel. The gate-source spacing is defined in the gate etchback step which includes a critical photoresist based planarization process [14]. A thick layer of ALD Al_2O_3 is used to realize the source-gate isolation, as well as to support the field plate extension. Finally, the source pad is conformally deposited in a sputtering system, forming the source-connected field plate at the same time. Relevant processing steps are schematically shown in **Fig. 2**. Compared to previous generations of Ga_2O_3 FinFETs [9] [10], the new device design features a reduced gate area and an extended source pad outside the gate edge. This allows the implementation of the FP without complicating the processing steps. This is essential in improving device yield and facilitating low-cost fabrication. The finished Ga_2O_3 FinFET (**Fig. 1**) has a 30-nm gate dielectric (ALD Al_2O_3), a 125-nm (h_{fp}) ALD Al_2O_3 source-gate spacer and a source metal with a 10-μm FP extension (L_{fp}) outside of the gate edges.

III. Results

High frequency C-V measurements are taken on vertical MOS capacitors on etched (001) surface, and the net charge concentration in the n^--Ga_2O_3 is calculated as about 1.2×10^{16} cm^{-3} (**Fig. 3**). DC I-V characteristics of a transistor with a fin width of ~0.5 μm (same channel geometries as the SEM image in Fig. 1(b)) show a maximum drain current density of 600 A/cm^2, a differential on-resistance of 5.5 mΩcm^2 at

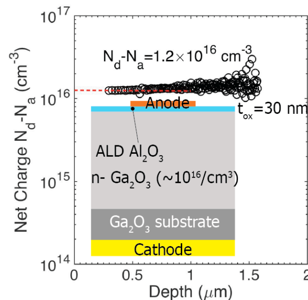

Fig. 3: Charge distribution in the drift layer extracted from high frequency (1 MHz) C-V measurements.

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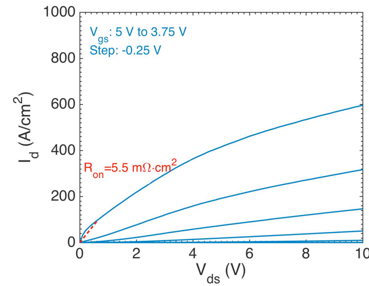

Fig. 4: DC I_d-V_{ds} characteristics of vertical Ga_2O_3 FinFETs with 0.5 μm fin width.

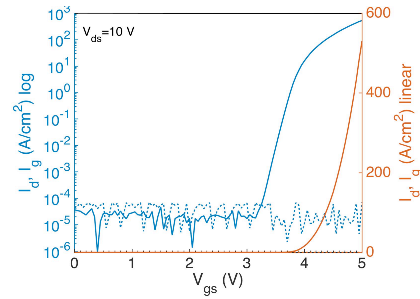

Fig. 5: DC I_d, I_g-V_{gs} characteristics of vertical Ga_2O_3 FinFETs with 0.5 μm fin width in log/linear scales.

V_{gs}=5 V (**Fig. 4**) and a threshold voltage V_{th}~3.8 V (**Fig. 5**) at V_{ds}=10 V. The current density and on-resistance are both normalized using the footprint of the vertical channel. The gate leakage current is lower than the limit of our measurement system for all applied voltages below the *BV*. The drain current on/off ratio is about 10^8, with its off state leakage at the same level as the gate leakage thanks to the strong RESURF effect provided by the fin channel. The unusually high V_{th} may be explained by a sheet of negative interface charge on the order of 2-5×10^{12} cm^{-2} on the sidewalls between the Al_2O_3 gate dielectric and the Ga_2O_3 channel [13]. Since this sheet charge concentration is significantly higher than the total donor concentration in the channel (3×10^{11} cm^{-2}), it reverses the electric field in the gate dielectric layer and causes V_{th} to be insensitive to the channel width.

2D simulations are performed to guide the design of the device for high *BV*s. It can be shown by both electrostatic analysis and numerical simulation that the electric field at the bottom of the fin channel is reduced significantly with a narrower fin channel width (W_{ch}). For example, for W_{ch}~0.5 μm channels in the FinFETs in this work and parameters used in **Fig. 6**, the electric field peak value at the bottom corner of the channel is 3.05 MV/cm, while peak value underneath the central area of the gate pad is 3 MV/cm. In comparison, the peak value at the edge of the gate pad is 9 MV/cm without any RESURF effects (all values are taken at a depth of 0.1 μm below the etched Ga_2O_3 surface). The stark difference is explained as the following: a gate without an edge termination has a lateral depletion region outside the edge, leading to severe electric field crowding typically described by the cylindrical junction model [15]. Due to the symmetry of the double-sided gate structure, the lateral depletion width near the bottom of the fin channel is limited to W_{ch}/2. This effectively removes majority of the space charges outside of the gate edge that would have caused the

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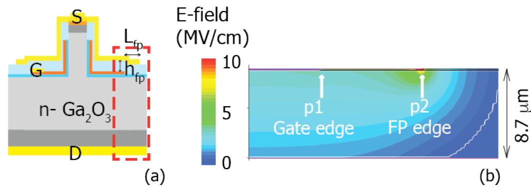


Fig. 6: Vertical Ga_2O_3 FinFET structure with FP. (b) Simulation of off-state electric field distribution at V_{ds}=1600 V showing electric field peaks at the gate (p1) and FP (p2) edges. L_{fp}=10 μm, h_{fp}=0.125 μm, N_d=1.2×10^{16} cm^{-3}.

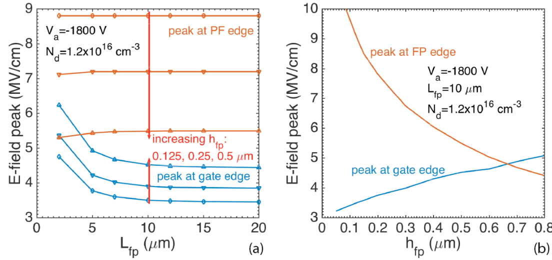
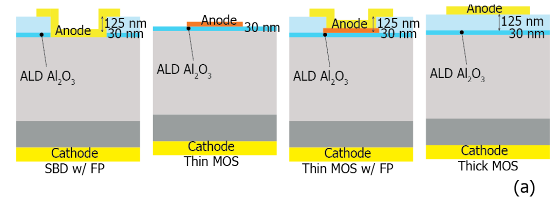


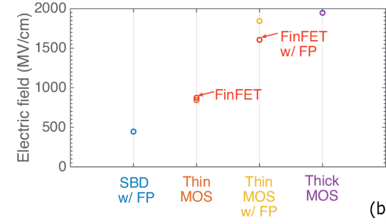
Fig. 7: Simulation of electric field peaks at the gate and FP edge as functions of (a) FP length (L_{fp}) and (b) FP height (h_{fp}). E-field values are taken at a depth of 0.1 μm inside Ga_2O_3. Other parameters are the same as those in Fig. 6.

electric field crowding. This effect is fundamentally very similar to the deep mesa edge termination [16], but with added benefits of easier experimental implementaion and the fact that it applies to unipolar power devices.

The electric field distribution near the gate edge with the addition of the FP show two peaks at the gate edge (p1) and FP edge (p2) respectively (**Fig. 6**). Two main parameters are considered for their impact on electric field peaks: the thickness of the supporting dielectric h_{fp} and FP extension ouside of the gate L_{fp}. It is discovered that for the voltage range considered, a FP extension L_{fp} of 10 μm or longer is able to suppress the electric field peak p1 for any thickness value of the h_{fp}, while the electric field at p2 is not significantly affected by L_{fp} (**Fig. 7(a)**). For a L_{fp} value of 10 μm, the tradeoff between p1 and p2 values and their heavy dependence on h_{fp} is clearly seen in **Fig. 7(b)**, where the optimal value of h_{fp} can be determined when the 2 field peaks have comparable magnitude.

Experimentally, a dielectric thickness h_{fp} of 0.125 μm is used due to the practical limitation of the device processes. Vertical diodes with various edge terminations (**Fig. 8(a)**) are measured as a reference to the transistor results, and the highest *BV* of each structure is shown in **Fig. 8(b)**. *BV* of the thick (155 nm dielectric) MOS diode is measured at 1950 V, which is more than twice of the *BV* measured on thin (30 nm dielectric) MOS diodes without FP. This is because the increase of the dielectric thickness has reduced the peak electric field at the surface of Ga_2O_3 at the same reverse voltage. The breakdown mechanism in dielectric materials [17] suggests that its *BV* will be limited by the electric field near the Al_2O_3/Ga_2O_3 interface, therefore much higher reverse voltage can be sustained by the thick MOS. The Schottky barrier diodes (SBD) with FP fabricated on the same sample have much lower *BV*s most likely due to plasma etch damage since all diodes are fabricated on dry-etched Ga_2O_3 surfaces. From the electric field simulation, the electric field peak at the gate edge (p1) of the thin MOS is





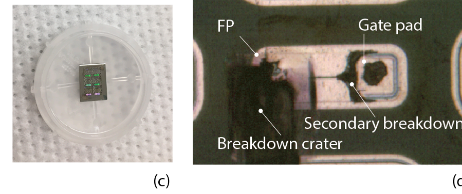


Fig. 8: Reverse breakdown voltages of Ga_2O_3 SBD and MOS structures: (a) schematic cross sections of diodes with different edge terminations, (b) measured highest reverse *BV*s of each structure, (c) fabricated Ga_2O_3 vertical FinFET sample size 10mm×7.5mm and (d) an optical image of a typical FinFET after breakdown.

significantly reduced by the FP. The thin MOS diode with FP has a *BV* of 1840 V, similar to those measured in thick MOS diodes. Off-state (V_{gs}=0 V) breakdown measurements of vertical FinFETs with and without FP show *BV*s of 1605 V and 876 V respectively (**Fig. 9**), which are similar to the results on vertical MOS diodes. The gate and drain leakage currents stay lower than 10^{-3} A/cm^2 until dielectric breakdown. Multiple FinFETs with fin channel widths ranging from 0.4 μm to 0.6 μm have been tested, and their *BV*s are largely independent of fin widths, indicating that breakdown is not dominated by the fin channel region. Both experimental data and simulation suggest that the breakdown is likely dominated by the dielectric breakdown at the edge of the FP (p2), which is then substantiated by the visual evidence that the most material damage after the destructive breakdown appears at the edge of the devices (**Fig. 8(d)**). In order to further improve the breakdown voltage of the transistor, additional edge termination may be implemented such as the multiple field plates, resistive ion implantation and floating guard rings.

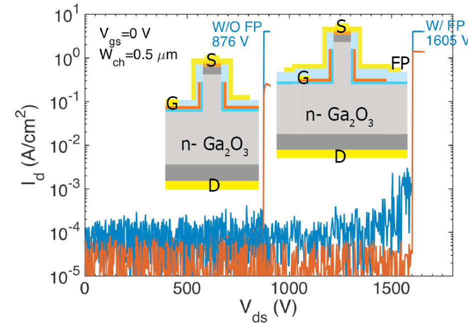


Fig. 9: Off-state (V_{gs}=0 V) I_d, I_g-V_{ds} and *BV* measured on vertical Ga_2O_3 FinFETs with and without FP.

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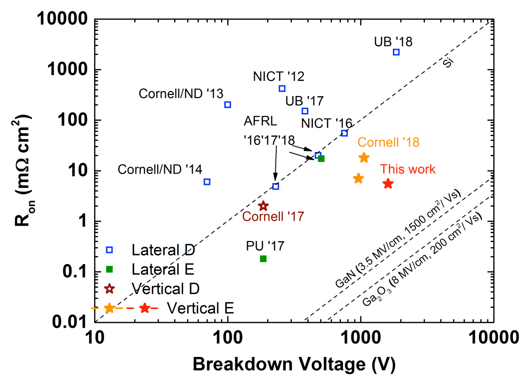

Fig. 10: On resistance and breakdown voltage benchmark of state-of-the-art Ga_2O_3 lateral and vertical power transistors [18]-[26]. The data

On-resistance and BV benchmark for state-of-the-art lateral and vertical Ga_2O_3 transistors is summarized in **Fig. 10**. Compared to previous generation of vertical FinFETs with a lower charge concentration of 10^{15} cm^{-3} in the drift layer [10], the FP FinFETs in this work has slightly lower R_{on} and much higher BV, thus significantly improved BFOM comparable to the state-of-the-art lateral Ga_2O_3 FETs. Furthermore, the vertical FinFET in this work combine a superior electrostatic design based on RESURF principles and a novel fabrication process flow, which makes it an attractive power transistor concept that can be applied to any wide band gap semiconductors.

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References

[1] M. Higashiwaki, A. Kuramata, H. Murakami and Y. Kumagai, "State-of-the-art technologies of gallium oxide power devices", J. Phys. D: Appl. Phys. Vol. 50, pp. 333002-1-12, July 2017.

[2] N. Ma, N. Tanen, A. Verma, Z. Guo, T. Luo, H. G. Xing and D. Jena, "Intrinsic electron mobility limits in β-Ga_2O_3", Appl. Phys. Lett., Vol. 109, pp. 212101-1-5, Nov. 2016.

[3] T. Oishi, Y. Koga, K. Harada and M. Kasu, "High-mobility β-Ga_2O_3 (-201) single crystals grown by edge-defined film-fed growth method and their Schottky barrier diodes with Ni contact", Appl. Phys. Express, Vol. 8, pp. 031101-1-3, Feb. 2015.

[4] E. G. Villora, K. Shimamura, Y. Yoshikawa, K. Aoki and No. Ichinose, "Large-size β-Ga_2O_3 single crystals and wafers", J. Crystal Growth, Vol. 270, pp. 420-426, Aug. 2004.

[5] M. Baldini, M. Albrecht, A. Fiedler, K. Irmscher, R. Schewski and G. Wagner, "Si- and Sn-Doped Homoepitaxial β-Ga_2O_3 Layers Grown by MOVPE on (010)-Oriented Substrates", ECS J. Solid State Sci. Tech., Vol. 6, No. 2, pp. Q3040-Q3044, Oct. 2016.

[6] H. Murakami, K. Nomura, K. Goto, K. Sasaki, K. Kawara, Q. T. Theiu et al, "Homoepitaxial growth of β-Ga_2O_3 layers by halide vapor phase epitaxy", Appl. Phys. Express, Vol. 8, pp. 015503-1-4, Dec. 2014.

[7] K. Konishi, K. Goto, H. Murakami, Y. Kumagai, A. Kuramata, S. Yamakoshi and M. Higashiwaki, "1-kV vertical Ga_2O_3 field-plated Schottky barrier diodes", Appl. Phys. Lett., Vol. 110, pp. 103506-1-4, Mar. 2017.

[8] K. Zeng, A. Vaidya and U. Singisetti, "1.85 kV Breakdown Voltage in Lateral Field-Plated Ga_2O_3 MOSFETs", IEEE Electron Device Lett., Vol. 39, No. 9, pp. 1385-1388, Sept. 2018.

[9] Z. Hu, K. Nomoto, W. Li, L. J. Zhang, J.-H. Shin, N. Tanen, T. Nakamura, D. Jena and H. G. Xing, "Vertical fin Ga_2O_3 power field effect transistors with on/off ratio > 10^9", Device Research Conf. (DRC), pp. 1-3, June 2017.

[10] Z. Hu, K. Nomoto, W. Li, N. Tanen, K. Sasaki, A. Kuramata, D. Jena and H. G. Xing, "Enhancement-mode Ga_2O_3 Vertical Transistors With Breakdown Voltage > 1kV", IEEE Electron Device Lett., Vol. 39, No. 6, pp. 869-872, June 2018.

[11] W. Li, Z. Hu, K. Nomoto, Z. Zhang, J.-Y. Hsu, Q. T. Thieu, K. Sasaki, A. Kuramata, D. Jena and H. Xing, "1230 V β-Ga_2O_3 trench Schottky barrier diodes with an ultra-low leakage current of < 1 $\mu A/cm^2$", Appl. Phys. Lett., Vol. 113, pp. 202101-1-5, Nov. 2018.

[12] W. Li, Z. Hu, K. Nomoto, R. Jinno, Z. Zhang, T. Q. Tu, K. Sasaki, A. Kuramata, D. Jena and H. Xing, "2.44 kV Ga_2O_3 vertical trench Schottky barrier diodes with very low reverse leakage current", IEEE IEDM digest, pp. 8.5.1-8.5.4, Dec. 2018.

[13] Z. Hu, K. Nomoto, W. Li, Z. Zhang, N. Tanen, Q. T. Thieu, K. Sasaki, A. Kuramata, T. Nakamura, D. Jena and H. Xing, "Breakdown mechanism in 1 kA/cm^2 and 960 V E-mode β-Ga_2O_3 vertical transistors", Appl. Phys. Lett., Vol. 113, pp. 122103-1-5, Sept. 2018.

[14] Y. Zhang, M. Sun, D. Piedra, J. Hu, Z. Liu, Y. Lin, X. Gao, K. Shepard and T. Palacios, "1200 V GaN Vertical Fin Power Field-Effect Transistors", IEEE IEDM digest, pp. 9.2.1-9.2.4, Dec. 2017.

[15] B. J. Baliga, "Fundamentals of Power Semiconductor Devices", Chapter 3, New York, NY, USA: Springer-Verlag, 2008.

[16] H. Fukushima, S. Usami, M. Ogura, Y. Ando, A. Tanaka, M. Deki et al, "Vertical GaN p-n diode with deeply etched mesa and the capability of avalanche breakdown", Appl. Phys. Express, Vol. 12, pp. 026502-1-4, Feb. 2019.

[17] J. W. McPherson, "Time dependent dielectric breakdown physics – Models resisited", Micro. Reliability, Vol. 52, pp. 1753-1760, July, 2012.

[18] W. S. Hwang, A. Verma, H. Peelaers, V. Protasenko, S. Rouvimov, H. G. Xing, A. Seabaugh, W. Haensch, C. Van de Walle, Z. Galazka, M. Albrecht, R. Fornari and D. Jena, "High-voltage field effect transistors with wide-bandgap β-Ga_2O_3 nanomembranes", Appl. Phys. Lett., Vol. 104, pp. 203111-1-5, May 2014.

[19] W. S. Hwang, A. Verma, V. Protasenko, S. Rouvimov, H. G. Xing, A. Seabaugh, W. Haensch, C. Van de Walle, Z. Galazka, M. Albrecht, R. Forrnari and D. Jena, "Nanomembrane β-Ga_2O_3 High-Voltage Field Effect Transistors", Device Research Conf. (DRC), pp. 207-208, June 2013.

[20] M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui and S. Yamakoshi, "Gallium oxide (Ga_2O_3) metal-semiconductor field-effect transistors on single-crystal β-Ga_2O_3 (010) substrates", Appl. Phys. Lett., Vol. 100, pp. 013504-1-3, Jan. 2012.

[21] M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi and M. Higashiwaki, "Field-Plated Ga_2O_3 MOSFETs With a Breakdown Voltage of Over 750 V", IEEE Electron Device Lett., Vol. 37, No. 2, pp. 212-215, Feb. 2016.

[22] A. J. Green, K. D. Chabak, E. R. Heller, R. C. Fitch, M. Baldini, A. Fiedler, K. Irmscher, G. Wagner, Z. Galazka, S. E. Tetlak, A. Crespo, K. Leedy and G. H. Jessen, "3.8 MV/cm breakdown strength of MOVPE-Grown Sn-Doped β-Ga_2O_3 MOSFETs", IEEE Electron Device Lett., Vol. 37, No. 7, pp. 902-905, July 2016.

[23] N. Moser, J. McCandless, A. Crespo, K. Leedy, A. Green, A. Neal, S. Mou, E. Ahmadi, J. Speck, K. Chabak, N. Peixoto and G. Jessen, "Ge-Doped β-Ga_2O_3 MOSFETs", IEEE Electron Device Lett., Vol. 38, No. 6, pp. 775-778, June 2017.

[24] K. D. Chabak, J. P. McCandless, N. A. Moser, A. J. Green, K. Mahalingam, A. Crespo, N. Hendricks, B. M. Howe, S. E. Tetlak, K. Leedy, R. C. Fitch, D. Wakimoto, K. Sasaki, A. Kuramata and G. H. Jessen, "Recessed-Gate Enhancement-Mode β-Ga_2O_3 MOSFETs", IEEE Electron Device Lett., Vol. 39, No. 1, pp. 67-70, Jan. 2018.

[25] K. Zeng, J. S. Wallace, C. Heimburger, K. Sasaki, A. Kuramata, T. Masui, J. A. Gardella Jr. and U. Singisetti, "Ga_2O_3 MOSFETs using Spin-On-Glass Source/Drain Doping Technology", IEEE Electron Device Lett., Vol. 38, No. 4, pp. 513-516, Apr. 2017.

[26] H. Zhou, M. Si, S. Alghamdi, G. Qiu, L. Yang and P. D. Ye, "High-Performance Depletion/Enhancement-Mode β-Ga_2O_3 on Insulator (GOOI) Field-Effect-Transistors With Record Drain Currents of 600/450 mA/mm", IEEE Electron Device Lett., Vol. 38, No. 1, pp. 103-106, Jan. 2017.

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