Applied Physics Express 12, 061007 (2019)
https://doi.org/10.7567/1882-0786/ab206c

LETTER

Fin-channel orientation dependence of forward conduction in kV-class Ga_2O_3 trench Schottky barrier diodes

Wenshen Li[1*], Kazuki Nomoto[1], Zongyang Hu[1], Debdeep Jena[1,2,3], and Huili Grace Xing[1,2,3*]

[1]School of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14853, United States of America
[2]Department of Materials Science and Engineering, Cornell University, Ithaca, New York 14853, United States of America
[3]Kavli Institute for Nanoscale Science, Cornell University, Ithaca, New York 14853, United States of America

*E-mail: wl552@cornell.edu; grace.xing@cornell.edu

Received April 13, 2019; revised April 27, 2019; accepted May 8, 2019; published online May 23, 2019

Ga_2O_3 vertical trench Schottky barrier diodes with four different fin-channel orientations are realized on (001) substrates and compared. Fin-channels along the [010] direction with (100)-like sidewalls result in the highest forward current, while other channel orientations all lead to a shallow turn-on behavior and much lower forward current, indicative of severe sidewall depletion attributed to negative interface charges. The comparison indicates that the interface charge density is the smallest on the (100)-like surfaces. The breakdown voltage of the diodes with 1-μm fin width is around 2.4 kV, with no apparent dependence on the channel orientation. © 2019 The Japan Society of Applied Physics

β-Ga_2O_3 has attracted considerable interest as a promising wide-bandgap semiconductor material for high power devices. Aside from the availability of melt-grown substrates,[1)] the sizable bandgap value of 4.5–4.7 eV allows for a large critical electric field exceeding 5 MV cm^{-1} as experimentally observed.[2–6)] Aided by the excellent field strength, high breakdown voltages exceeding 1 kV have been demonstrated in both diodes[3,6–11)] and transistors.[12,13)] In addition, a Baliga's figure-of-merit (BFOM) of around 0.5 GW cm^{-2} has been achieved in both lateral[11)] and vertical Schottky barrier diodes (SBDs),[6)] which already exceeded the unipolar limit of Si.

Vertical power devices can provide higher current density than the lateral counterparts. For high voltage applications, vertical power devices typically involve the use of p-type doping. However, p-type doping in Ga_2O_3 remains elusive due to the lack of shallow acceptors.[14)] Alternatively, vertical fin-channels with metal-insulator-semiconductor (MIS) structure covering the fin sidewall can be used in vertical power devices without the need for p-type doping.[15,16)] With the incorporation of fin-channels, vertical enhancement-mode Ga_2O_3 transistors with good gate-control[12,17)] as well as vertical Ga_2O_3 trench Schottky barrier diodes with reduced reverse leakage current[6,9,10,18)] have been realized.

In vertical fin-channel devices, the sidewall interface quality of the MIS-junction is of high importance to the device performance. We have shown that interface trapping at the fin sidewall can exacerbate drain-induced barrier lowering (DIBL) effects in vertical fin transistors.[17)] In trench SBDs, the interface trapping is found to induce hysteresis in the forward conduction.[10)] Due to the low symmetry nature of β-Ga_2O_3, this issue may be compounded by different behaviors associated with different fin-channel/sidewall orientations. Previous studies on Schottky contacts have suggested that differences exist in surface-state distribution on different β-Ga_2O_3 surfaces.[19)] In this study, we compare the electrical characteristics of trench SBDs with different fin-channel/sidewall orientations. A strong influence of the orientation on the forward conduction has been observed and is linked with the difference in interface charge density at the fin sidewall. The study highlights the importance of sidewall interface quality in vertical fin-channel devices and provides importance guidance on the choice of fin-channel orientations in β-Ga_2O_3.

The schematic cross-section of the trench SBDs under study is shown in Fig. 1(a). The diodes have a trench-depth (d_{tr}) of 1.55 μm and fin channel widths (W_{fin}) ranging from 1 μm to 4 μm. The area ratio (*A.R.*) of the fin channel over the entire anode area can be calculated by W_{fin} divided by the pitch size. The diodes are fabricated on (001) Ga_2O_3 substrates, on which a 10 μm drift layer is grown by halide vapor phase epitaxy (HVPE) with a net doping concentration of $\sim 2 \times 10^{16}$ cm^{-3}. The fabrication process is described in Ref. 6. The fin channels were formed by dry-etch using a gas mixture of BCl_3 and Ar. The wafer was then soaked in HCl and HF each for 20 min to remove the etch damage, before the subsequent processes. The MIS-junction consists of a 100-nm Al_2O_3 layer deposited at 300 °C using a plasma atomic layer deposition (ALD) system. Along with the fabrication of the trench SBDs, regular SBDs with and without mesa structure together with MOS-capacitors were co-fabricated on the same wafer, as shown in Figs. 1(b)–1(d). The forward *I*–*V* characteristics of the diodes were measured under pulsed condition to avoid self-heating,[10)] while the reverse *I*–*V* characteristics were measured under the DC condition.

The sidewall interface quality is first examined in the circular-shaped regular SBDs. Figure 2 shows the comparison of the forward *I*–*V* characteristics between the SBDs with mesa and the SBDs without mesa. The current is normalized by the area of the Schottky contact, which in the SBDs with mesa has a diameter 6 μm smaller than that of the mesa. In the SBDs without mesa, the current density increases with decreasing diodes diameter thanks to current spreading [see Fig. 3(b)]. In comparison, the current density of the SBDs with mesa has the opposite trend. Figure 3(a) shows the extracted differential specific on-resistance ($R_{on,sp}$) from both types of diodes, which clearly exhibits opposite trends with the diode diameter. Since the only difference in conduction path between the two types of diodes is the mesa region, it can be concluded that the conductance of the mesa region does not scale linearly with the Schottky contact area. This suggests that there exists a sidewall depletion region due to surface band-bending along the periphery of the mesa, as shown by the illustration in Fig. 3(b). Since there is a 3 μm gap between the edge of the Schottky contact and the edge of the mesa, the *average* depletion width should be larger than 3 μm. Using the measured net doping concentration of

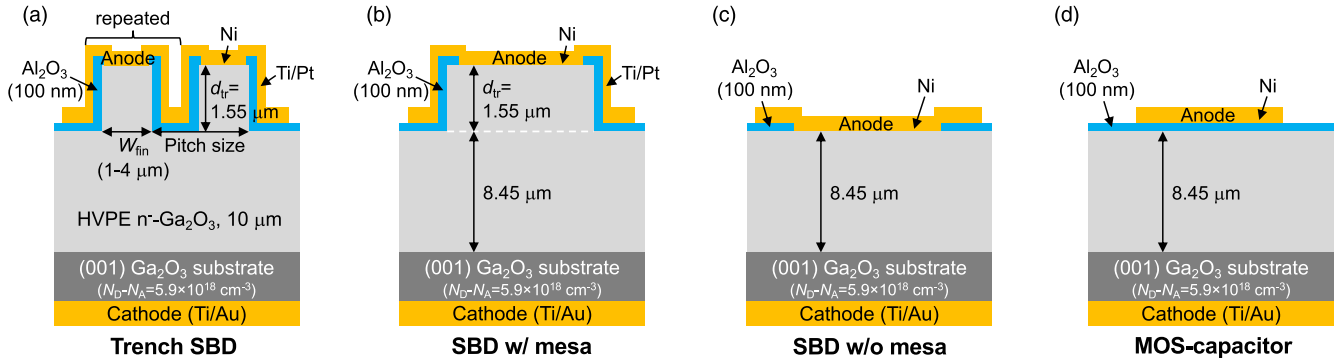

Fig. 1. (Color online) Schematic cross-sections of the devices fabricated on the same wafer: (a) trench Schottky barrier diodes (SBDs), (b) regular SBDs with mesa, (c) regular SBDs without mesa, (d) MOS-capacitors.

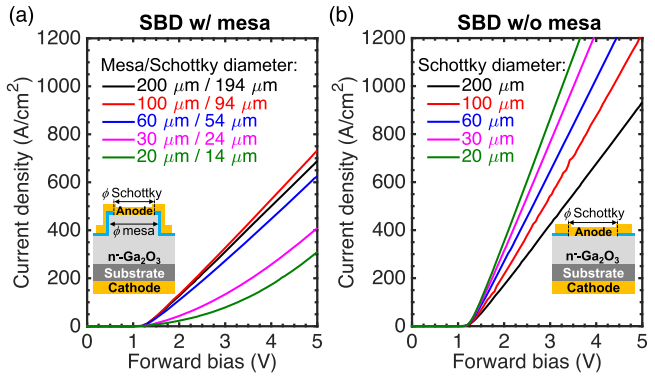

Fig. 2. (Color online) Forward *I*–*V* characteristics of (a) regular SBDs with mesa and (b) regular SBDs without mesa. The current is normalized by the Schottky contact area. Measurements are taken under pulsed condition with a pulse width of 8.4 μs and a duty cycle of 0.84%.

$\sim 7 \times 10^{15}\,\mathrm{cm}^{-3}$ near the surface (see Ref. 6), a minimum negative interface charge density of $2.1 \times 10^{12}\,\mathrm{cm}^{-2}$ can be estimated by assuming the depleted space-charge is balanced by the negative interface charge. This value is similar with the extracted interface charge density on etched (001) surface.[10] The fixed charge density within the Al_2O_3 dielectric is extracted to be around $+1 \times 10^{11}\,\mathrm{cm}^{-2}$ from the measured capacitance of the MOS-capacitor at zero bias, thus not contributing to the sidewall depletion.

As shown in our previous work,[6] trench SBDs fabricated on the same wafer with the fin-channels orientated along the [010] direction—hence (100)-like sidewalls—have normal turn-on behaviors, similar to the SBDs without mesa, as shown in Fig. 2(b). These trench SBDs show a turn-on voltage (V_{on}) of 1.25 V, and their differential $R_{on,sp}$ is found to have an ideal dependence on the fin area ratio, which means an absence of appreciable sidewall depletion beyond V_{on}. We can estimate the upper limit of negative interface charge density ($N_{int,max}$) on those (100)-like sidewalls with this simple expression:

$$N_{\mathrm{int,max}} = \frac{\varepsilon_{\mathrm{ox}} V_{\mathrm{on}}}{e d_{\mathrm{ox}}},$$

where e is the electron charge, $\varepsilon_{ox} = 8.2\varepsilon_0$ is the dielectric constant of the Al_2O_3, d_{ox} is the thickness of the Al_2O_3 layer. From this equation, $N_{int,max}$ is calculated to be $6 \times 10^{11}\,\mathrm{cm}^{-2}$, which is about 1/4 of the afore-estimated minimum average interface charge density on the mesa sidewalls in the circular SBDs with mesa [Fig. 2(a)]. *This discrepancy can only be explained by a dependence of interface charge density on sidewall orientations.*

To verify this, we measure trench SBDs with four different fin-channel/sidewall orientations fabricated on the same wafer. Figure 4 shows the schematic top view of the device footprint and the scanning electron microscopy (SEM) images of the fin-channel cross-sections. Trench SBDs we previously reported all have fin-channels oriented along the [010] direction—as shown by the scenario in Fig. 4(a),[6,9,10] which we use as the reference direction. The other three fin-channel orientations are rotated 30°, 60°, and 90°, respectively, with respect to the [010] reference direction. SEM

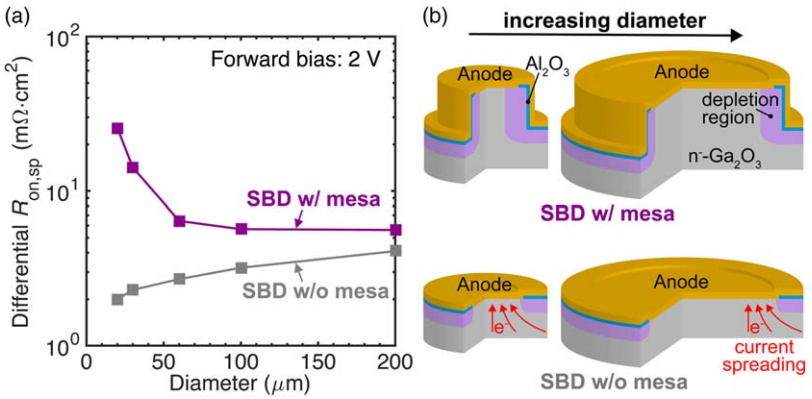

Fig. 3. (Color online) (a) Differential specific on-resistance ($R_{on,sp}$) *versus* the diode diameter for the regular SBDs with and without mesa. (b) Illustration of the sidewall depletion responsible for the increase of $R_{on,sp}$ with decreasing diameter in SBDs with mesa, as well as the current spreading responsible for the decrease of $R_{on,sp}$ with decreasing diameter in SBDs without mesa.

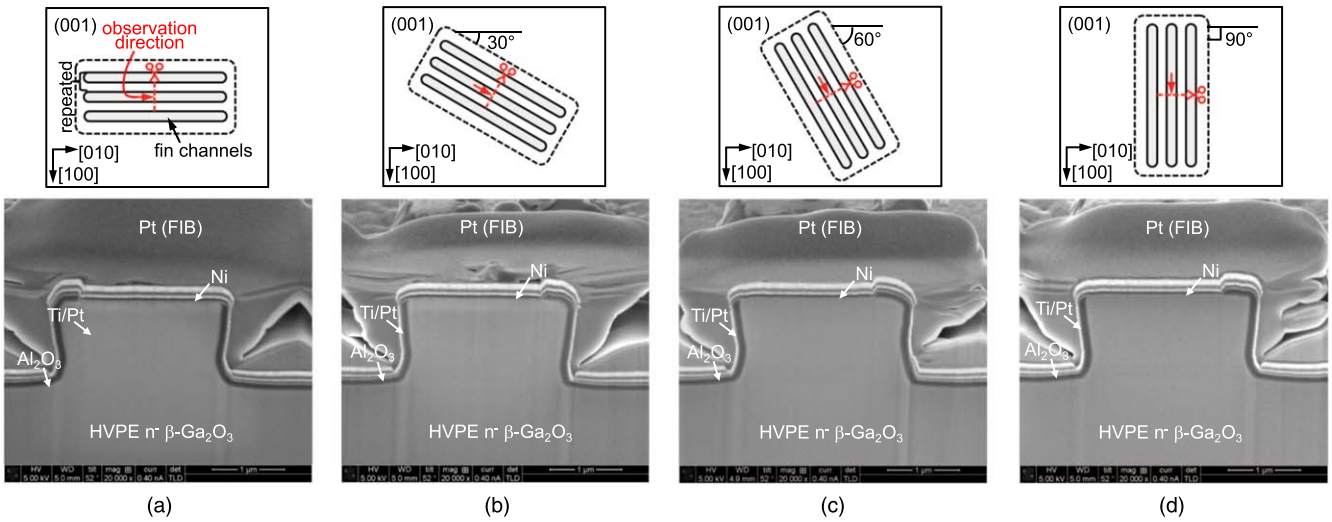

Fig. 4. (Color online) Scanning electron microscopy (SEM) cross-sectional images of the trench SBDs with different fin orientations: (a) along the [010] direction (0° rotation), (b) 30° rotation, (c) 60° rotation and (d) along the [100] direction (90° rotation). The cross-section cutline positions are indicated by the red dashed lines, while the viewing directions by the red arrows in the schematic top-view cartoons. The viewing angle of the SEM is 52° from the norm of the sample top surface.

images of all cross-sections show similar channel profile, featuring slightly inward-slanted sidewall with a sidewall angle of 95°–97° and smooth trench bottom corners. Thus, the channel morphology alone should not cause a large difference in device characteristics.

Figure 5 shows the forward *I*–*V* characteristics of the trench SBDs with different fin-widths and channel orientations. Devices with the reference orientation and thus (100)-like sidewall shows a normal turn-on behavior. The barrier height is extracted to be 1.38 eV from the thermionic emission model and the ideality factor is 1.06 at 295 K. The $R_{on,sp}$ of the diodes with $W_{fin} = 2$–4 μm is 10 m$\Omega \cdot$ cm^2, while the $R_{on,sp}$ of the diodes with $W_{fin} = 1$ μm is ~20 mΩ·cm^2. The difference in $R_{on,sp}$ is mainly due to the different fin area ratio. Aside from the reference orientation, the other three sidewall orientations all lead to a shallow turn-on behavior and much lower on-currents, indicating the presence of significant sidewall-depletion due to interface charge. The worst case is when the fin sidewalls are (010)-like. Similar shallow turn-on behavior has also been observed in etched fin channels with slanted sidewall profile by Ref. 5, but the sidewall orientation was not specified. Since devices with $W_{fin} = 4$ μm and (010)-like sidewalls also show the shallow turn-on behavior, the sidewall-depletion width must be larger than 2 μm, which is consistent with the observations from the regular SBDs with mesa.

The cause of the negative interface charge on the sidewalls is likely from dry-etch-induced surface damage, which might not be fully-removed by the wet etch using acids. Although, F incorporation during the wet etch in HF may also introduce negative charges,[3)] we do not believe it is the main reason, since we observed similar sidewall-depletion and fin-orientation dependence in devices without wet etch on another wafer. The surface damage likely induces acceptor-like deep states, which lead to negative interface charges and surface band-bending. The existence of upward surface band-bending of 1.63 eV on chemical-mechanical polished (CMP-ed) (010)-surface has indeed been observed with X-ray photoelectron spectroscopy (XPS) by Ref. 19, corresponding to a negative surface charge density of 8.8×10^{12} cm^{-2}. Reference 19 also showed that the (010) surface has a larger surface band-bending and Schottky barrier height than the $(\bar{2}01)$ surface.[19)] In fact, the Schottky barrier of the same metal contact on the (010) surface has been reported to be generally higher than on other surfaces,[19–22)] while the Schottky barrier on the (100) surface

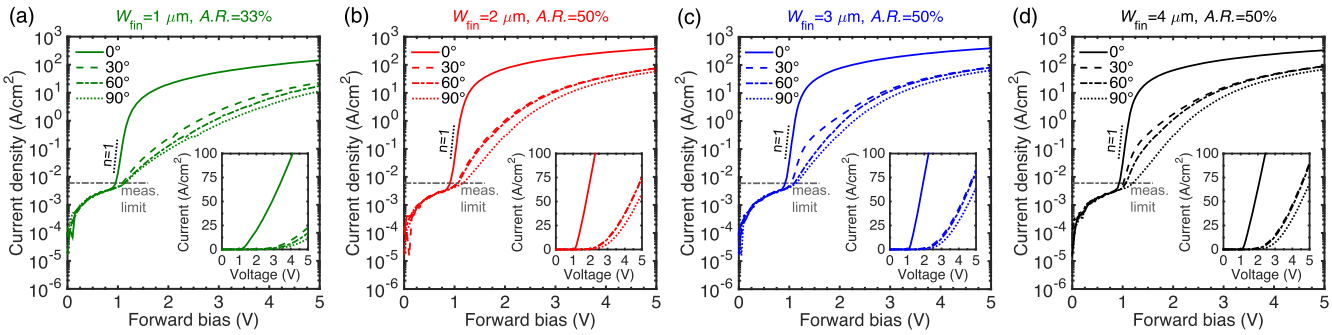

Fig. 5. (Color online) Forward *I*–*V* characteristics of the trench SBDs with different fin-widths (W_{fin}) and fin-channel orientations: (a) $W_{fin} = 1$ μm, fin area ratio ($A.R.$) = 33%; (b) $W_{fin} = 2$ μm, $A.R.$ = 50%; (c) $W_{fin} = 3$ μm, $A.R.$ = 50%; (d) $W_{fin} = 4$ μm, $A.R.$ = 50%. All *I*–*V* curves are measured from fresh upward scans under the same pulsed conditions used in the measurements of the regular SBDs. Below the measurement limit, the pulsed *I*–*V* curves are the same for all devices since they are limited by the system charging time. In diodes with fin-channels orientated along the [010] direction (0° rotation), the semi-log *I*–*V* characteristics under DC sweep (not shown) are similar to our earlier report.[6)]

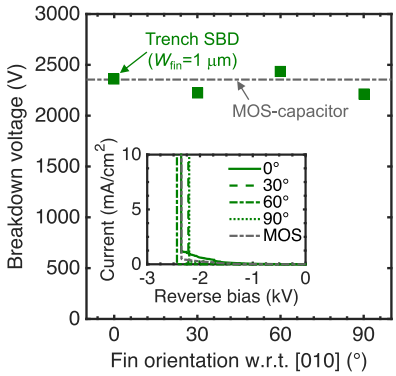

Fig. 6. (Color online) Breakdown voltage of the trench SBDs with 1-μm channel width with respect to the fin orientation angle, in comparison with the breakdown voltage of the MOS-capacitor. The inset shows the corresponding reverse *I*–*V* characteristics.

is among the lowest.[11,23,24] This may be correlated with the difference in surface band-bending and the corresponding surface charge density, as the barrier height appears strongly influenced by Fermi-level pinning in β-Ga_2O_3.[20,25] The lowest interface charge density on the (100)-like surfaces indicates that this surface may be least susceptible to surface damage, which is likely linked with easy exfoliation of (100)-oriented β-Ga_2O_3 flakes due to the strong in-plane covalent bonds and weak perpendicular bonds.[26] On the other hand, it is worth noting another distinct possibility that the dry-etch-induced surface damage is sufficiently removed by our wet-etch treatments, therefore, the crystallographic orientation dependence of surface/interface charge densities is inherent in β-Ga_2O_3. The exact mechanism behind the crystallographic orientation dependence requires further study, especially on pristine β-Ga_2O_3 surfaces such as epitaxially grown surfaces that are not subject to CMP, dry etch and so on. Nearly all studies in the literature to date have been carried out on β-Ga_2O_3 surfaces that were CMP-ed or etched, except the exfoliated (100) flakes.

The reverse characteristics of the trench SBDs with a 1-μm fin width is shown in Fig. 6. The breakdown voltage (BV) for all fin-orientations is around 2.4 kV, similar with the BV of the MOS-capacitor. It suggests that the breakdown of the devices with a 1-μm fin width maybe limited by field crowding at the device periphery, whereas for larger fin widths the breakdown voltage is shown to be limited by field-crowding at the trench corners.[6] The lack of fin-orientation dependence is as-expected since the presence of the negative interface charge at the fin sidewall will not exacerbate the field crowding at the trench corners.

In conclusion, we identified the presence of sidewall-depletion at etched mesa sidewalls on (001) β-Ga_2O_3 wafers. The sidewall-depletion is attributed to negative interface charges, likely induced by dry-etch-induced surface damage. The forward *I*–*V* characteristics of trench SBDs with four different fin-channel orientations are compared. Trench SBDs with (100)-like sidewall have near-ideal turn-on behaviors, while all other orientations lead to a shallow turn-on behavior and a much lower current density. It suggests that the interface charge density on the etched (100)-like surface is much lower than on other sidewall surfaces. The reverse breakdown characteristics are not influenced by the fin-orientation. The study identifies the significant impact of the sidewall interface quality in vertical fin-channel devices and reveals the superiority of the (100)-like β-Ga_2O_3 surfaces in the presence of surface damage. Whether this crystallographic dependence is native to β-Ga_2O_3 requires further investigation.

Acknowledgments This work was supported in part by the NSF DMREF Program under Grant 1534303, AFOSR under Grants FA9550-17-1-0048, FA9550-18-1-0529 and FA9550-18-1-0479. The device fabrication was carried out at the Cornell Nanoscale Science and Technology Facilities (CNF) sponsored by the NSF NNCI program (ECCS-1542081). This work made use of the Cornell Center for Materials Research Shared Facilities which are supported through the NSF MRSEC program (DMR-1719875).

1) A. Kuramata, K. Koshi, S. Watanabe, Y. Yamaoka, T. Masui, and S. Yamakoshi, Jpn. J. Appl. Phys. **55**, 1202A2 (2016).
2) A. J. Green et al., IEEE Electron Device Lett. **37**, 902 (2016).
3) K. Konishi, K. Goto, H. Murakami, Y. Kumagai, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, Appl. Phys. Lett. **110**, 103506 (2017).
4) X. Yan, I. S. Esqueda, J. Ma, J. Tice, and H. Wang, Appl. Phys. Lett. **112**, 032101 (2018).
5) C. Joishi, S. Rafique, Z. Xia, L. Han, S. Krishnamoorthy, Y. Zhang, S. Lodha, H. Zhao, and S. Rajan, Appl. Phy. Express **11**, 031101 (2018).
6) W. Li, Z. Hu, K. Nomoto, R. Jinno, Z. Zhang, T. Q. Tu, K. Sasaki, A. Kuramata, D. Jena, and H. G. Xing, IEEE Int. Electron Devices Meeting (IEDM), 2018, p. 8.5.1.
7) J. Yang, S. Ahn, F. Ren, S. J. Pearton, S. Jang, J. Kim, and A. Kuramata, Appl. Phys. Lett. **110**, 192101 (2017).
8) J. Yang, S. Ahn, F. Ren, S. J. Pearton, S. Jang, and A. Kuramata, IEEE Electron Device Lett. **38**, 906 (2017).
9) W. Li, K. Nomoto, Z. Hu, N. Tanen, K. Sasaki, A. Kuramata, D. Jena, and H. G. Xing, Proc. 76th Annu. Device Research Conf. (DRC), 2018, p. 1.
10) W. Li, Z. Hu, K. Nomoto, Z. Zhang, J. Y. Hsu, Q. T. Thieu, K. Sasaki, A. Kuramata, D. Jena, and H. G. Xing, App. Phys. Lett. **113**, 202101 (2018).
11) Z. Hu et al., IEEE Electron Device Lett. **39**, 1564 (2018).
12) Z. Hu, K. Nomoto, W. Li, N. Tanen, K. Sasaki, A. Kuramata, T. Nakamura, D. Jena, and H. G. Xing, IEEE Electron Device Lett. **39**, 869 (2018).
13) K. Zeng, A. Vaidya, and U. Singisetti, IEEE Electron Device Lett. **39**, 1385 (2018).
14) A. Kyrtsos, M. Matsubara, and E. Bellotti, Appl. Phys. Lett. **112**, 032108 (2018).
15) M. Mehrotra and B. J. Baliga, Proc. IEEE Int. Electron Devices Meeting, Proc. IEEE Int. Electron Devices Meeting, Proc. IEEE Int. Electron Devices Meeting, Proc. IEEE Int. Electron Devices Meeting, 1993, p. 675.
16) Y. Zhang, M. Sun, D. Piedra, J. Hu, Z. Liu, Y. Lin, X. Gao, K. Shepard, and T. Palacios, IEEE Int. Electron Devices Meeting (IEDM), 2017, p. 9.
17) Z. Hu et al., Appl. Phys. Lett. **113**, 122103 (2018).
18) K. Sasaki, D. Wakimoto, Q. T. Thieu, Y. Koishikawa, A. Kuramata, M. Higashiwaki, and S. Yamakoshi, IEEE Electron Device Lett. **38**, 783 (2017).
19) H. Fu, H. Chen, X. Huang, I. Baranowski, J. Montes, T. H. Yang, and Y. Zhao, IEEE Trans. Electron Devices **65**, 3507 (2018).
20) Y. Yao, R. Gangireddy, J. Kim, K. K. Das, R. F. Davis, and L. M. Porter, J. Vac. Sci. Technol. B **35**, 03D113 (2017).
21) C. Hou, R. M. Gazoni, R. J. Reeves, and M. W. Allen, IEEE Electron Device Lett. **40**, 337 (2019).
22) C. Hou, R. M. Gazoni, R. J. Reeves, and M. W. Allen, Appl. Phys. Lett. **114**, 033502 (2019).
23) Q. He et al., IEEE Electron Device Lett. **39**, 556 (2018).
24) M. Mohamed, K. Irmscher, C. Janowitz, Z. Galazka, R. Manzke, and R. Fornari, Appl. Phys. Lett. **101**, 132106 (2012).
25) E. Farzana, Z. Zhang, P. K. Paul, A. R. Arehart, and S. A. Ringel, Appl. Phys. Lett. **110**, 202102 (2017).
26) S. K. Barman and M. N. Huda, Phys. Status Solidi RRL **13**, 1800554 (2019).