A Single-Device Embodiment of XNOR Logic: TransiXNOR

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Introduction: In most digital circuits and systems, transistors are engineered only for simple switching. Much recent research has focused on developing novel transistors as efficient switches [1]. On the other hand, a single transistor can also be designed to achieve richer functionalities. By taking advantage of the ambipolar behavior of tunnel field-effect transistors (TFETs), in this paper we propose a device concept, TransiXNOR, which is a dual-gate four-terminal transistor implementing XNOR logic within a single device.

Device Structure and Working Principle: The schematic structure of a TransiXNOR is shown in Fig.1(a). The structure resembles a dual-gate three-terminal TFET, but with three major differences: 1) top and bottom gates are biased independently; 2) channel is thin enough for two gates to control the same conducting channel; 3) tunnel injection is controlled at either source or drain. The working principle can be understood with the cartoons shown in Fig.1(b) at $V_{DS} = V_{DD}$. When both top and bottom gates are zero biased (V_{TG}=V_{BG}=0V, *left panel*), the channel is electrostatically p-doped such that the valence band edge of channel is above the conduction band edge of drain. Therefore, the channel-drain tunnel junction (under reverse bias) is ON. Together with the forward-biased source-channel junction, the transistor allows current to flow between source and drain. On the other hand, when V_{TG}=V_{BG}=V_{DD} (*right panel*), the conduction band edge of channel is below the valence band edge of source, thus the source-channel tunnel junction is ON and current can flow. However, when both top and bottom gates are at $V_{DD}/2$, or one gate is at V_{DD} and the other is at zero (*middle panel*), both source and drain junctions are OFF, thus no current flows. If we map the TransiXNOR ON/OFF states with respect to V_{TG} and V_{BG} at $V_{DS} = V_{DD}$(shown in Fig.1(c)), the TransiXNOR is ON only when V_{TG} and V_{BG} are either both low or both high, while staying OFF otherwise. This behavior is precisely the XNOR logic.

Simulation, Results and Discussion: For the numerical simulation of TransiXNOR, semiconducting 2 quintuple-layer (2QL) Bi_2Se_3[2] is chosen as the channel material, with device structure shown in Fig.1(a). The material parameters for Bi_2Se_3 and gate dielectric are shown in Tab.1, adopted from the Bi_2Se_3 TFET simulation work by Zhang et al. [3]. Ballistic transport is solved self-consistently with the 2D Poisson equation, within the Non-Equilibrium Green's function (NEGF) formalism, using the NanoTCAD ViDES simulation environment[4], which is the same as Ref. [3]. The gate length is 18 nm and source/drain lengths are 10 nm. The workfunction of both gate metals is carefully chosen to achieve minimal OFF current and symmetric ambipolar behavior. The supply voltage V_{DD} is set at 0.2 V. Fig.2 upper row shows the TransiXNOR I_{DS}-V_{TG} transfer characteristics under three different V_{BG} ($V_{DS} = V_{DD}$). Fig.2 lower row shows the band diagrams under three specific bias conditions, which is the same three distinctive operation regimes shown in Fig. 1(b). The results show that the simulated device follows designed working principle, exhibiting the XNOR logic. The output characteristics (I_{DS}-V_{DS}) and band diagrams of specific relevant bias conditions are shown in Fig.3. For V_{BG}=0.2 V, the output characteristics resemble that of ordinary n-type TFETs (Fig.3(a.1)). This can be understood using the simulated band diagrams in Fig.3(b.1): tunneling happens at the source-channel junction. At low V_{DS}, most of V_{DS} is dropped over the source-channel junction due to its high junction resistance. At higher V_{DS}, most of V_{DS} is dropped over the channel-drain junction thus leading to a saturated I_{DS}, which gives a typical n-type TFET behavior. However, for V_{BG}=0 V, the output characteristics resemble that of diodes (Fig.3(a.2)). This can be explained by the simulated band diagrams in Fig.3(b.2): tunneling happens at the channel-drain junction, over which V_{DS} is largely dropped in its entire range. This inevitably affects the tunneling energy window of the channel-drain tunnel junction, thus channel-drain junction effectively acts as a reversed-biased Zener diode. A grid of drain current maps with different V_{TG} and V_{BG} at different V_{DS} is shown in Fig.4. The color scheme represents drain current density (μA/μm) in log scale. Because of the diode-like output characteristics stemming from the channel-drain tunnel junction, TransiXNOR establishes XNOR behavior when $V_{DS} > V_{DD}/2$ but AND behavior when $V_{DS} < V_{DD}/2$.

Conclusion: In this work, a single-device embodiment of XNOR logic, TransiXNOR, is designed and simulated. With double gates controlling the current tunneling plane either at the source or at the drain, the TransiXNOR is ON if and only if the dual gates are biased at both high or low voltage, thus the XNOR logic.

Acknowledgment: This work is supported by SRC nCORE task 2758.001 and NSF E2CDA program (ECCS 1740286). The authors thank Qin Zhang for helpful discussions.

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Parameter	Value
Channel (Bi_2Se_3) thickness	1.4 nm
Bi_2Se_3 dielectric constant (ϵ_r)	100
Bi_2Se_3 bandgap	0.252 eV
Bi_2Se_3 electron/hole effective mass	0.124/2.23 m_0
Source region p-doped concentration	5.5×10^{13} cm^{-2}
Drain region n-doped concentration	3.8×10^{12} cm^{-2}
Gate dielectric (HfO_2) thickness	1.1 nm
Gate dielectric (HfO_2) permittivity	25

Table 1: Bi_2Se_3 and gate dielectric related parameters used in the numerical simulation adopted from [2].

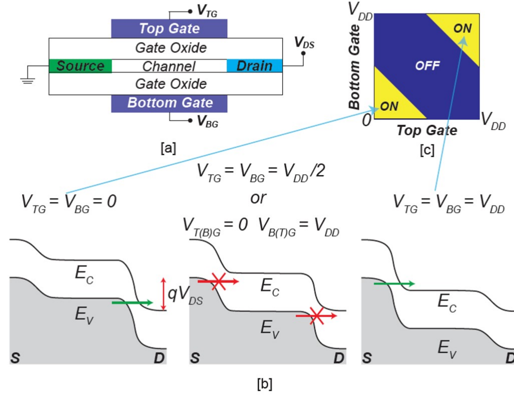

Fig. 1: TransiXNOR working principle: (a) schematic device structure; (b) schematic band diagrams at V_{DS}=V_{DD}, representing three distinctive operation regimes; (c) schematic mapping of ON/OFF states at different V_{TG} and V_{BG} when V_{DS}=V_{DD}, which is XNOR logic.

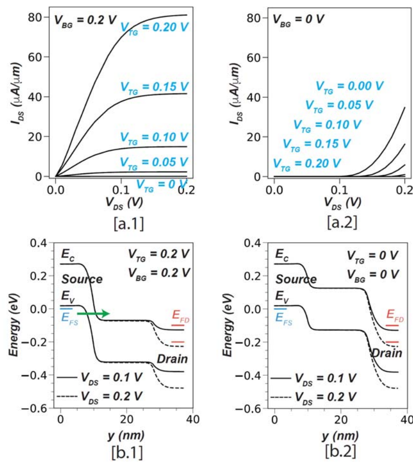

Fig. 3: Simulated family output characteristics (I_{DS}-V_{DS}) with various V_{TG} at (a.1) V_{BG}=0.2 V; (a.2) V_{BG}=0 V. (b.1) Band diagram when V_{TG}=V_{BG}=0.2 V, and V_{DS}=0.1 V (solid line) or 0.2 V (dash line); (b.2) band diagram when V_{TG}=V_{BG}=0 V, and V_{DS}=0.1 V (solid line) or 0.2 V (dash line).

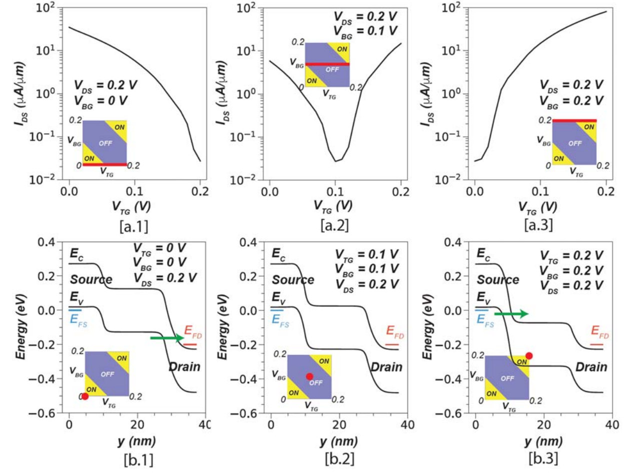

Fig. 2: *(upper row)* Simulated I_{DS}-V_{TG} transfer characteristics at V_{DS}=0.2 V for (a.1) V_{BG}=0 V, p-type; (a.2) V_{BG}=0.1 V, ambipolar; and (a.3) V_{BG}=0.2 V, n-type. *(lower row)* Simulated band diagrams at V_{DS}=0.2 V for (b.1) V_{TG}=V_{BG}=0 V, (b.2) V_{TG}=V_{BG}=0.1 V, and (b.3) V_{TG}=V_{BG}=0.2 V, exhibiting the same three distinctive operation regimes shown in Fig. 1(b). Corresponding bias conditions are shown as red dots or lines in the insets.

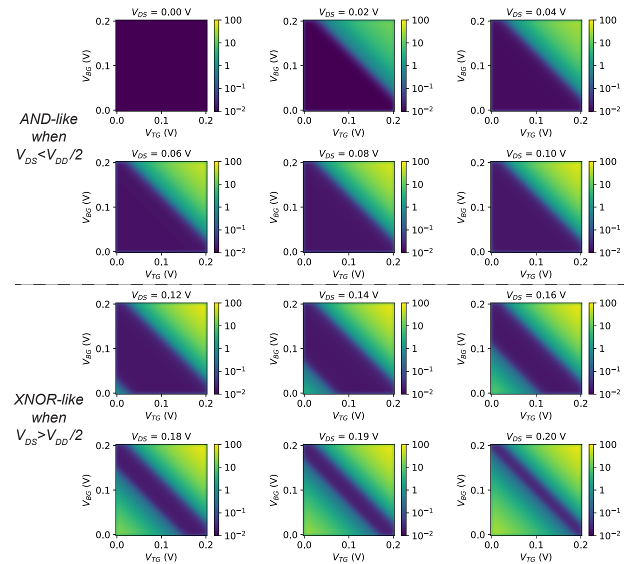

Fig. 4: A grid of 2D mappings of I_{DS} versus V_{TG} and V_{BG} at different V_{DS}. The color scheme represents current density (μA/μm) in logarithm scale.

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