GaN-Based Multi-Channel Transistors with Lateral Gate for Linear and Efficient Millimeter-Wave Power Amplifiers

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***Abstract*— We report on GaN-based field effect transistors with laterally-gated multiple 2DEG channels, called BRIDGE FETs (buried dual gate FETs). Unique operation principle of the transistors demonstrated unprecedented device characteristics suitable for efficient and linear millimeter-wave power amplifier applications. Multiple 2DEG channels formed in AlGaN/GaN and AlN/GaN material systems are compatible with the BRIDE FET structure, adding design flexibility for an increased drain current density with higher frequency performance. The BRIDGE FET fabricated on a 4-channel epi structure with a net 2DEG density of 1.2×10^{13} cm^{-2} exhibited 1.7× higher saturation current density than those on a single-channel with the same 2DEG density. This is attributed to a higher saturation velocity of 2DEG with a lower density per channel. Finally, hexagonal micro-scale device cells consisting of segmented BRIDGE FETs construct a power amplifier (PA) unit cell, where distributing heat sources uniformly over an entire PA cell area maximizes its area power density while minimizing a rise of the peak junction temperature.**

***Keywords*—GaN, BRIDGE FET, Laterally-Gated, Multiple 2DEG channels, Micro-Scale Device Array Structure, Linearity.**

I. INTRODUCTION

Today's complex communication systems require transceivers to process RF signals efficiently with large bandwidth and high fidelity. While GaN-based HEMT technology has advanced to reach higher power densities, it has not fundamentally changed the power requirements for the linearity performance. In this work, we demonstrate new material and transistor architectures to break traditional trade-off among power density, efficiency, linearity, and operating frequency of traditional GaN transistors.

II. EXPERIMENTAL DETAILS

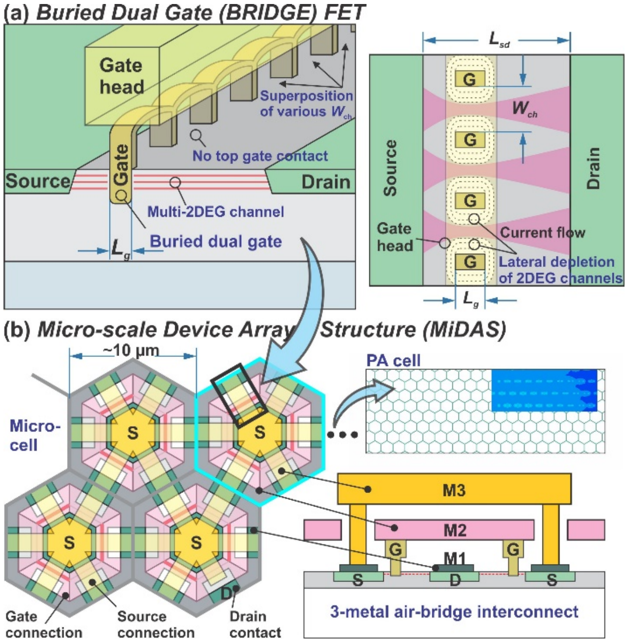

Fig. 1. Schematic illustration of GaN FET with buried dual gates (BRIDGE FET) (a) and micro-scale device array structure (MiDAS) to construct a high power density power amplifier cell (b).

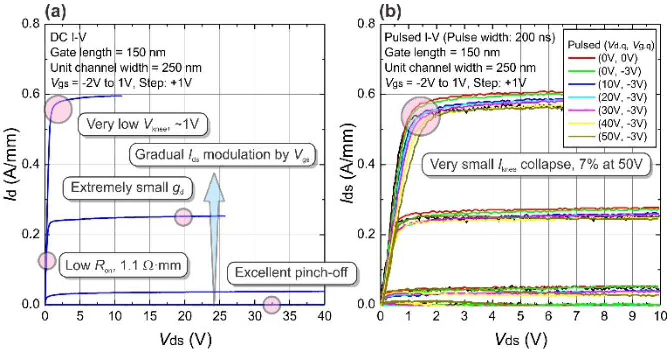

Fig. 2. Output (a) and pulsed I-V (pulse width = 200 ns) characteristics (b) of a single-channel 150-nm-gate BRIDGE FET.

Figure 1 shows GaN-based field effect transistors with buried dual gates (BRIDGE FET), where parallel gates buried into an Al(Ga)N/GaN HEMT epitaxial structure form lateral Schottky contacts to the 2DEG channel layer [1]. An absence of the top gate contact makes the device unique in contrast to conventional transistors in its operation principle; the drain current is controlled solely by modulating the width of the 2DEG while maintaining its sheet electron density (n_s). Due to the ohmic contact width (W_g) being wider than the active 2DEG width (W_{2DEG}), the applied drain voltage (V_{ds}) is concentrated in the channel between the buried gates. This enables (1) an early velocity saturation at a low V_{ds}, resulting in a low knee voltage (V_{knee}) of 1V, and (2) an effectively low on-resistance (R_{on}) of 1.1 Ω·mm. The buried gates that contact

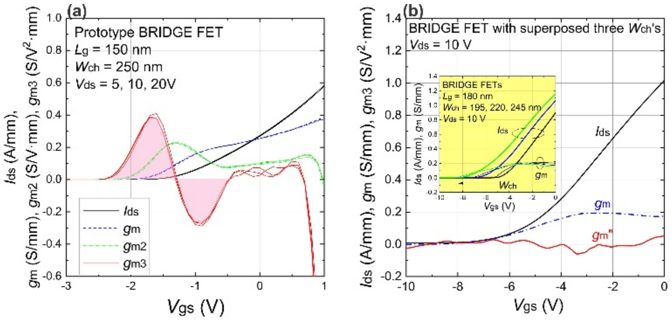

Fig. 3. Transfer characteristics of a single-channel 150-nm gate BRIDGE FET (a) and engineered transfer characteristics with negligible gm" (second derivative of gm) peaks realized in a BRIDGE FET consisting of three channel widths (b).

the GaN layer below the 2DEG enhances electron confinement, leading to an improved electrostatic isolation between source and drain, and therefore, good pinch-off characteristics and small output conductance (g_d) (Fig 2(a)). Deliberate elimination of a top-contact gate reduces the density of trapped electrons at a high field region near the surface and alleviates capacitive coupling between the trapped electrons and the 2DEG. The pulsed I-V measurement confirmed a large reduction of knee current collapse: only 7% at a quiescent drain voltage of 50V (Fig. 2(b)). One of the key linearity enhancing attributes of the BRIDGE FET is the gradual transfer characteristics due to its MESFET-like device operation. In conventional top gated HEMTs, g_m peaks at about 20-30% of the maximum drain current and decreases with increasing the gate bias (V_{gs}), which is due to a reduction of the electron velocity caused by n_s modulation [2]. The abrupt reduction of g_m near threshold voltage (V_{th}) is inherent to the vertical gate electric field in parallel to the direction of the 2DEG confinement in the channel. On the other hand, the gradual pinch off characteristics of the BRIDGE FET result in a greatly reduced the first and the second g_m derivatives (g_m', g_m") (Fig. 3(a)). The V_{th} of the BRIDGE FET can be precisely controlled by the channel width (W_{ch}), which allows for engineering a g_m profile by superposing three different W_{ch}'s to cancel g_m" peaks for improved large signal linearity performance (Fig. 3(b)).

RF performance of the BRIDGE FETs was improved through reduction of parasitic resistances and capacitances. A 180-nm-gate BRIDGE FET demonstrated a maximum oscillation frequency (f_{max}) of 250 GHz at 25V (Fig 4(a)). Soft gain compression is a known problem with GaN HEMT amplifiers and a significant cause of nonlinearity. To realize constant large signal gain over a wider range of input power, a uniform small-signal gain along the load line is desired. Figure 4(b) shows a contour plot of maximum stable gain (*MSG*) measured at 30 GHz for a BRIDGE FET. Owing to its unique g_m profile, low V_{knee}, and small g_d in combination with the reduction of the reduced gate-drain capacitance (C_{gd}) at higher V_{ds}, the BRIDGE FET exhibits almost constant *MSG* along the load line over a wide V_{ds} range.

The buried gate structure of the BRIDGE FET allows for simultaneous modulation of stacked 2DEG channels, enabling

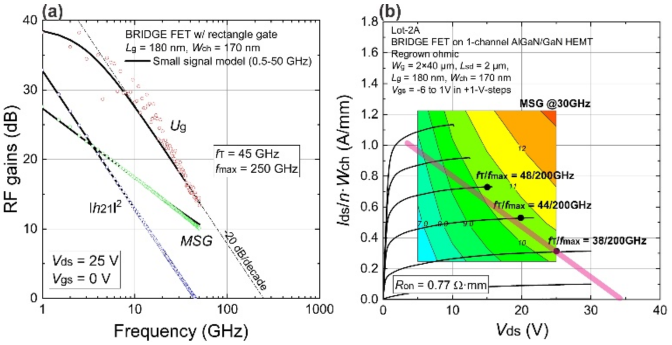

Fig. 4. RF characteristics and MSG contour of a single-channel 180-nm-gate BRIDGE FET.

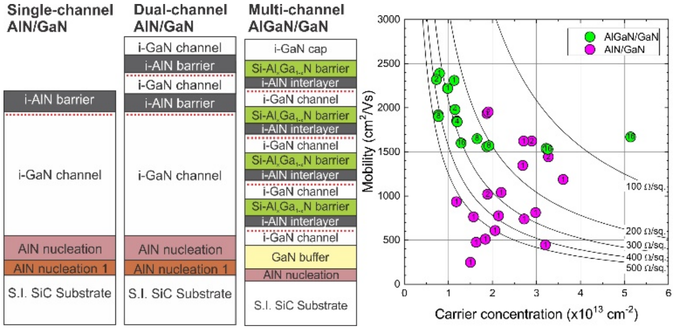

Fig. 5. Electrical properties of multiple 2DEG channel AlGaN/GaN and AlN/GaN epitaxial structures.

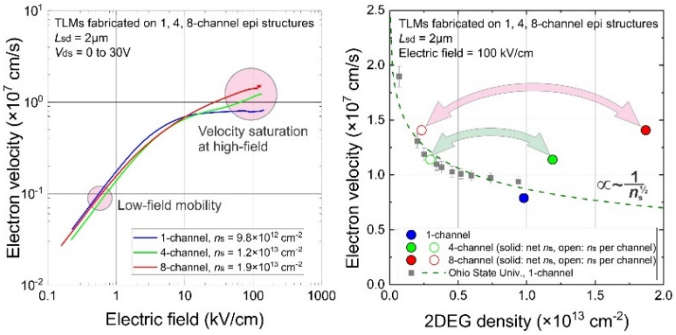

Fig. 6. Experimentally extracted electron velocity as a function of the electric field for single-, 4-, and 8-channel AlGaN/GaN HEMT epitaxial structures (a). Electron saturation velocity at a high field of 100 kV/cm plotted as a function of the 2DEG density (b).

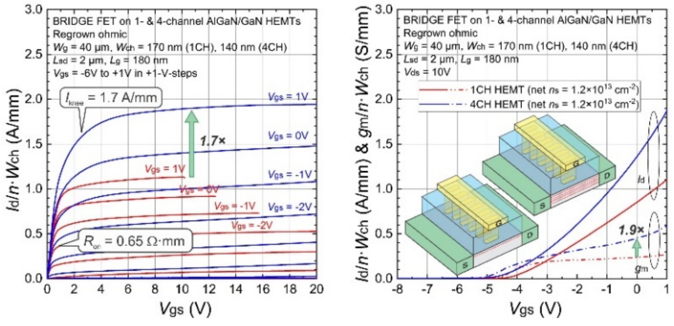

Fig. 7. Comparison of output (a) and transfer (b) characteristics between a single-and 4-channel BRIDGE FETs with the same net 2DEG density of 1.2×10^{13} cm^{-2}.

proportional power scaling with the net 2DEG density. Figure 5 illustrates electrical properties of AlGaN/GaN and AlN/GaN epitaxial structures consisting of a single and multiple 2DEG channel(s). Large net 2DEG densities of 5.2×10^{13} cm^{-3} and 3.2×10^{13} cm^{-3} with a high electron mobility of >1600 $cm^2/V\cdot s$ and >1400 $cm^2/V\cdot s$ have been obtained in a 16-channel AlGaN/GaN and a 2-channel AlN/GaN epitaxial structure, respectively. Electron velocities were extracted experimentally from two-terminal *I-V* characteristics of a TLM test structure fabricated on a single-, 2- and 4-channel HEMT epitaxial structures. Fig. 6(a) illustrates extracted electron velocity plotted as a function of the electric field. At low electric fields, electron velocities are similar among three structures, reflecting their similar electron mobility (~1600 $cm^2/V\cdot s$). Electron velocities at high electric fields (> 20 kV/cm), on the other hand, are higher for the 2- and 4-channel epi structures. This result is attributed to the density-dependent electron saturation velocity in GaN-based HEMTs, which is caused by a strong interaction between electrons and LO phonons [2,3]. The extracted electron velocities at a high electric field of 100 kV/cm are plotted as a function of the net 2DEG density (solid circles) as well as the 2DEG density per channel (open circles), which are compared with experimental and theoretical data for a single-channel HEMT structure reported by S. Bajaj *et al.* [3]. The data suggest that the higher electron saturation velocity in the multi-channel structures is due to a reduced 2DEG density per channel while maintaining their high net 2DEG densities enabled by stacking multiple channels. It should be noted that higher electron velocities obtained in multi-channel epi structures are beneficial for achieving not only high drain current density (= $q\cdot n\cdot v_s$) but also improved frequency performance of the transistors.

Fig. 7 compares DC characteristics of a single- and 4-channel BRIDGE FETs with the same net 2DEG density of 1.2×10^{13} cm^{-2}. The devices have a similar V_{th} of -4.5V. The 4-channel device exhibited an increased saturation current by 1.7× and g_m by 1.9× (at V_{gs} = 0V) as compared to the single-channel device. This is considered to be due to the increased electron velocity in the 4-channel epitaxial material with a reduced 2DEG density per channel (= 0.3×10^{13} cm^{-2}).

With increasing transistor's power density, a total available power from a PA cell is eventually limited by self-heating. To mitigate the limitation, we introduced a micro-scale device array (MiDAS) concept to minimize the peak junction temperature (T_j) during large signal operation (Fig. 1(b)). Thermal simulation demonstrated greatly reduced peak T_j in MiDAS device as compared to the conventional device with two gate fingers (Fig. 8).

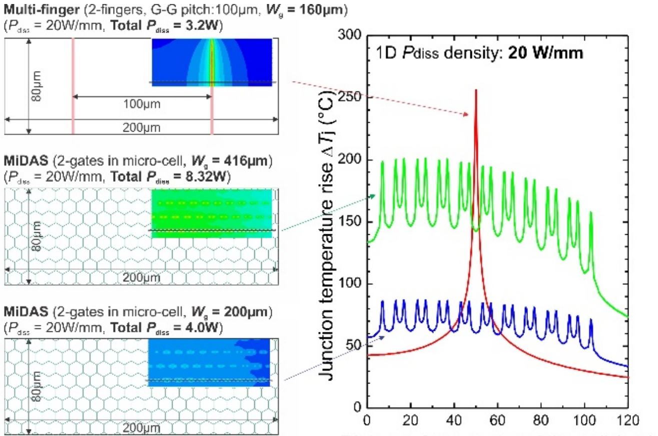

Fig. 8. Simulated temperature profiles for conventional 2-finger gate and MiDAS device architectures at a dissipated power density of 20 W/mm.

III. CONCLUSION

GaN-based FETs with buried dual gate (BRIDGE FETs) were fabricated using a single- and a 4-channel HEMT epitaxial structures. The unique operation principle of the BRIDGE FETs in combination with multi-2DEG-channel epitaxial structures offers performance advantages and design flexibility for efficient and linear operations in millimeter-wave power amplifiers. Furthermore, micro-scale device array concept was introduced to maximize the area output power density from a power amplifier cell by minimizing the peak junction temperature rise during large signal operation.

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REFERENCES

[1] K. Shinohara, C. King, A. D. Carter, E. J. Regan, A. Arias, J. Bergman, M. Urteaga, B. Brar, "GaN-Based Field-Effect Transistors With Laterally Gated Two-Dimensional Electron Gas", IEEE Electron Device Lett., vol. 39, no. 3, pp. 417-420, May 2012. doi: 10.1109/LED.2018.2797940.

[2] T. Fang, R. Wang, H. Xing, S. Rajan, and D. Jena, "Effect of Optical Phonon Scattering on the Performance of GaN Transistors," IEEE Electron Device Lett., vol. 33, no. 5, pp. 709-711, May 2012. doi: 10.1109/LED.2012.2187169.

[3] S. Bajaj, O. F. Shoron, P. S. Park, S. Krishnamoorthy, F. Akyol, T. Hung, S. Reza, E. M. Chumbes, J. Khurgin, and S. Rajan, "Density-dependent electron transport and precise modeling of GaN high electron mobility transistors," Appl. Phys. Lett., 107, 153504 (2015), doi: 10.1063/1.4933181.