

# Bottom tunnel junction blue light-emitting field-effect transistors

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## ABSTRACT

A recent thrust toward efficient modulated light emitters for use in Li-Fi communications has sparked renewed interest in visible III-N InGaN light-emitting diodes (LEDs). With their high external quantum efficiencies, blue InGaN LEDs are ideal components for such devices. We report a method for achieving voltage-controlled gate-modulated light emission using monolithic integration of fin- and nanowire-n-i-n vertical FETs with bottom-tunnel junction planar blue InGaN LEDs. This method takes advantage of the improved performance of bottom-tunnel junction LEDs over their top-tunnel junction counterparts, while allowing for strong gate control on a low-cross-sectional area fin or wire without sacrificing the LED active area as in lateral integration designs. Electrical modulation of five orders and an order of magnitude of optical modulation are achieved in the device.

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Visible light-emitting diodes (LEDs) based on the Indium Gallium Nitride (InGaN) material system have emerged as fundamental components in micro-LED display technology, car headlamps, and cell phone backlighting, among other lighting applications.<sup>1–7</sup> More recently, interest in InGaN LEDs has spread beyond lighting applications toward a different area—light fidelity (Li-Fi) communications—due to the promise of faster and more secure data transmission compared to conventional Wi-Fi.<sup>8,9</sup> InGaN LEDs are attractive for such applications due to their preponderance in lighting and also due to their high external quantum efficiencies (EQEs) in the visible spectral range—a range that is  $>2000\times$  larger in bandwidth than the entire RF spectral range and the one that is currently underutilized.<sup>10</sup>

In order to use LEDs for Li-Fi communications, high speed modulation of the LED light output is desirable. This modulation is achieved with the use of a current or voltage driver. In the GaAs semiconductor family, heterojunction bipolar transistors (HBTs) have been redesigned epitaxially into LEDs and even laser diodes (LDs) for current driven operation.<sup>11</sup> Although the Nitride semiconductor family allows for visible to UV emission wavelengths and higher power operation, to realize HBT-LEDs or HBT-LDs similar to GaAs requires the quantum well (QW) active region to be placed inside p-type base

layers, which are rather resistive and problematic for contact formation. Voltage-driven control methods involve simpler control schemes and offer more flexibility than current-driven methods.<sup>12–14</sup> Using GaN FETs directly integrated on the LED for voltage driving can take advantage of a single epitaxial step and the excellent performance demonstrated by vertical GaN FETs. Toward this end, integration of GaN-based FETs and LEDs on the same epi-wafer can enable high power and high efficiency voltage-controlled modulated visible light emission while eliminating interconnects and reducing the overall device footprint. Previous demonstrations integrating III-Nitride FETs and LED structures on the same epi-wafer for these applications involve lateral integration of High Electron Mobility Transistors (HEMTs) with the LED or vertical integration through a top-down full nanowire platform.<sup>15–23</sup> However, both strategies limit the LED active area on the wafer: the former strategy requires removing the LED epi from certain regions of the wafer (and in certain processes, an additional regrowth step to define the LED structure). The latter constrains the LED active volume down to the size of a gate-controllable nanowire, severely limiting the optical output power. The strategy demonstrated in this work offers a solution to both problems by integrating nanowire and fin vertical n-FETs on large-area planar LEDs

through top-down fabrication on a heterostructure that is realized in one epitaxial stack. This approach allows for strong all-around gate control on the relatively low cross-sectional area FETs, while allowing large area LEDs that take advantage of the on-wafer area for high output power.

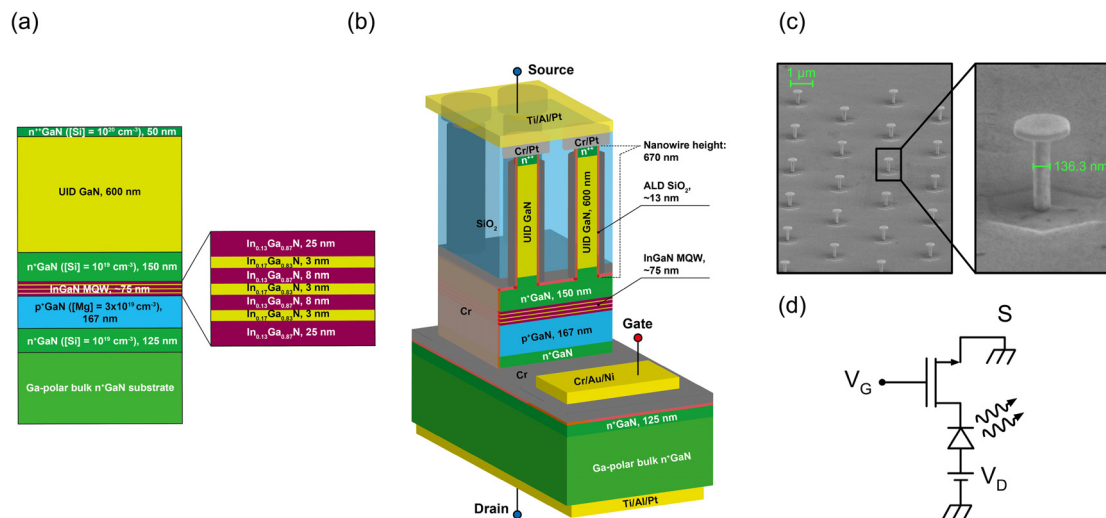
In order to vertically integrate nanowire- or fin-n-FETs with planar LEDs, the wires or fins must sit on top of the planar LED. This requires the top layer of the LED to be n-GaN rather than p-GaN. A tunnel junction (TJ) LED is required if conventional n-GaN substrates are used. This particular demonstration uses bottom-TJ homojunction LEDs, which have been shown to outperform standard top-TJ LEDs in terms of wall-plug efficiency,<sup>24,25</sup> with n-i-n vertical n-FETs on top, as shown in Fig. 1, with a circuit level schematic of light-emitting FET (LEFET) devices shown in Fig. 1(d).

The light-emitting FET (LEFET) structure was grown by plasma-assisted molecular beam epitaxy (PAMBE) in a single growth on a free standing Lumilog bulk n-type GaN substrate with a dislocation density of  $10^7 \text{ cm}^{-2}$ . The growth was performed using a Nitrogen RF plasma power of 400 W, corresponding to a growth rate of 420 nm/h. During growth, reflection high-energy electron diffraction (RHEED) was used to confirm a metal-rich growth condition, which promotes 2D growth in PAMBE.

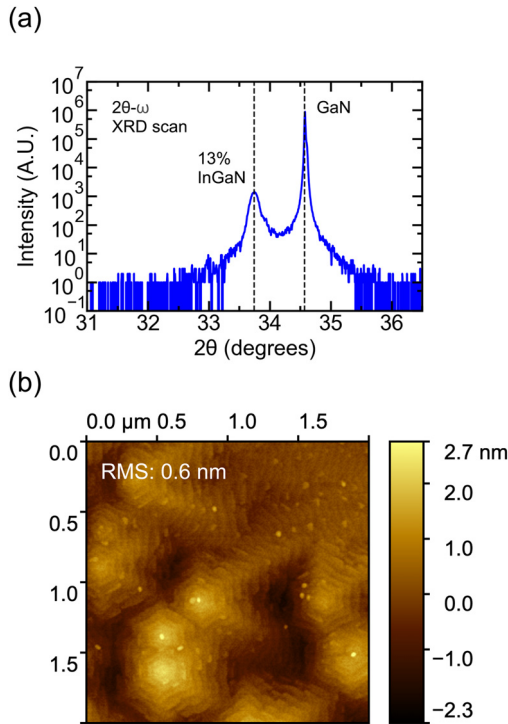
The epitaxial layer structure of the sample is shown in Fig. 1(a). The initial 125 nm  $n^+$ GaN:Si layer was grown at a thermocouple temperature of  $750^\circ\text{C}$  with a Si beam equivalent pressure (BEP) of  $3.8 \times 10^{-10}$  Torr. This BEP corresponds to a Si donor concentration of  $1.6 \times 10^{19} \text{ cm}^{-3}$ , as calibrated by secondary ion mass spectrometry (SIMS) on a separate sample. The substrate temperature was then reduced to  $745^\circ\text{C}$  to grow the 167 nm  $p^+$ GaN:Mg layer in order to enhance Mg incorporation. Mg BEP was kept at  $2.3 \times 10^{-8}$  Torr, corresponding to a Mg acceptor concentration of  $2 \times 10^{19} \text{ cm}^{-3}$ . After growing  $p^+$ GaN:Mg, the growth was interrupted to desorb excess Ga prior to active region growth. The active region consists of three 17% InGaN quantum wells (QWs) separated by 13% InGaN quantum

barriers (QBs), all grown at a lower temperature of  $657^\circ\text{C}$  to enhance Indium incorporation. After the active region, a 150 nm  $n^+$ GaN layer is grown followed by 600 nm of unintentionally doped (UID) GaN as the channel for the FET. Finally, a 50 nm degenerately doped  $n^+$ GaN ( $[\text{Si}] = 1 \times 10^{20} \text{ cm}^{-3}$ ) layer was grown as the source n-contact layer for the transistor.

Optical microscope images after the MBE growth showed Ga metal droplets on the surface, confirming the metal rich growth condition. After removing the droplets with HCl, structural characterization was performed through x-ray diffraction (XRD) and atomic force microscopy (AFM), with the results shown in Figs. 2(a) and 2(b), respectively. The XRD shows that the InGaN cladding composition in the LED is 13%, and the AFM shows a smooth surface (with a root mean square roughness of  $\sim 0.6 \text{ nm}$ ). After performing structural characterization, the sample was processed into devices consisting of various numbers of vertical n-FET nanowires or fins of varying dimensions on top of  $55 \times 55 \mu\text{m}^2$  LED mesas, in a similar manner to other GaN and  $\text{Ga}_2\text{O}_3$  vertical FETs.<sup>26–28</sup> A schematic of a processed nanowire LEFET is shown in Fig. 1(b). First,  $55 \times 55 \mu\text{m}^2$  LED areas were isolated through inductively coupled plasma reactive ion etching (ICP-RIE) down to the  $n^+$ GaN nucleation layer. Next, nanowires and fins were defined on the mesa surface through electron beam lithography (EBL). The etch process for nanowire/fin definition consisted of first an ICP etch (using Cr/Pt as an etch mask as well as a top source contact) followed by a wet etch in AZ400K to make the sidewalls vertical for efficient lateral gating [see Fig. 1(c)]. The fins were defined with the long edge along the m-plane direction in order to allow for adequate wet etching. Then,  $\text{SiO}_2$  was deposited by atomic layer deposition (ALD) as a gate dielectric for the nanowire/fin FETs. Next, Cr was sputtered as the sidewall gate metal, followed by e-beam evaporation of large Cr/Au/Ni pads for electrically contacting the gate. The undesired sputtered Cr above the source contact of the fins and wires was etched away after a planarization process, after which  $\text{SiO}_2$  was blanket deposited by plasma-enhanced chemical vapor deposition (PECVD)



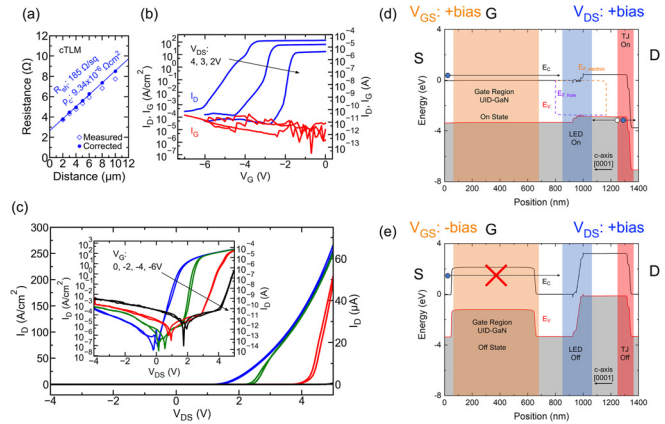
**FIG. 1.** (a) Epitaxial layer structure for the Light-Emitting FET (LEFET). The structure consists of a vertical n-i-n GaN FET sitting above a bottom-TJ homojunction InGaN LED. (b) Schematic of a fabricated nanowire LEFET structure, showing source, gate, and drain contacts for biasing the device, and dielectrics for isolation. (c) SEM image showing submicrometer nanowires with vertical sidewalls after wet etching, before removing the etch mask. (d) Circuit level schematic of the LEFET.



**FIG. 2.** (a) X-ray diffraction spectrum for the LEFET structure, showing a GaN substrate peak and an  $\text{In}_{0.13}\text{Ga}_{0.87}\text{N}$  peak from the LED cladding regions. (b)  $2 \times 2 \mu\text{m}^2$  AFM scan for the structure in this study immediately after MBE growth. Atomic steps and relatively low RMS roughness are observed, with some threading dislocation features present due to propagation from the substrate.

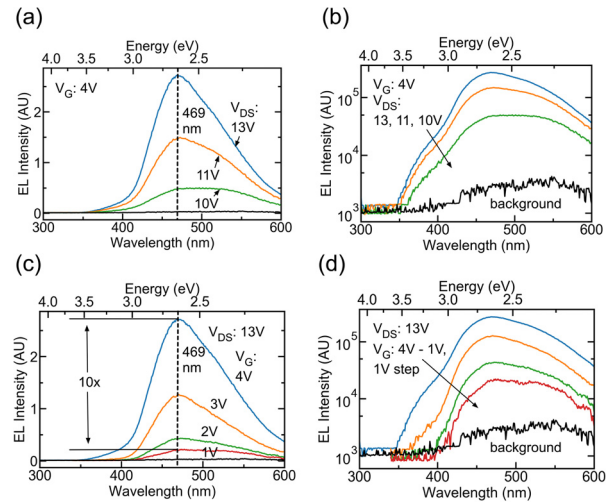
to isolate the rest of the sidewall gate metal. This  $\text{SiO}_2$  was then planarized to again expose the Cr/Pt wire/fin source contact, after which thick source pads (Ti/Al/Pt) for probing were deposited. Gate isolation for the FET wires/fins between different devices (which still had their gates shorted together by the sputtered Cr at this point) and contact holes for the thick gate pads was realized together with an  $\text{SiO}_2$  etch followed by a Cr etch. Finally, a Ti/Al/Pt back contact was deposited with a window left free of metal for collecting light from the back side.

After device processing, electrical and optical measurements were performed, with the results for a  $500 \text{ nm} \times 50 \mu\text{m}$  single-fin depletion-mode device shown in Figs. 3 and 4, respectively. Compared to the multi-fin/wire devices, the single fin/wire devices showed lower gate leakage current and higher on/off ratios due to the reduced gate area. Circular transfer length method (cTLM) measurements shown in Fig. 3(a) reveal low contact and sheet resistances of  $9.34 \times 10^{-6} \Omega \text{ cm}^2$  for the top source contact and  $185 \Omega/\text{sq}$  for the  $n^{++}$  GaN contact layer underneath, resulting in negligible voltage drops across these regions.  $I_D$ - $V_G$  and  $I_D$ - $V_D$  measurements on the  $500 \text{ nm} \times 50 \mu\text{m}$  single-fin device are shown in Figs. 3(b) and 3(c), respectively, with current density values shown on the plots normalized to the area of the fin FET. From the  $I_D$ - $V_G$  curve in Fig. 3(b), an on/off ratio of  $\sim 5$  orders is observed up to  $V_{DS} = 4 \text{ V}$ , with gate leakage current low in all cases (below  $\sim 100 \text{ pA}$ ). The on current increases with increasing  $V_{DS}$  as expected due to the turn-on of the LED pn diode. The  $I_D$ - $V_D$  measurements in Fig. 3(c) show that



**FIG. 3.** (a) Circular TLM data for the source contact of the LEFET. (b)  $I_D$ - $V_G$  measurement for a single-fin device with fin dimensions of  $500 \text{ nm} \times 50 \mu\text{m}$  and LED dimensions of  $55 \times 55 \mu\text{m}^2$ . Current density is calculated using the area of the fin. (c) Linear  $I_D$ - $V_D$  characteristic (with the log scale in the inset) showing reduction in on current of  $\sim 100\times$  at  $V_{DS} = 5 \text{ V}$  as  $V_G$  is reduced from  $0 \text{ V}$  to  $-6 \text{ V}$ . (d) and (e) Qualitative depiction of band diagrams for the device in the on and off states, respectively. With a fixed positive  $V_{DS}$ , switching  $V_G$  from positive to negative biases modulates electron conduction across the FET channel and allows voltage to drop across the diode.

between  $V_G = 0 \text{ V}$  and  $V_G = -6 \text{ V}$ , a two order gate modulation of the on current is achieved at  $V_{DS} = +5 \text{ V}$ . Figures 3(e) and 3(f) depict the energy band diagrams of the LEFET device in the on and off states, respectively, when biased in a manner applicable for Li-Fi purposes: modulating  $V_G$  with fixed forward bias  $V_{DS}$ . In ideal operation,



**FIG. 4.** (a) and (b) Linear and log scale plots, respectively, of electroluminescence (EL) intensity vs wavelength for a single-fin device, with  $V_G$  fixed at  $+4 \text{ V}$ . The EL intensity rises as expected with increasing  $V_{DS}$  as the level of forward bias across the diode is increased. (c) and (d) Linear and log scale plots, respectively, of EL intensity vs wavelength for the same device, with  $V_{DS}$  fixed at  $13 \text{ V}$ . A factor of 10 reduction in EL intensity is observed as  $V_G$  is decreased from  $+4 \text{ V}$  to  $+1 \text{ V}$ , demonstrating the gate's ability to limit electron transport into the LED. At  $V_G = 0 \text{ V}$ , light is still emitted although, at a low intensity, the detector is not sensitive enough to resolve.

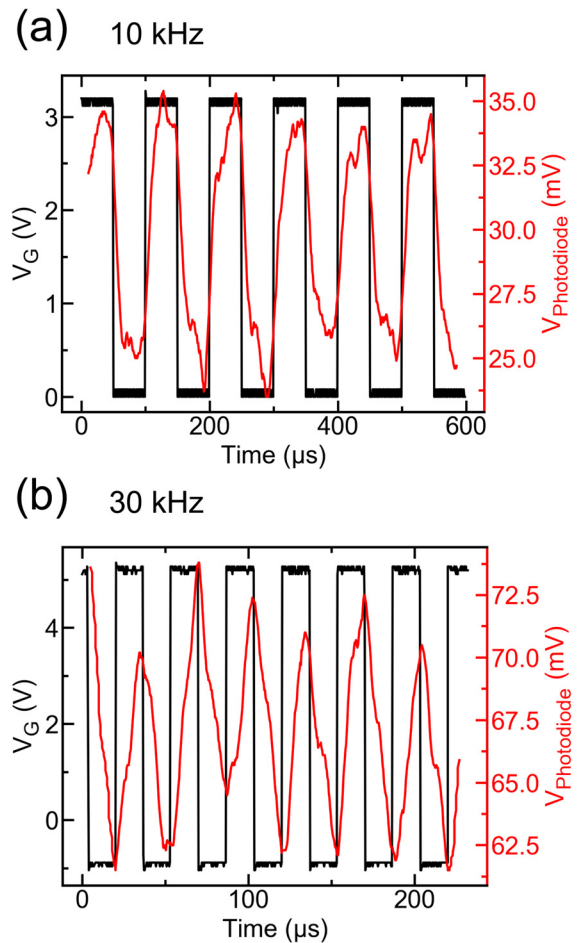
electrons are injected into the LED portion of the device from the transistor source only when  $V_G$  is switched to a sufficiently high positive voltage.

The measured electroluminescence (EL) spectra are shown in Fig. 4, demonstrating the optical modulation enabled by the FinFET. Figures 4(a) and 4(b) show the effect of the drain voltage on the emission spectra on linear and log scales for the  $500 \text{ nm} \times 50 \mu\text{m}$  single fin device at a fixed  $V_G = 4 \text{ V}$  for  $V_{DS}$  between  $10 \text{ V}$  and  $13 \text{ V}$ . With larger  $V_{DS}$ , more light is emitted from the device due to a larger forward bias appearing across the LED portion of the device.  $V_{DS}$  used here is higher than that in the electrical measurements due to the limited sensitivity of the optical detection setup used for this work. The emission peak appears at  $469 \text{ nm}$ , consistent with a 17% average Indium composition in the QWs.

Figures 4(c) and 4(d) demonstrate the desired modulation of the EL spectra through gating of the GaN FinFET. At a fixed  $V_{DS} = 13 \text{ V}$ , varying  $V_G$  from  $+4 \text{ V}$  to  $+1 \text{ V}$  results in a reduction of EL intensity by a factor of 10. Larger on/off modulation ratios are achieved at lower  $V_{DS}$  although the optical measurement apparatus used is not sensitive enough to measure them. Gate control is limited at these high  $V_{DS}$  values at which light can be collected by the detector due to the high gate–drain field. The brightness of the LED at lower  $V_{DS}$  can be drastically increased through the use of a heterojunction GaN/InGaN/GaN buried tunnel junction rather than a homojunction, leading to a lower series resistance, as demonstrated in previous work.<sup>25</sup> Such devices show strong EL at current densities of  $\sim 1 \text{ kA/cm}^2$  (corresponding to  $\sim 5 \text{ V}$ )—a  $V_{DS}$  voltage/field at which the FET portion of this device shows  $\sim 5$  orders of on/off ratio. Additionally, increasing the thickness of the  $n^+$  GaN layer between the fin-FET and planar LED active region will enhance current spreading, increasing optical output power.

For visible light communications, switching speed is an important parameter that dictates data transmission rates. The optical switching speed of the device was measured by switching  $V_G$  with  $V_{DS}$  fixed at  $10 \text{ V}$  and tracking the output signal from a photodiode placed directly underneath the device using an oscilloscope. A square voltage pulse with a duty cycle of 50% was used as the input signal on the gate, with the frequency varying between  $1 \text{ kHz}$  and  $100 \text{ kHz}$ . The input electrical signal (black) and output photodiode voltage signal (red) are shown in Fig. 5 for frequencies of  $10$  and  $30 \text{ kHz}$ . Limitations of the optical collection setup result in a low signal to noise ratio, and so a Savitzky–Golay filter was used after collecting the data to reduce the noise in the photodiode output signal. The device maintains an optical switching response up to  $30 \text{ kHz}$ , beyond which the optical response flattens out. Although this modulation proves the feasibility of the LEFET for direct voltage modulation of light, the current design of the device geometry is not optimal for the much higher speeds necessary. Future designs will require careful control of the UID GaN thickness and the sidewall gate dielectric and the resulting gate capacitance to enhance the gate-voltage modulation speed of the optical output power.

We have demonstrated a technique for achieving monolithic integration of n-FETs and LEDs, using vertical fin- and nanowire-FETs and bottom tunnel junction planar blue LEDs. This platform allows for strong gate control ( $\sim 5$  orders of magnitude on/off for  $I_D$ ) without limiting the on-wafer LED active area and does not require regrowth. Optical switching behavior up to  $30 \text{ kHz}$  is demonstrated in the first prototype, with room for improvement through the use of



**FIG. 5.** (a) and (b) Switching measurements performed on the  $500 \text{ nm} \times 50 \mu\text{m}$  single fin device with a 50% duty cycle square wave applied to the gate at frequencies of  $10 \text{ kHz}$  and  $30 \text{ kHz}$ , respectively. For the  $10 \text{ kHz}$  measurement,  $V_G$  is switched from  $0$  to  $+3 \text{ V}$ , while for the  $30 \text{ kHz}$  measurement,  $V_G$  is switched from  $-1 \text{ V}$  to  $+4 \text{ V}$ .  $V_{DS}$  is held constant at  $10 \text{ V}$  for both measurements. The black signal denotes the input voltage  $V_G$ , while the red signal is the response measured by a photodiode placed  $\sim 2 \text{ cm}$  away from the sample. A Savitzky–Golay filter was used to reduce noise in the photodiode response.

InGaN heterojunction TJs. The LEFET device geometry can be easily modified for light extraction from the surface without sacrificing significant wafer area by patterning the top source contact. Such devices are promising for use in Li-Fi communications and in micro-LED displays, in which gate voltage controllability and utility of space are important parameters. The technique described here can be applied to integrate vertical fin-FETs with laser diodes, enabling efficient directional Li-Fi emitters among other technologies.

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## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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